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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5634eydfb-30

1.Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline.

Table 1.1 Outline of Specifications (1 / 4)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 54 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • Memory-protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 1 M/1.5 M/2 Mbytes • 54 MHz, no-wait memory access • On-board programming: 3 types Off-board programming
	RAM	• Capacity: 128 Kbytes • 54 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 32 Kbytes • Number of times for programming/erasing: 100,000
MCU operating mode		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	• Main clock oscillator, low-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection • Measuring circuit for accuracy of clock frequency (clock-accuracy check: CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLKB), external bus clock (BCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 54 MHz (at max.) Peripheral modules run in synchronization with the peripheral module clock (PCLKB): 32 MHz (at max.) Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 27 MHz (at max.) The flash peripheral circuit runs in synchronization with the FlashIF clock (FCLK): 32 MHz (at max.)
Reset		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset
Voltage detection	Voltage detection circuit	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. The detection voltage level of voltage detection circuit 0 is fixed Voltage detection circuit 1 is capable of selecting the detection voltage from 3 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 3 levels
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, low-speed operating mode 1, low-speed operating mode 2
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 178 • External interrupts: 14 (NMI, IRQ0 to IRQ12 pins) • Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority

Table 1.1 Outline of Specifications (2 / 4)

Classification	Module/Function	Description
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8-bit or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	144-pin • I/O: 114 • Input: 9 (P40 to P47, P35) • Pull-up resistors: 111 • Open-drain outputs: 114 • 5-V tolerance: Not supported
Event link controller (ELC)		• Event signals of 56 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for ports B and E
Multi-function pin controller (MPC)		• Capable of selecting input/output function from multiple pins
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Supports the input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available with six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 1 unit • Pulse output with the MTU output as a trigger • Maximum of 16 pulse-output possible
	8-bit timer (TMR)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Capable of generating a receive clock for the RCR
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1 / 4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	—	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	—	Connect this pin to the VSS pin via the 0.1 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	—	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
Clock frequency accuracy measurement	CACREF	Input	Input for the trigger signal in measuring accuracy of the clock frequency
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the onchip emulator is used, this pin should be driven high. When not used, it should be driven low.
On-chip emulator	FINEC	Input	Fine interface clock pin
	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC#	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0# to WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0# to BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
	WAIT#	Input	Input pin for wait request signals in access to the external space.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.

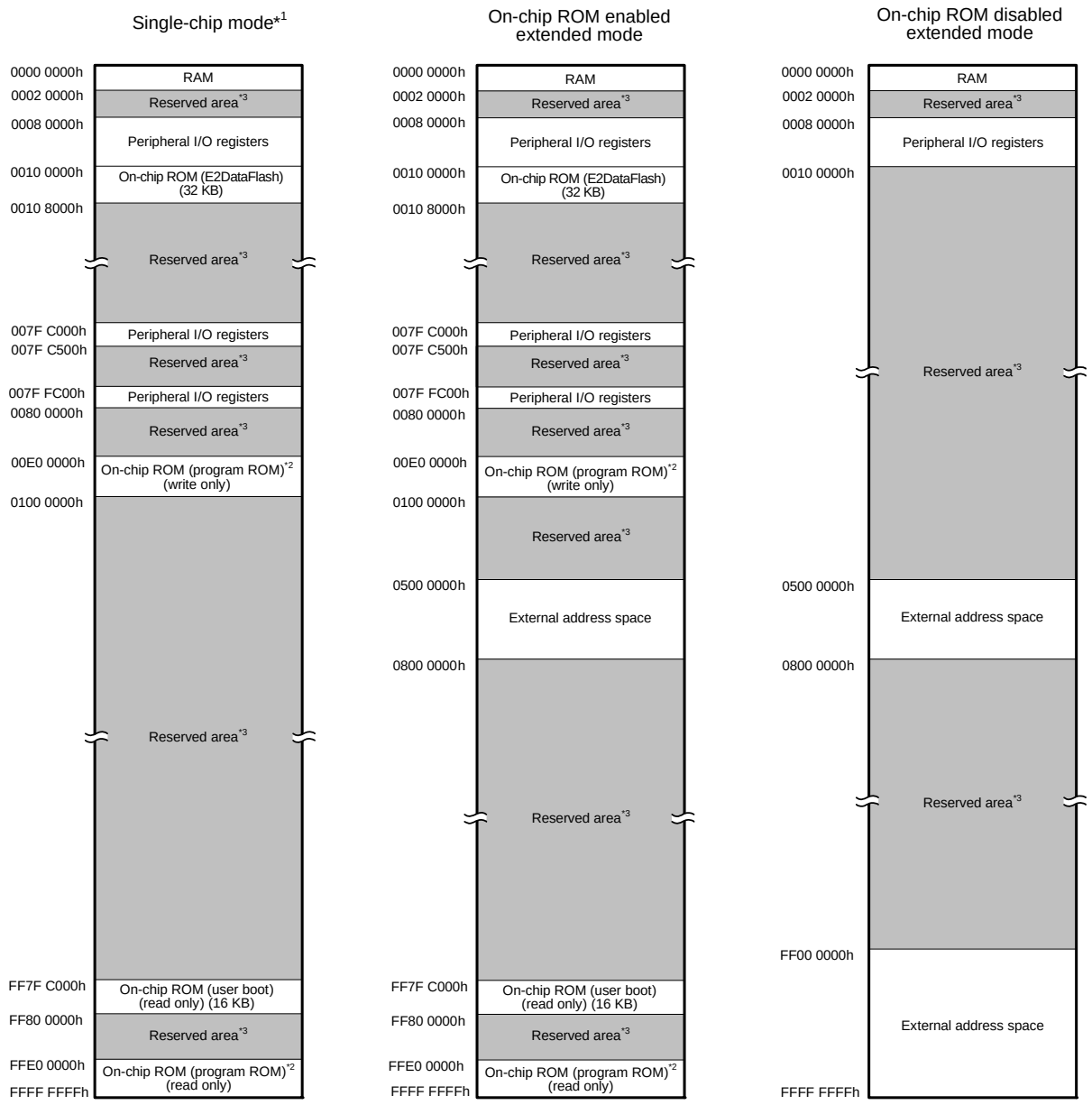
Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (1 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, POE, PPG, CAC)	Communications (SCIe, SCIf, RSPI, RIIC, CEC, RCR)	Interrupt	AD, DA
1	AVSS0						
2		P05					DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMCI1	SCK6	IRQ10	
7		P01		TMCI0	RXD6/SMISO6/SSCL6/PMC1	IRQ9	
8		P00		TMRI0	TXD6/SMOSI6/SSDA6/PMC0	IRQ8	
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS0#/RTS0#/SS0#/CTS6#/ RTS6#/SS6#		
14	VCL						
15		PJ1		MTIOC3A			
16	MD/FINED						
17		PJ2					
18		PJ4					
19	RES#						
20	XTAL						
21	VSS						
22	EXTAL						
23	VCC						
24		P35				NMI	
25	TRST#	P34		MTIOC0A/TMCI3/POE2#/ PO12	SCK0/SCK6	IRQ4	
26		P33		MTIOC0D/TIOCD0/TMRI3/ POE3#/PO11	RXD0/SMISO0/SSCL0/RXD6/ SMISO6/SSCL6	IRQ3_DS	
27		P32		MTIOC0C/TIOCC0/TMO3/ PO10	TXD0/SMOSI0/SSDA0/TXD6/ SMOSI6/SSDA6	IRQ2_DS	
28	TMS	P31		MTIOC4D/TMCI2/PO9	CTS1#/RTS1#/SS1#/SSLB0	IRQ1_DS	
29	TDI	P30		MTIOC4B/TMRI3/POE8#/ PO8	RXD1/SMISO1/SSCL1/MISOB	IRQ0_DS	
30	FINEC/TCK	P27	CS3#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
31	TDO	P26	CS2#	MTIOC2A/TMO1/PO6	TXD1/SMOSI1/SSDA1/CTS3#/ RTS3#/SS3#/MOSIB		
32		P25	CS1#	MTIOC4C/MTCLKB/TIOCA4/ PO5	RXD3/SMISO3/SSCL3		ADTRG0#
33		P24	CS0#	MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4	SCK3		
34		P23		MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/SSDA3/CTS0#/ RTS0#/SS0#		
35		P22		MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2	SCK0		
36		P21		MTIOC1B/TIOCA3/TMCI0/ PO1	RXD0/SMISO0/SSCL0/SCL1	IRQ9	
37		P20		MTIOC1A/TIOCB3/TMRI0/ PO0	TXD0/SMOSI0/SSDA0/SDA1	IRQ8	
38		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ POE8#/PO15	SCK1/TXD3/SMOSI3/SSDA3/ MISOA/SDA0_DS	IRQ7	

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The ROM capacity differs depending on the products.

ROM (Byte)			RAM (Byte)	
Capacity	Address (for Reading)	Address (for Writing)	Capacity	Address
2 M	FFE0 0000h to FFFF FFFFh	00E0 0000h to 00FF FFFFh	128 K	0000 0000h to 0001 FFFFh
1.5 M	FFE8 0000h to FFFF FFFFh	00E8 0000h to 00FF FFFFh	128 K	0000 0000h to 0001 FFFFh
1 M	FFF0 0000h to FFFF FFFFh	00F0 0000h to 00FF FFFFh	128 K	0000 0000h to 0001 FFFFh

Note: See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (2 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACA	
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 201Fh	DMAC0	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 205Fh	DMAC1	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 209Fh	DMAC2	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 20DFh	DMAC3	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2200h	DMAC	DMA Module Activation Register	DMAST	8	8	2 ICLK			
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK		DTCa	
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK			
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK			
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK			
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK			
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1 to 2BCLK		Buses	
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1 to 2BCLK			
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1 to 2BCLK			
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1 to 2BCLK			
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1 to 2BCLK			
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1 to 2BCLK			

Table 4.1 List of I/O Registers (Address Order) (5 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK		ICUb	
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK			
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK			
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK			
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK			
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK			
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK			
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK			
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK			
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK			
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK			
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK			
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK			
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK			
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK			
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK			
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK			
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK			
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK			
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK			
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK			
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK			
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK			
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK			
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK			
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK			
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK			
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK			
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK			
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK			
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK			
0008 7093h	ICU	Interrupt Request Register 147	IR147	8	8	2 ICLK			
0008 7094h	ICU	Interrupt Request Register 148	IR148	8	8	2 ICLK			
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK			
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK			
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK			
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK			
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK			
0008 709Ah	ICU	Interrupt Request Register 154	IR154	8	8	2 ICLK			
0008 709Bh	ICU	Interrupt Request Register 155	IR155	8	8	2 ICLK			
0008 709Ch	ICU	Interrupt Request Register 156	IR156	8	8	2 ICLK			
0008 709Dh	ICU	Interrupt Request Register 157	IR157	8	8	2 ICLK			
0008 709Eh	ICU	Interrupt Request Register 158	IR158	8	8	2 ICLK			
0008 709Fh	ICU	Interrupt Request Register 159	IR159	8	8	2 ICLK			
0008 70A0h	ICU	Interrupt Request Register 160	IR160	8	8	2 ICLK			
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK			
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK			
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK			
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK			
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK			
0008 70A6h	ICU	Interrupt Request Register 166	IR166	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (19 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 8694h	MTU4	Noise Filter Control Register	NFCR	8	8, 16	2 to 3PCLKB	2 ICLK	MTU2a	
0008 8695h	MTU5	Noise Filter Control Register	NFCR	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 8700h	MTU0	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8701h	MTU0	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		
0008 8702h	MTU0	Timer I/O Control Register H	TIORH	8	8	2 to 3PCLKB	2 ICLK		
0008 8703h	MTU0	Timer I/O Control Register L	TIORL	8	8	2 to 3PCLKB	2 ICLK		
0008 8704h	MTU0	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8705h	MTU0	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8706h	MTU0	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8708h	MTU0	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 870Ah	MTU0	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 870Ch	MTU0	Timer General Register C	TGRC	16	16	2 to 3PCLKB	2 ICLK		
0008 870Eh	MTU0	Timer General Register D	TGRD	16	16	2 to 3PCLKB	2 ICLK		
0008 8720h	MTU0	Timer General Register E	TGRE	16	16	2 to 3PCLKB	2 ICLK		
0008 8722h	MTU0	Timer General Register F	TGRF	16	16	2 to 3PCLKB	2 ICLK		
0008 8724h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	2 to 3PCLKB	2 ICLK		
0008 8726h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 to 3PCLKB	2 ICLK		
0008 8780h	MTU1	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8781h	MTU1	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		
0008 8782h	MTU1	Timer I/O Control Register	TIOR	8	8	2 to 3PCLKB	2 ICLK		
0008 8784h	MTU1	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8785h	MTU1	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8786h	MTU1	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8788h	MTU1	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 878Ah	MTU1	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 8790h	MTU1	Timer Input Capture Control Register	TICCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8800h	MTU2	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8801h	MTU2	Timer Mode Register	TMDR	8	8	2 to 3PCLKB	2 ICLK		
0008 8802h	MTU2	Timer I/O Control Register	TIOR	8	8	2 to 3PCLKB	2 ICLK		
0008 8804h	MTU2	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8805h	MTU2	Timer Status Register	TSR	8	8	2 to 3PCLKB	2 ICLK		
0008 8806h	MTU2	Timer Counter	TCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8808h	MTU2	Timer General Register A	TGRA	16	16	2 to 3PCLKB	2 ICLK		
0008 880Ah	MTU2	Timer General Register B	TGRB	16	16	2 to 3PCLKB	2 ICLK		
0008 8880h	MTU5	Timer Counter U	TCNTU	16	16	2 to 3PCLKB	2 ICLK		
0008 8882h	MTU5	Timer General Register U	TGRU	16	16	2 to 3PCLKB	2 ICLK		
0008 8884h	MTU5	Timer Control Register U	TCRU	8	8	2 to 3PCLKB	2 ICLK		
0008 8886h	MTU5	Timer I/O Control Register U	TIORU	8	8	2 to 3PCLKB	2 ICLK		
0008 8890h	MTU5	Timer Counter V	TCNTV	16	16	2 to 3PCLKB	2 ICLK		
0008 8892h	MTU5	Timer General Register V	TGRV	16	16	2 to 3PCLKB	2 ICLK		
0008 8894h	MTU5	Timer Control Register V	TCRV	8	8	2 to 3PCLKB	2 ICLK		
0008 8896h	MTU5	Timer I/O Control Register V	TIORV	8	8	2 to 3PCLKB	2 ICLK		
0008 88A0h	MTU5	Timer Counter W	TCNTW	16	16	2 to 3PCLKB	2 ICLK		
0008 88A2h	MTU5	Timer General Register W	TGRW	16	16	2 to 3PCLKB	2 ICLK		
0008 88A4h	MTU5	Timer Control Register W	TCRW	8	8	2 to 3PCLKB	2 ICLK		
0008 88A6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 to 3PCLKB	2 ICLK		
0008 88B2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 to 3PCLKB	2 ICLK		
0008 88B4h	MTU5	Timer Start Register	TSTR	8	8	2 to 3PCLKB	2 ICLK		
0008 88B6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 to 3PCLKB	2 ICLK		
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	16	2 to 3PCLKB	2 ICLK	POE2a	
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	16	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (25 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 B126h	ELC	Port Group Control Register 2	PGC2	8	8	2 to 3PCLKB	2 ICLK	ELC	
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 to 3PCLKB	2 ICLK		
0008 B128h	ELC	Port Buffer Register 2	PDBF2	8	8	2 to 3PCLKB	2 ICLK		
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Bh	ELC	Event Link Port Setting Register 2	PEL2	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Ch	ELC	Event Link Port Setting Register 3	PEL3	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 to 3PCLKB	2 ICLK		
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK	SCIe, SCIf	
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 B309h	SCI12	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Ah	SCI12	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Bh	SCI12	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Ch	SCI12	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2 to 3PCLKB	2 ICLK		
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 to 3PCLKB	2 ICLK		
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 to 3PCLKB	2 ICLK		
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 to 3PCLKB	2 ICLK		
0008 B327h	SCI12	Status Register	STR	8	8	2 to 3PCLKB	2 ICLK		
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 to 3PCLKB	2 ICLK		
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 to 3PCLKB	2 ICLK		
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 to 3PCLKB	2 ICLK		
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK	I/O Ports	
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C006h	PORT6	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (27 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK	I/O Ports	
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C066h	PORT6	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C067h	PORT7	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C068h	PORT8	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C069h	PORT9	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Fh	PORTF	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C073h	PORTK	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C074h	PORTL	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C080h	PORT0	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Ah	PORT5	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Bh	PORT5	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Ch	PORT6	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Eh	PORT7	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Fh	PORT7	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0A6h	PORTK	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0A7h	PORTK	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C6h	PORT6	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C7h	PORT7	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C8h	PORT8	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C9h	PORT9	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (30 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C19Ch	MPC	PB4 Pin Function Control Registers	PB4PFS	8	8	2 to 3PCLKB	2 ICLK	MPC	
0008 C19Dh	MPC	PB5 Pin Function Control Registers	PB5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C19Eh	MPC	PB6 Pin Function Control Registers	PB6PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C19Fh	MPC	PB7 Pin Function Control Registers	PB7PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A0h	MPC	PC0 Pin Function Control Registers	PC0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A1h	MPC	PC1 Pin Function Control Registers	PC1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A2h	MPC	PC2 Pin Function Control Registers	PC2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A3h	MPC	PC3 Pin Function Control Registers	PC3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A4h	MPC	PC4 Pin Function Control Registers	PC4PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A5h	MPC	PC5 Pin Function Control Registers	PC5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A6h	MPC	PC6 Pin Function Control Registers	PC6PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A7h	MPC	PC7 Pin Function Control Registers	PC7PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A8h	MPC	PD0 Pin Function Control Registers	PD0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1A9h	MPC	PD1 Pin Function Control Registers	PD1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1AAh	MPC	PD2 Pin Function Control Registers	PD2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1ABh	MPC	PD3 Pin Function Control Registers	PD3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1ACh	MPC	PD4 Pin Function Control Registers	PD4PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1ADh	MPC	PD5 Pin Function Control Registers	PD5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1AEh	MPC	PD6 Pin Function Control Registers	PD6PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1AFh	MPC	PD7 Pin Function Control Registers	PD7PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B0h	MPC	PE0 Pin Function Control Registers	PE0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B1h	MPC	PE1 Pin Function Control Registers	PE1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B2h	MPC	PE2 Pin Function Control Registers	PE2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B3h	MPC	PE3 Pin Function Control Registers	PE3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B4h	MPC	PE4 Pin Function Control Registers	PE4PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B5h	MPC	PE5 Pin Function Control Registers	PE5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B6h	MPC	PE6 Pin Function Control Registers	PE6PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1B7h	MPC	PE7 Pin Function Control Registers	PE7PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1BDh	MPC	PF5 Pin Function Control Registers	PF5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1C8h	MPC	PH0 Pin Function Control Registers	PH0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1C9h	MPC	PH1 Pin Function Control Registers	PH1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1CAh	MPC	PH2 Pin Function Control Registers	PH2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1CBh	MPC	PH3 Pin Function Control Registers	PH3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1D1h	MPC	PJ1 Pin Function Control Registers	PJ1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1D3h	MPC	PJ3 Pin Function Control Registers	PJ3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1DAh	MPC	PK2 Pin Function Control Registers	PK2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1DBh	MPC	PK3 Pin Function Control Registers	PK3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1DCh	MPC	PK4 Pin Function Control Registers	PK4PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1DDh	MPC	PK5 Pin Function Control Registers	PK5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C1E5h	MPC	PL5 Pin Function Control Register	PL5PFS	8	8	2 to 3PCLKB	2 ICLK		Not available in 5-V packages.
0008 C280h	SYSTEM	Deep Standby Control Register	DPSBYCR	8	8	4 to 5PCLKB	2 to 3 ICLK	Low Power Consumption	
0008 C282h	SYSTEM	Deep Standby Interrupt Enable Register 0	DPSIER0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C284h	SYSTEM	Deep Standby Interrupt Enable Register 2	DPSIER2	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C286h	SYSTEM	Deep Standby Interrupt Flag Register 0	DPSIFR0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 to 5PCLKB	2 to 3 ICLK	Resets	
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 to 5PCLKB	2 to 3 ICLK		

Table 4.1 List of I/O Registers (Address Order) (33 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 0B16h	RCR0	Receive Data 0 Register	DAT0	8	8	1 to 2PCLK	1 ICLK	RCR	Not available in 5-V packages.
000A 0B17h	RCR0	Receive Data 1 Register	DAT1	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B18h	RCR0	Receive Data 2 Register	DAT2	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B19h	RCR0	Receive Data 3 Register	DAT3	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B1Ah	RCR0	Receive Data 4 Register	DAT4	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B1Bh	RCR0	Receive Data 5 Register	DAT5	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B1Ch	RCR0	Receive Data 6 Register	DAT6	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B1Dh	RCR0	Receive Data 7 Register	DAT7	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B1Eh	RCR0	Measurement Result Register	TIM	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B80h	RCR1	Function Select Register 0	CON0	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B81h	RCR1	Function Select Register 1	CON1	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B82h	RCR1	Status Register	STS	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B83h	RCR1	Interrupt Control Register	INT	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B84h	RCR1	Compare Control Register	CPC	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B85h	RCR1	Compare Value Setting Register	CPD	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B86h	RCR1	Header Pattern Setting Register (Min)	HDPMIN	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B88h	RCR1	Header Pattern Setting Register (Max)	HDPMAX	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B8Ah	RCR1	Data 0 Pattern Setting Register (Min)	D0PMIN	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B8Bh	RCR1	Data 0 Pattern Setting Register (Max)	D0PMAX	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B8Ch	RCR1	Data 1 Pattern Setting Register (Min)	D1PMIN	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B8Dh	RCR1	Data 1 Pattern Setting Register (Max)	D1PMAX	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B8Eh	RCR1	Special Data Pattern Setting Register (Min)	SDPMIN	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B90h	RCR1	Special Data Pattern Setting Register (Max)	SDPMAX	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B92h	RCR1	Pattern End Setting Register	PE	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.

5.3.2 Reset Timing

Table 5.19 Reset Timing

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2	—	—	ms	Figure 5.7
	Deep software standby mode	t_{RESWD}	1	—	—	ms	Figure 5.8
	Software standby mode, low-speed operating modes 1 and 2	t_{RESWS}	1	—	—	ms	
	Programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	59	—	60	t_{CYC}	Figure 5.7
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	112	—	120	t_{CYC}	

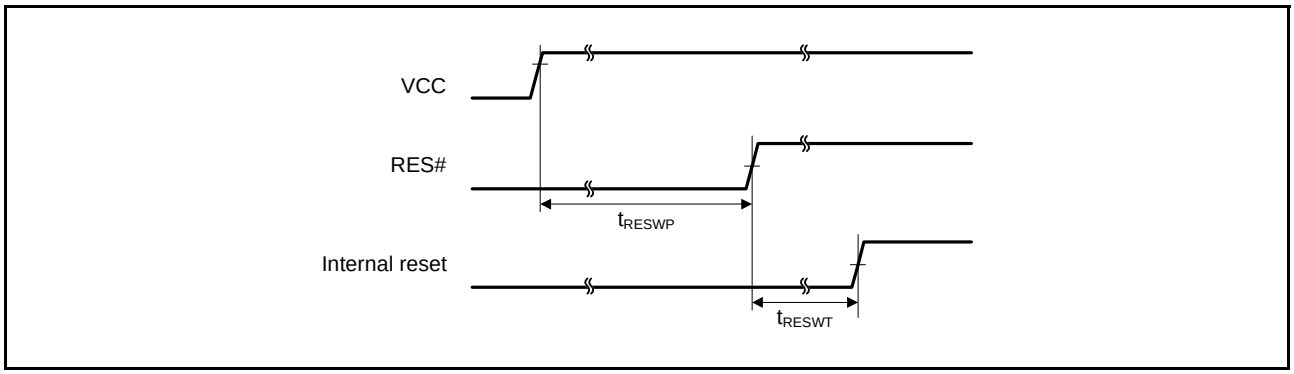


Figure 5.7 Reset Input Timing at Power-On

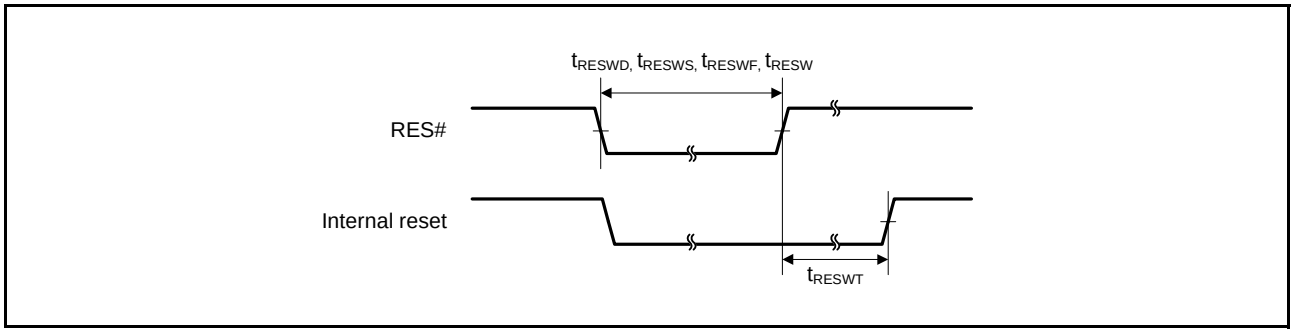


Figure 5.8 Reset Input Timing

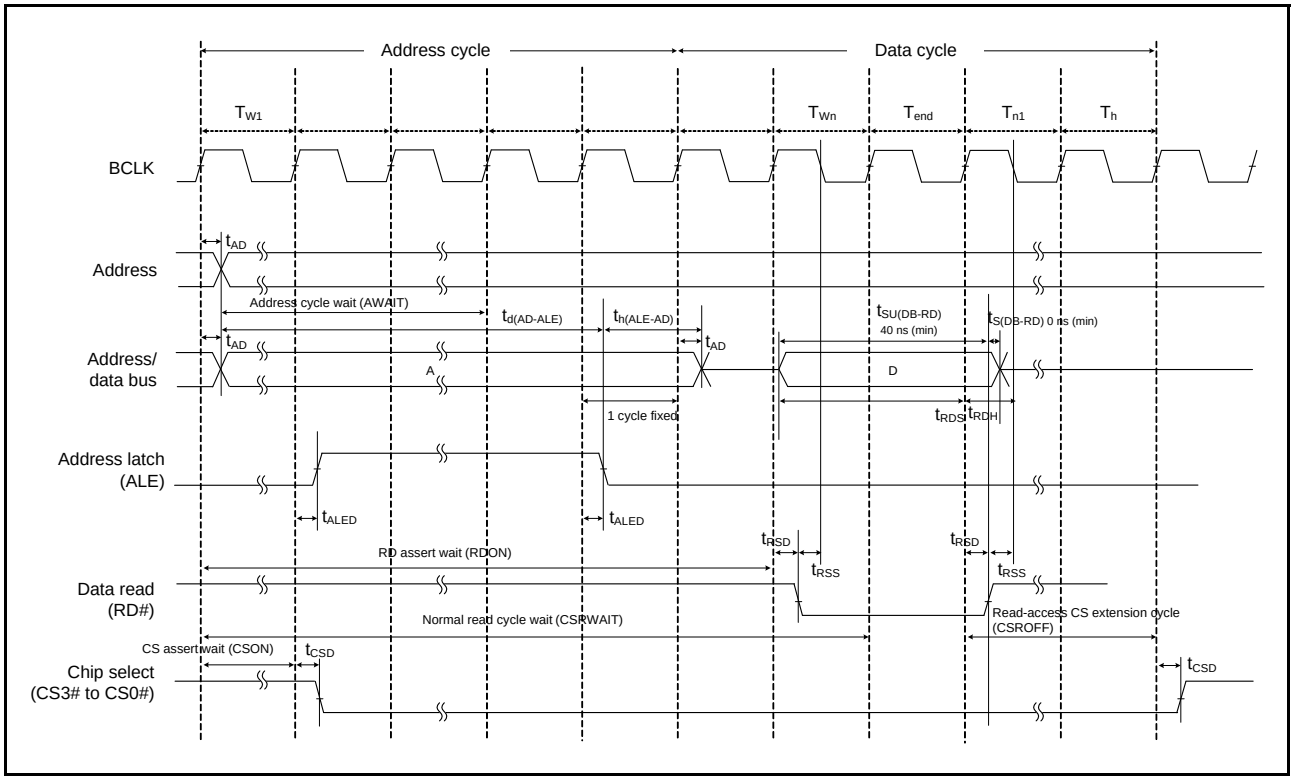


Figure 5.18 Example of Operation in Read Access over the External Bus (Multiplexed)

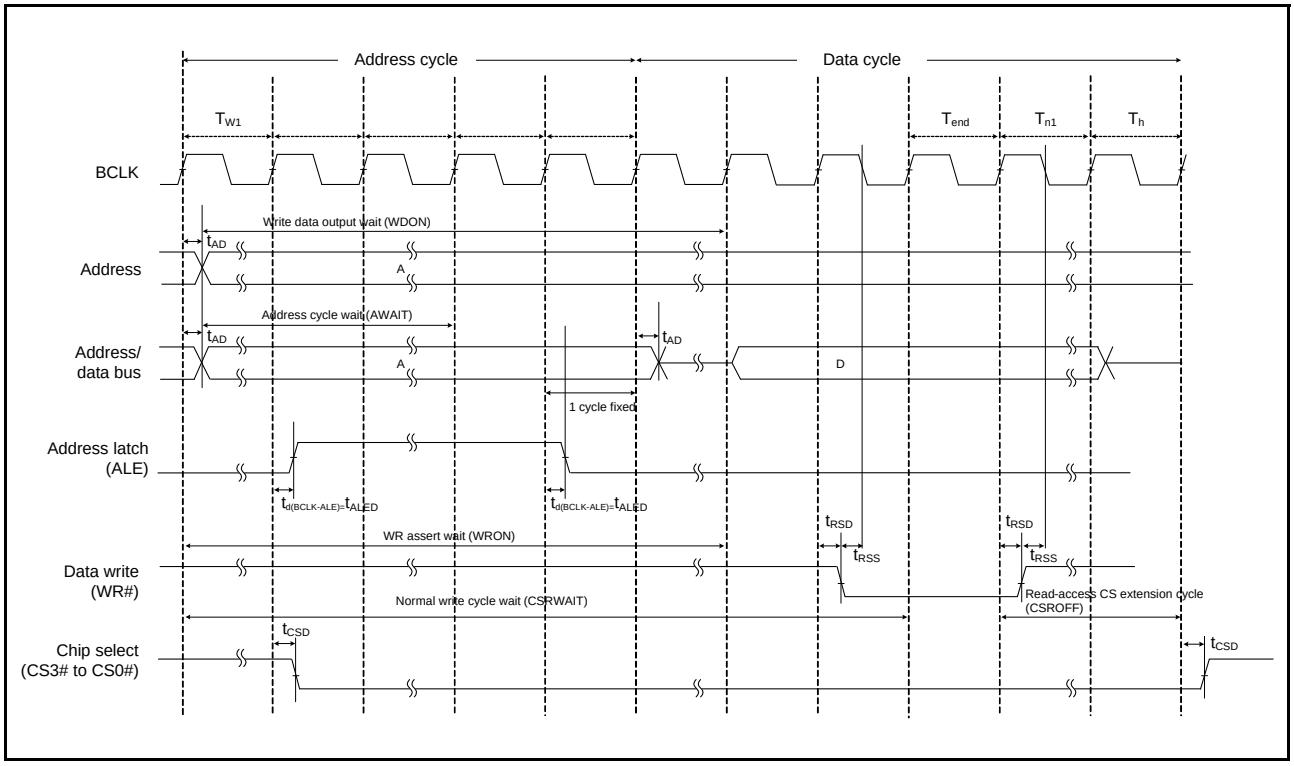


Figure 5.19 Example of Operation in Write Access over the External Bus (Multiplexed)

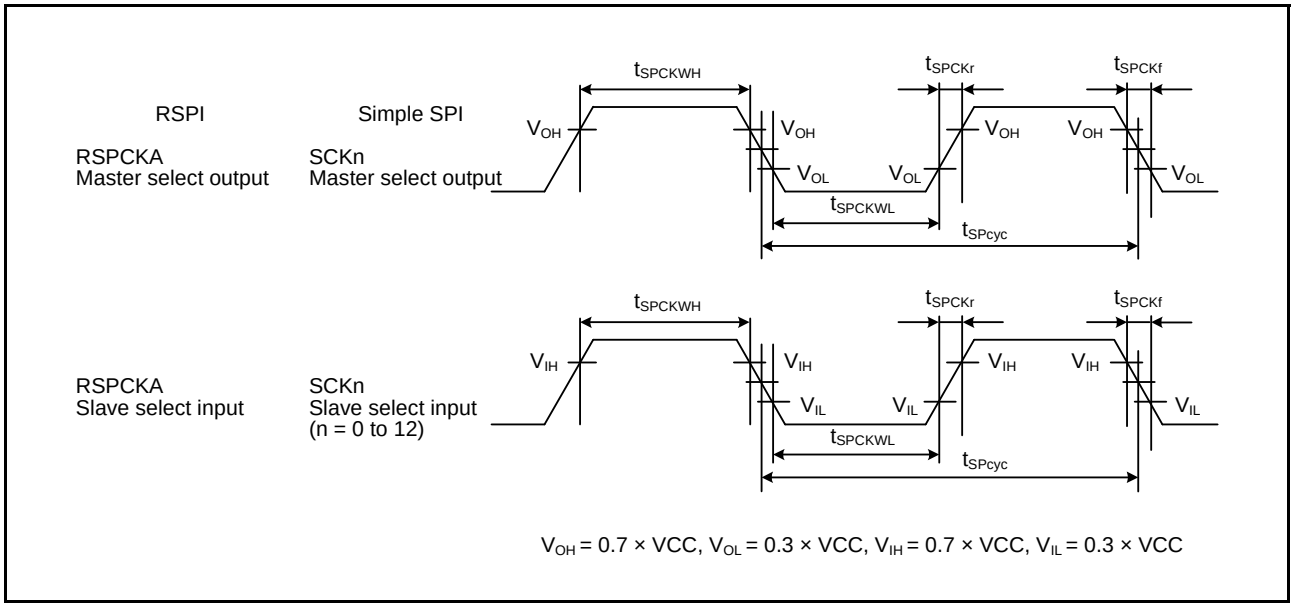


Figure 5.28 RSPI Clock Timing and Simple SPI Clock Timing

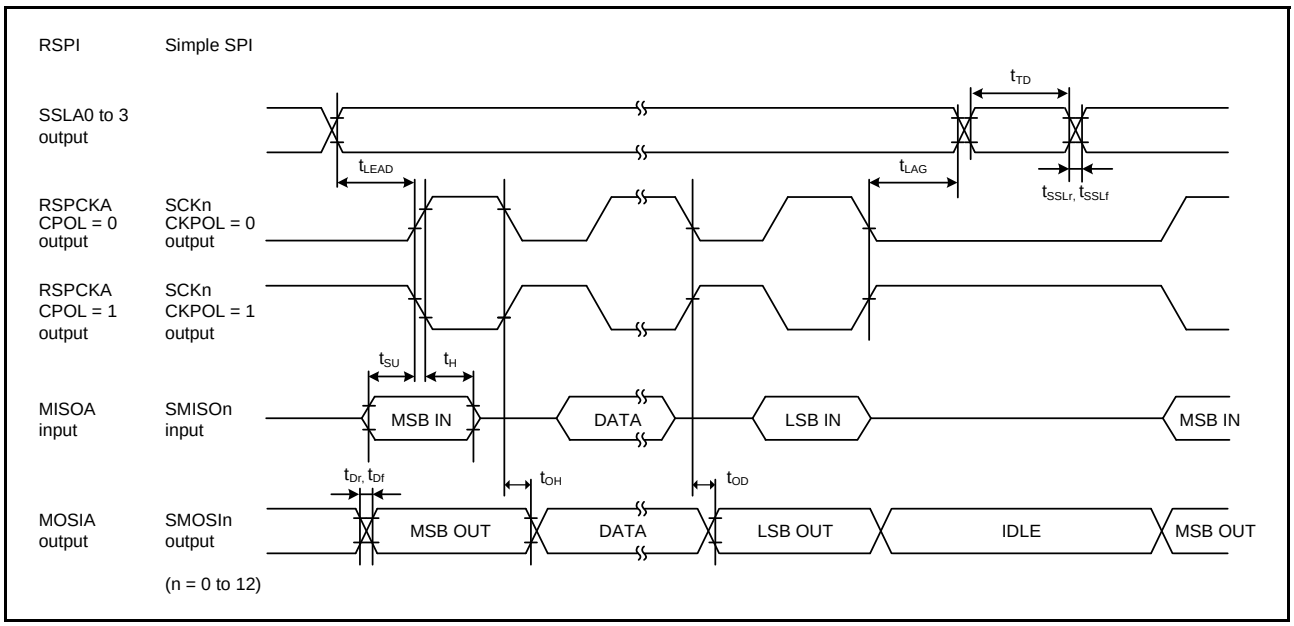


Figure 5.29 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 1)

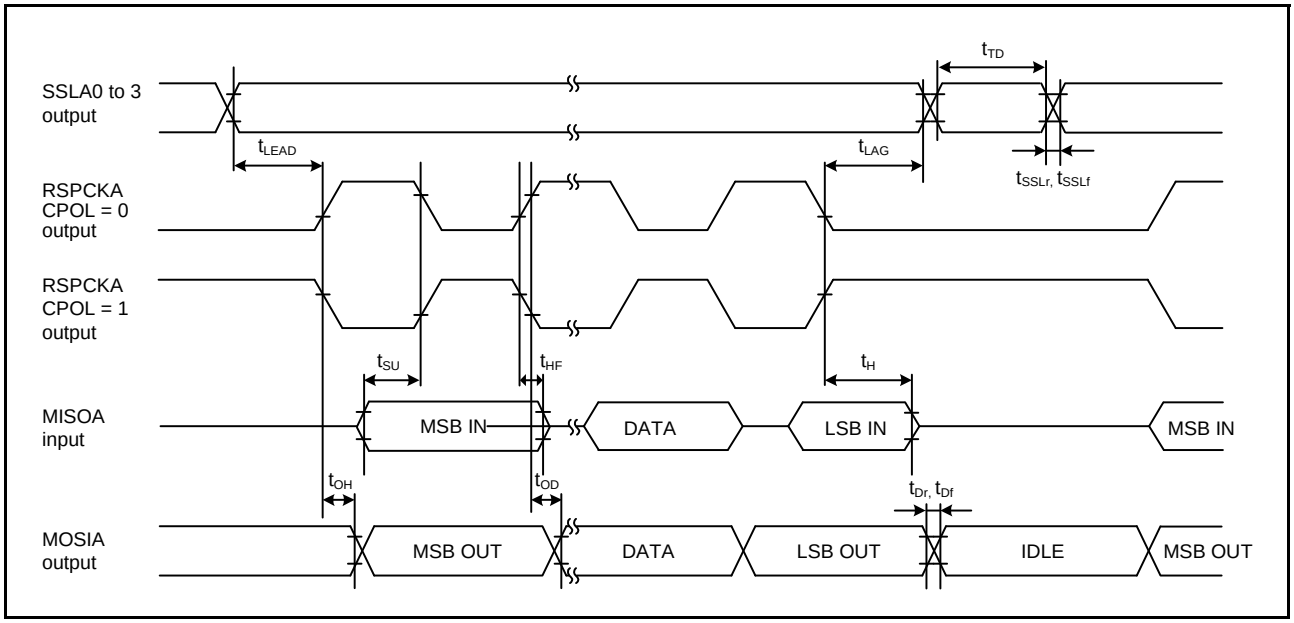


Figure 5.32 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Divided by 2)

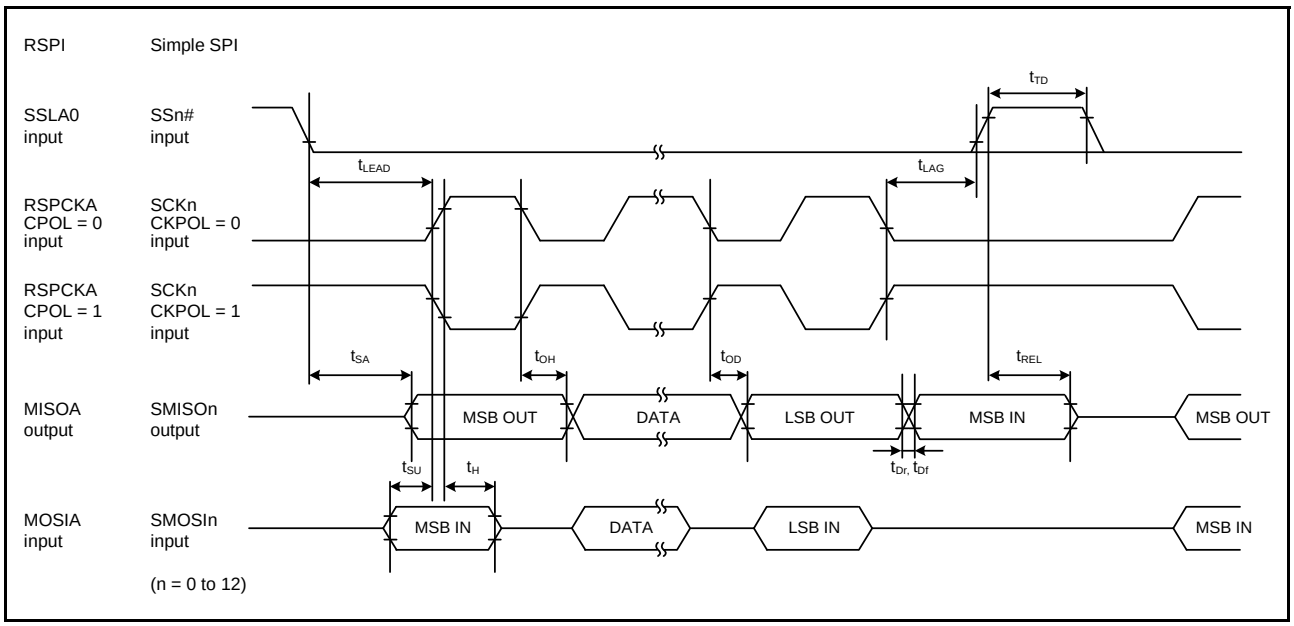


Figure 5.33 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

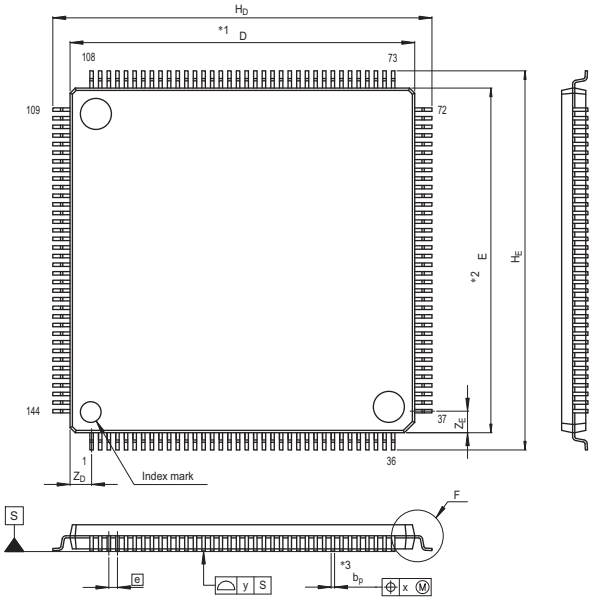
Full-scale error

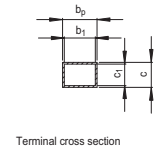
Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

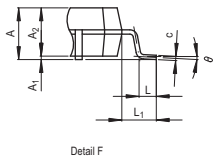
Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 144-Pin LQFP (PLQP0144KA-A)