Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	120
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64185dfd-ub

Table 1.2 Performance Overview for the 144-pin Package (2/2)

Unit	Function	Explanation
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer
Serial Interface	UART0 to UART8	Asynchronous/synchronous serial interface × 9 channels • I^2C-bus (UART0 to UART6) • Special mode 2 (UART0 to UART6) • IEBus (optional (1)) (UART0 to UART6)
A/D Converter		10-bit resolution × 34 channels Sample and hold functionality integrated
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 24 Serial interface: Variable-length synchronous serial I/O mode, IEBus mode (optional (1))
Multi-master I^2C-bus Interface		1 channel
CAN Module		2 channels CAN functionality compliant with ISO 11898-1 32 mailboxes
Flash Memory		Programming and erasure supply voltage: VCC = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
Operating Frequency/Supply Voltage		64 MHz (high speed version)/VCC = 3.0 to 5.5 V 50 MHz (normal speed version)/VCC = 3.0 to 5.5 V
Operating Temperature		-20°C to 85°C (N version) -40°C to 85°C (D version) -40°C to 85°C (P version)
Current Consumption		45 mA (VCC = 5.0 V, f(CPU) = 64 MHz) 35 mA (VCC = 5.0 V, f(CPU) = 50 MHz) 8 µA (VCC = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode)
Package		144-pin plastic molded LQFP (PLQP0144KA-A)

Note:
1. Contact a Renesas Electronics sales office to use the optional features.

Table 1.9 Pin Characteristics for the 144-pin Package (3/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Module Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
75		P4_2			RXD3/SCL3/STXD3	ISRXD2/IEIN		A18
76	VSS							
77		P4_1			CLK3			A17
78		P4_0			$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$			A16
79		P3_7		TA4IN/$\overline{\text{U}}$				A15(/D15)
80		P3_6		TA4OUT/U				A14(/D14)
81		P3_5		TA2IN/$\overline{\text{W}}$				A13(/D13)
82		P3_4		TA2OUT/W				A12(/D12)
83		P3_3		TA1IN/$\overline{\text{V}}$				A11(/D11)
84		P3_2		TA1OUT/V				A10(/D10)
85		P3_1		TA3OUT		UD0B/UD1B		A9(/D9)
86		P12_4						D20
87		P12_3			$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$/$\overline{\text{SS6}}$			D19
88		P12_2			RXD6/SCL6/STXD6			D18
89		P12_1			CLK6			D17
90		P12_0			TXD6/SDA6/SRXD6			D16
91	VCC							
92		P3_0		TA0OUT		UD0A/UD1A		A8(/D8)
93	VSS							
94		P2_7					AN2_7	A7(/D7)
95		P2_6					AN2_6	A6(/D6)
96		P2_5					AN2_5	A5(/D5)
97		P2_4					AN2_4	A4(/D4)
98		P2_3					AN2_3	A3(/D3)
99		P2_2					AN2_2	A2(/D2)
100		P2_1					AN2_1	A1(/D1)/ $\overline{\text{BC2}}$(/D1)
101		P2_0					AN2_0	A0(/D0)/ $\overline{\text{BC0}}$(/D0)
102		P1_7	$\overline{\text{INT5}}$			IIO0_7/IIO1_7		D15
103		P1_6	$\overline{\text{INT4}}$			IIO0_6/IIO1_6		D14
104		P1_5	$\overline{\text{INT3}}$			IIO0_5/IIO1_5		D13
105		P1_4				IIO0_4/IIO1_4		D12
106		P1_3				IIO0_3/IIO1_3		D11
107		P1_2				IIO0_2/IIO1_2		D10
108		P1_1				IIO0_1/IIO1_1		D9
109		P1_0				IIO0_0/IIO1_0		D8
110		P0_7					AN0_7	D7
111		P0_6					AN0_6	D6
112		P0_5					AN0_5	D5
113		P0_4					AN0_4	D4
114		P11_4						$\overline{\text{BC3}}$/$\overline{\text{WR3}}$

Table 1.10 Pin Characteristics for the 144-pin Package (4/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Module Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
115		P11_3			$\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$	IIO1_3		$\overline{\text{CS3}}$/$\overline{\text{WR2}}$
116		P11_2			RXD8	IIO1_2		$\overline{\text{CS2}}$
117		P11_1			CLK8	IIO1_1		$\overline{\text{CS1}}$
118		P11_0			TXD8	IIO1_0		$\overline{\text{CS0}}$
119		P0_3					AN0_3	D3
120		P0_2					AN0_2	D2
121		P0_1					AN0_1	D1
122		P0_0					AN0_0	D0
123		P15_7			$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$/$\overline{\text{SS6}}$	IIO0_7	AN15_7	
124		P15_6			CLK6	IIO0_6	AN15_6	
125		P15_5			RXD6/SCL6/STXD6	IIO0_5	AN15_5	
126		P15_4			TXD6/SDA6/SRXD6	IIO0_4	AN15_4	
127		P15_3			$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$	IIO0_3	AN15_3	
128		P15_2			RXD7	IIO0_2	AN15_2	
129		P15_1			CLK7	IIO0_1	AN15_1	
130	VSS							
131		P15_0			TXD7	IIO0_0	AN15_0	
132	VCC							
133		P10_7	$\overline{\text{KI3}}$				AN_7	
134		P10_6	$\overline{\text{KI2}}$				AN_6	
135		P10_5	$\overline{\text{KI1}}$				AN_5	
136		P10_4	$\overline{\text{KI0}}$				AN_4	
137		P10_3					AN_3	
138		P10_2					AN_2	
139		P10_1					AN_1	
140	AVSS							
141		P10_0					AN_0	
142	VREF							
143	AVCC							
144		P9_7			RXD4/SCL4/STXD4		$\overline{\text{ADTRG}}$	

Table 4.2 SFR List (2)

Address	Register	Symbol	Reset Value
000060h			
000061h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
000062h	UART5 Transmit/NACK Interrupt Control Register	S5TIC	XXXX X000b
000063h	UART2 Receive/ACK Interrupt Control Register/I2C-bus Line Interrupt Control Register	S2RIC/I2CLIC	XXXX X000b
000064h	UART6 Transmit/NACK Interrupt Control Register	S6TIC	XXXX X000b
000065h	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
000066h	UART5/6 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN5IC/BCN6IC	XXXX X000b
000067h	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
000068h	DMA0 Transfer Complete Interrupt Control Register	DM0IC	XXXX X000b
000069h	UART0/3 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
00006Ah	DMA2 Transfer Complete Interrupt Control Register	DM2IC	XXXX X000b
00006Bh	A/D Converter 0 Convert Completion Interrupt Control Register	AD0IC	XXXX X000b
00006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
00006Dh	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000b
00006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
00006Fh	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
000070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
000071h	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
000072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
000073h	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
000074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
000075h	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
000076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
000077h	Intelligent I/O Interrupt Control Register 10	IIO10IC	XXXX X000b
000078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
000079h			
00007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
00007Bh	CAN0 Wake-up Interrupt Control Register	C0WIC	XXXX X000b
00007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
00007Dh			
00007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
00007Fh			
000080h			
000081h	UART2 Transmit/NACK Interrupt Control Register/I2C-bus Interrupt Control Register	S2TIC/I2CIC	XXXX X000b
000082h	UART5 Receive/ACK Interrupt Control Register	S5RIC	XXXX X000b
000083h	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
000084h	UART6 Receive/ACK Interrupt Control Register	S6RIC	XXXX X000b
000085h	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
000086h			
000087h	UART2 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.5 SFR List (5)

Address	Register	Symbol	Reset Value
0000E0h			
0000E1h	CAN0 Receive Interrupt Control Register	C0RIC	XXXX X000b
0000E2h			
0000E3h	CAN1 Transmit Interrupt Control Register	C1TIC	XXXX X000b
0000E4h			
0000E5h	CAN1 Error Interrupt Control Register	C1EIC	XXXX X000b
0000E6h			
0000E7h			
0000E8h			
0000E9h			
0000EAh			
0000EBh			
0000ECh			
0000EDh			
0000EEh			
0000EFh			
0000F0h	CAN0 Receive FIFO Interrupt Control Register	C0FRIC	XXXX X000b
0000F1h			
0000F2h	CAN1 Receive FIFO Interrupt Control Register	C1FRIC	XXXX X000b
0000F3h			
0000F4h			
0000F5h			
0000F6h			
0000F7h			
0000F8h			
0000F9h			
0000FAh			
0000FBh			
0000FCh	INT8 Interrupt Control Register	INT8IC	XX00 X000b
0000FDh	UART7 Receive Interrupt Control Register	S7RIC	XXXX X000b
0000FEh	INT6 Interrupt Control Register	INT6IC	XX00 X000b
0000FFh	UART8 Receive Interrupt Control Register	S8RIC	XXXX X000b
000100h	Group 1 Time Measurement/Waveform Generation Register 0	G1TM0/G1PO0	XXXXh
000101h			
000102h	Group 1 Time Measurement/Waveform Generation Register 1	G1TM1/G1PO1	XXXXh
000103h			
000104h	Group 1 Time Measurement/Waveform Generation Register 2	G1TM2/G1PO2	XXXXh
000105h			
000106h	Group 1 Time Measurement/Waveform Generation Register 3	G1TM3/G1PO3	XXXXh
000107h			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.14 SFR List (14)

Address	Register	Symbol	Reset Value
000350h	Timer B0 Register	TB0	XXXXh
000351h			
000352h	Timer B1 Register	TB1	XXXXh
000353h			
000354h	Timer B2 Register	TB2	XXXXh
000355h			
000356h	Timer A0 Mode Register	TA0MR	0000 0000b
000357h	Timer A1 Mode Register	TA1MR	0000 0000b
000358h	Timer A2 Mode Register	TA2MR	0000 0000b
000359h	Timer A3 Mode Register	TA3MR	0000 0000b
00035Ah	Timer A4 Mode Register	TA4MR	0000 0000b
00035Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
00035Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
00035Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
00035Eh	Timer B2 Special Mode Register	TB2SC	XXXX XXX0b
00035Fh	Count Source Prescaler Register	TCSPR	0000 0000b
000360h			
000361h			
000362h			
000363h			
000364h	UART0 Special Mode Register 4	U0SMR4	00h
000365h	UART0 Special Mode Register 3	U0SMR3	00h
000366h	UART0 Special Mode Register 2	U0SMR2	00h
000367h	UART0 Special Mode Register	U0SMR	00h
000368h	UART0 Transmit/Receive Mode Register	U0MR	00h
000369h	UART0 Bit Rate Register	U0BRG	XXh
00036Ah	UART0 Transmit Buffer Register	U0TB	XXXXh
00036Bh			
00036Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
00036Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
00036Eh	UART0 Receive Buffer Register	U0RB	XXXXh
00036Fh			
000370h			
000371h			
000372h			
000373h			
000374h			
000375h			
000376h			
000377h			
000378h			
000379h			
00037Ah			
00037Bh			
00037Ch	CRC Data Register	CRCD	XXXXh
00037Dh			
00037Eh	CRC Input Register	CRCIN	XXh
00037Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.26 SFR List (26)

Address	Register	Symbol	Reset Value
046800h to 0477FFh			
047800h	CAN1 Mailbox 0: Message Identifier	C1MB0	XXXX XXXXh
047801h			
047802h			
047803h			
047804h			
047805h	CAN1 Mailbox 0: Data Length		XXh
047806h	CAN1 Mailbox 0: Data Field		XXXX XXXX
047807h			XXXX XXXXh
047808h			
047809h			
04780Ah			
04780Bh			
04780Ch			
04780Dh			
04780Eh	CAN1 Mailbox 0: Time Stamp		XXXXh
04780Fh			
047810h	CAN1 Mailbox 1: Message Identifier	C1MB1	XXXX XXXXh
047811h			
047812h			
047813h			
047814h			
047815h	CAN1 Mailbox 1: Data Length		XXh
047816h	CAN1 Mailbox 1: Data Field		XXXX XXXX
047817h			XXXX XXXXh
047818h			
047819h			
04781Ah			
04781Bh			
04781Ch			
04781Dh			
04781Eh	CAN1 Mailbox 1: Time Stamp		XXXXh
04781Fh			
047820h	CAN1 Mailbox 2: Message Identifier	C1MB2	XXXX XXXXh
047821h			
047822h			
047823h			
047824h			
047825h	CAN1 Mailbox 2: Data Length		XXh
047826h	CAN1 Mailbox 2: Data Field		XXXX XXXX
047827h			XXXX XXXXh
047828h			
047829h			
04782Ah			
04782Bh			
04782Ch			
04782Dh			
04782Eh	CAN1 Mailbox 2: Time Stamp		XXXXh
04782Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.27 SFR List (27)

Address	Register	Symbol	Reset Value
047830h	CAN1 Mailbox 3: Message Identifier	C1MB3	XXXX XXXXh
047831h			
047832h			
047833h			
047834h			
047835h	CAN1 Mailbox 3: Data Length		XXh
047836h	CAN1 Mailbox 3: Data Field		XXXX XXXX
047837h			XXXX XXXXh
047838h			
047839h			
04783Ah			
04783Bh			
04783Ch			
04783Dh			
04783Eh	CAN1 Mailbox 3: Time Stamp		XXXXh
04783Fh			
047840h	CAN1 Mailbox 4: Message Identifier	C1MB4	XXXX XXXXh
047841h			
047842h			
047843h			
047844h			
047845h	CAN1 Mailbox 4: Data Length		XXh
047846h	CAN1 Mailbox 4: Data Field		XXXX XXXX
047847h			XXXX XXXXh
047848h			
047849h			
04784Ah			
04784Bh			
04784Ch			
04784Dh			
04784Eh	CAN1 Mailbox 4: Time Stamp		XXXXh
04784Fh			
047850h	CAN1 Mailbox 5: Message Identifier	C1MB5	XXXX XXXXh
047851h			
047852h			
047853h			
047854h			
047855h	CAN1 Mailbox 5: Data Length		XXh
047856h	CAN1 Mailbox 5: Data Field		XXXX XXXX
047857h			XXXX XXXXh
047858h			
047859h			
04785Ah			
04785Bh			
04785Ch			
04785Dh			
04785Eh	CAN1 Mailbox 5: Time Stamp		XXXXh
04785Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.31 SFR List (31)

Address	Register	Symbol	Reset Value
0478F0h	CAN1 Mailbox 15: Message Identifier	C1MB15	XXXX XXXXh
0478F1h			
0478F2h			
0478F3h			
0478F4h			
0478F5h	CAN1 Mailbox 15: Data Length		XXh
0478F6h	CAN1 Mailbox 15: Data Field		XXXX XXXX
0478F7h			XXXX XXXXh
0478F8h			
0478F9h			
0478FAh			
0478FBh			
0478FCh			
0478FDh			
0478FEh	CAN1 Mailbox 15: Time Stamp		XXXXh
0478FFh			
047900h	CAN1 Mailbox 16: Message Identifier	C1MB16	XXXX XXXXh
047901h			
047902h			
047903h			
047904h			
047905h	CAN1 Mailbox 16: Data Length		XXh
047906h	CAN1 Mailbox 16: Data Field		XXXX XXXX
047907h			XXXX XXXXh
047908h			
047909h			
04790Ah			
04790Bh			
04790Ch			
04790Dh			
04790Eh	CAN1 Mailbox 16: Time Stamp		XXXXh
04790Fh			
047910h	CAN1 Mailbox 17: Message Identifier	C1MB17	XXXX XXXXh
047911h			
047912h			
047913h			
047914h			
047915h	CAN1 Mailbox 17: Data Length		XXh
047916h	CAN1 Mailbox 17: Data Field		XXXX XXXX
047917h			XXXX XXXXh
047918h			
047919h			
04791Ah			
04791Bh			
04791Ch			
04791Dh			
04791Eh	CAN1 Mailbox 17: Time Stamp		XXXXh
04791Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 5.2 Operating Conditions (1/5) (1)

Symbol	Characteristic			Value			Unit
				Min.	Typ.	Max.	
V_{CC}	Digital supply voltage			3.0	5.0	5.5	V
AV_{CC}	Analog supply voltage				V_{CC}		V
V_{REF}	Reference voltage			3.0		V_{CC}	V
V_{SS}	Digital ground voltage				0		V
AV_{SS}	Analog ground voltage				0		V
dV_{CC}/dt	V_{CC} ramp up rate (V_{CC} < 2.0 V)			0.05			V/ms
V_{IH}	High level input voltage	XIN, $\overline{\text{RESET}}$, CNVSS, NSD, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P14_1, P14_3 to P14_6, P15_0 to P15_7 (3)		0.8 × V_{CC}		V_{CC}	V
		P4_0 to P4_7, P5_4 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_3		0.8 × V_{CC}		6.0	V
		P0_0 to P0_7, P1_0 to P1_7, P12_0 to P12_7, P13_0 to P13_7 (3)	in single-chip mode	0.8 × V_{CC}		V_{CC}	V
			in memory expansion mode or microprocessor mode	0.5 × V_{CC}		V_{CC}	V
V_{IL}	Low level input voltage	XIN, $\overline{\text{RESET}}$, CNVSS, NSD, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P14_1, P14_3 to P14_6, P15_0 to P15_7 (3)		0		0.2 × V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P12_0 to P12_7, P13_0 to P13_7 (3)	in single-chip mode	0		0.2 × V_{CC}	V
			in memory expansion mode or microprocessor mode	0		0.16 × V_{CC}	V
T_{opr}	Operating temperature range	N version		-20		85	°C
		D version		-40		85	°C
		P version		-40		85	°C

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. V_{IH} and V_{IL} for P8_7 are specified for P8_7 as a programmable port. These values are not applicable for P8_7 as XCIN.
3. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

V_{CC} = 5 V

Table 5.17 Electrical Characteristics (3/3)
(V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current	In single-chip mode, output pins are left open and others are connected to V_{SS} XIN-XOUT Drive strength: low XCIN-XCOUT Drive strength: low	$f_{(CPU)}$ = 64 MHz, $f_{(BCLK)}$ = 32 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, PLL, Stopped: XCIN, OCO		45	60	mA
			$f_{(CPU)}$ = 50 MHz, $f_{(BCLK)}$ = 25 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, PLL, Stopped: XCIN, OCO		35	50	mA
			$f_{(CPU)}$ = $f_{SO(PLL)}$/24 MHz, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO		12		mA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO		1.2		mA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown		220		µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown		230		µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO, T_a = 25°C, Wait mode		960	1600	µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, T_a = 25°C, Wait mode		8	140	µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, T_a = 25°C, Wait mode		10	150	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 25°C		5	70	µA

V_{CC} = 5 V

Table 5.19 D/A Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute precision				1.0	%
t_S	Settling time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference input current	See Note 1			1.5	mA

Note:
1. One D/A converter is used. The DAi register (i = 0, 1) of the other unused converter is set to 00h. The resistor ladder for the A/D converter is not considered.
Even when the VCUT bit in the AD0CON1 register is set to 0 (V_{REF} disconnected), I_{VREF} is supplied.

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.20 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(X)}$	External clock input period	62.5	250	ns
$t_{w(XH)}$	External clock input high level pulse width	25		ns
$t_{w(XL)}$	External clock input low level pulse width	25		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_w / t_c	External clock input duty	40	60	%

Table 5.21 External Bus Timing

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{su(D-R)}$	Data setup time before read	40		ns
$t_{h(R-D)}$	Data hold time after read	0		ns
$t_{dis(R-D)}$	Data disable time after read		0.5 × $t_{c(Base)}$ + 10	ns

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.22 Timer A Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.23 Timer A Input (gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.24 Timer A Input (external trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.25 Timer A Input (external trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.26 Timer A Input (increment/decrement switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.27 Timer B Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time (one edge counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{c(TB)}$	TBiIN input clock cycle time (both edges counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.28 Timer B Input (pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.29 Timer B Input (pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

V_{CC} = 3.3 V

Table 5.44 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 3.0 to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_a = T_{opr}, and $f_{(BCLK)}$ = 32 MHz, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}				10	Bits
—	Absolute error	V_{REF} = V_{CC} = 3.3 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 (1)			±5	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	V_{REF} = V_{CC} = 3.3 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 (1)			±5	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error	V_{REF} = V_{CC} = 3.3 V				±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	V_{REF} = V_{CC}		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		3.3			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		2.8			µs
t_{SAMP}	Sampling time	ϕ_{AD} = 10 MHz		0.3			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function		0.25		10	MHz
		With sample and hold function		1		10	MHz

Note:
1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.

V_{CC} = 3.3 V

Timing Requirements (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.56 Serial Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input clock cycle time	200		ns
$t_{w(CKH)}$	CLKi input high level pulse width	80		ns
$t_{w(CKL)}$	CLKi input low level pulse width	80		ns
$t_{su(D-C)}$	RXDi input setup time	80		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.57 A/D Trigger Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(ADH)}$	$\overline{ADTRG}$ input high level pulse width Hardware trigger input high level pulse width	$\frac{3}{\phi_{AD}}$		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input low level pulse width Hardware trigger input high level pulse width	125		ns

Table 5.58 External Interrupt $\overline{INTi}$ Input

Symbol	Characteristic		Value		Unit
			Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{c(CPU)}$ + 200		ns
$t_{w(INL)}$	$\overline{INTi}$ input low level pulse width	Edge sensitive	250		ns
		Level sensitive	$t_{c(CPU)}$ + 200		ns

Table 5.59 Intelligent I/O

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(ISCLK2)}$	ISCLK2 input clock cycle time	600		ns
$t_{w(ISCLK2H)}$	ISCLK2 input high level pulse width	270		ns
$t_{w(ISCLK2L)}$	ISCLK2 input low level pulse width	270		ns
$t_{su(RXD-ISCLK2)}$	ISRXD2 input setup time	150		ns
$t_{h(ISCLK2-RXD)}$	ISRXD2 input hold time	100		ns

V_{CC} = 3.3 V

Switching Characteristics (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.62 External Bus Timing (multiplexed bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-ALE)}$	Chip-select setup time before ALE	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		1.5 × $t_{c(Base)}$ - 15		ns
$t_{su(A-ALE)}$	Address setup time before ALE		(1)		ns
$t_{h(ALE-A)}$	Address hold time after ALE		0.5 × $t_{c(Base)}$ - 5		ns
$t_{h(R-A)}$	Address hold time after read		1.5 × $t_{c(Base)}$ - 15		ns
$t_{d(ALE-R)}$	ALE-read delay time		0.5 × $t_{c(Base)}$ - 5	0.5 × $t_{c(Base)}$ + 10	ns
$t_{w(ALE)}$	ALE pulse width		(1)		ns
$t_{dis(R-A)}$	Address disable time after read			8	ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		1.5 × $t_{c(Base)}$ - 15		ns
$t_{h(W-A)}$	Address hold time after write		1.5 × $t_{c(Base)}$ - 15		ns
$t_{d(ALE-W)}$	ALE-write delay time		0.5 × $t_{c(Base)}$ - 5	0.5 × $t_{c(Base)}$ + 10	ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		0.5 × $t_{c(Base)}$		ns

Note:

1. The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of Tsu(A-R), Tw(R), Tsu(A-W), and Tw(W) set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

   $t_{su(S-ALE)}$ = $t_{su(A-ALE)}$ = (Tsu(A-R) - 0.5) × $t_{c(Base)}$ -15 [ns]

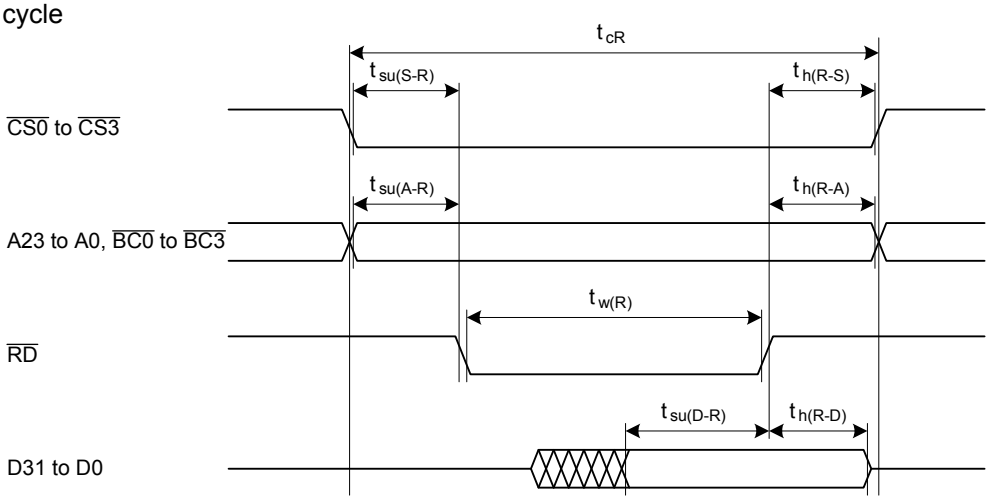
   $t_{w(ALE)}$ = (Tsu(A-R) - 0.5) × $t_{c(Base)}$ - 20 [ns]

   $t_{w(R)}$ = Tw(R) × $t_{c(Base)}$ -10 [ns]

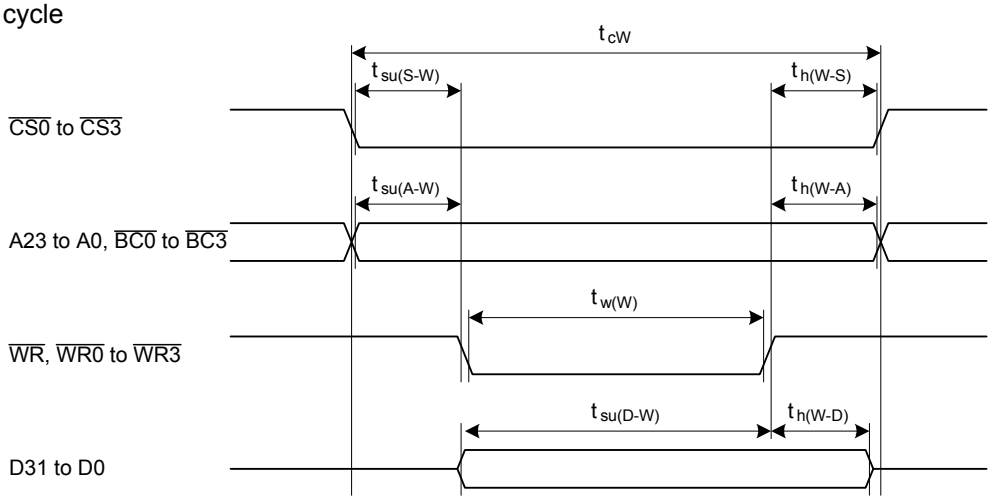
   $t_{w(W)}$ = $t_{su(D-W)}$ = Tw(W) × $t_{c(Base)}$ -10 [ns]

External bus timing (separate bus)

Read cycle



Write cycle



Measurement conditions

Item		V_{CC} = 4.2 to 5.5 V	V_{CC} = 3.0 to 3.6 V
Criterion for input voltage	V_{IH}	2.5 V	1.5 V
	V_{IL}	0.8 V	0.5 V
Criterion for output voltage	V_{OH}	2.0 V	2.4 V
	V_{OL}	0.8 V	0.5 V

Figure 5.8 External Bus Timing for Separate Bus

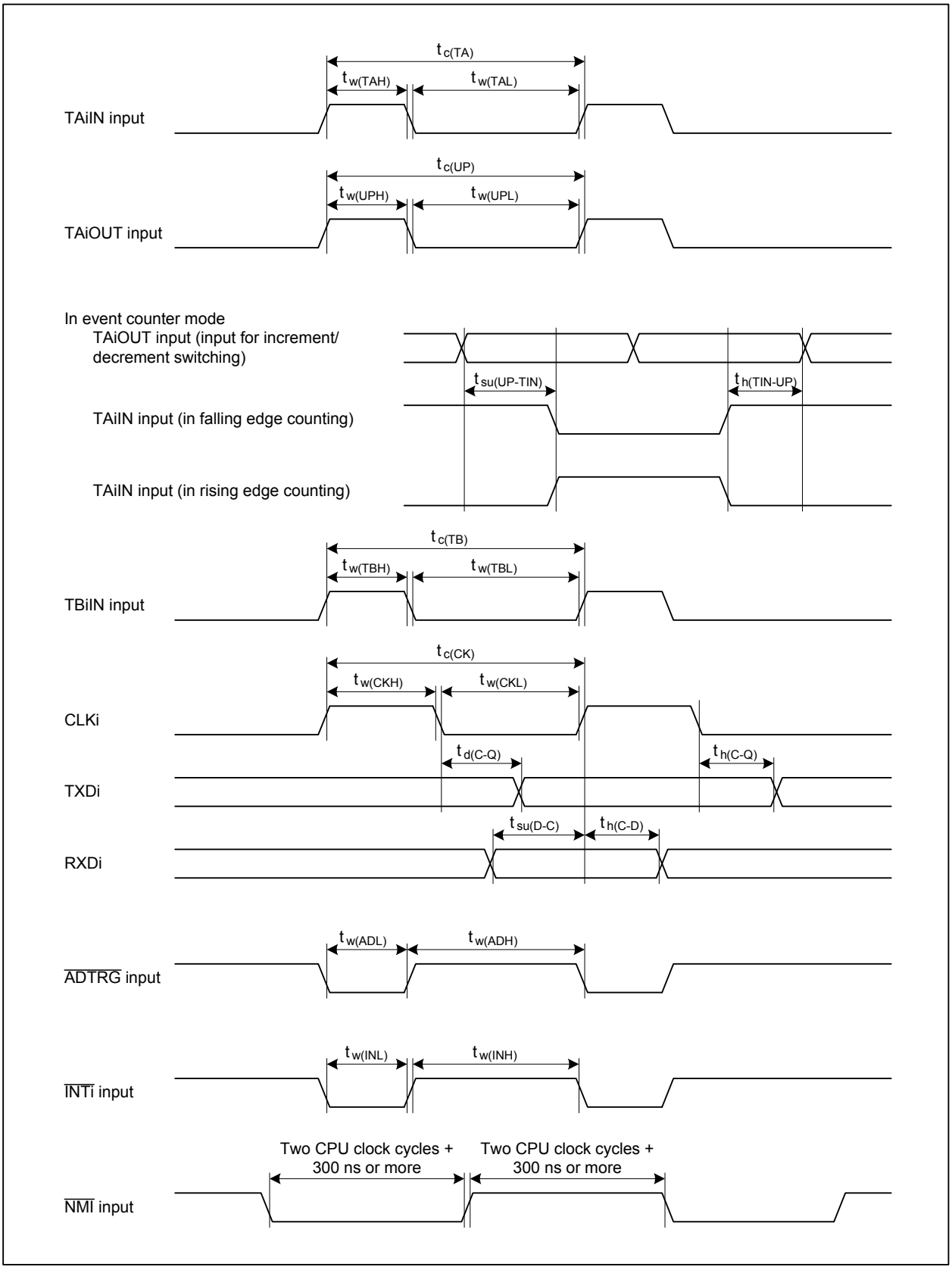


Figure 5.10 Timing of Peripherals