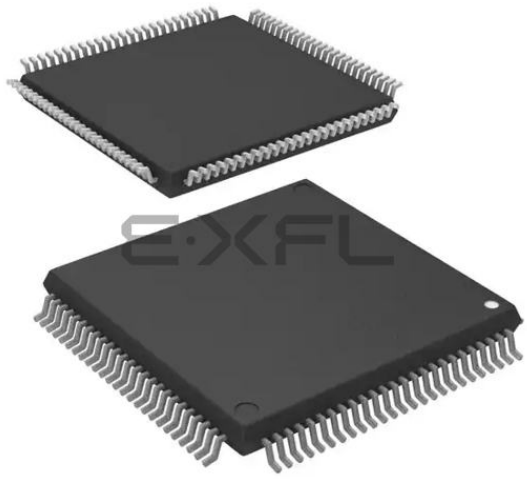
Renesas Electronics America Inc - R5F64186DFB#U0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64186dfb-u0

1.2 Product Information

Tables 1.5 and 1.6 list the product information and Figure 1.1 shows the details of the part number.

Table 1.5 R32C/118 Group Product List for Normal Speed Version (1/2) As of February, 2013

Part Number	Package Code (1)	ROM Capacity (2)	RAM Capacity	Remarks
R5F64185NFD (P)	PLQP0144KA-A	384 Kbytes + 8 Kbytes	40 Kbytes	-20°C to 85°C (N version)
R5F64185DFD				-40°C to 85°C (D version)
R5F64185PFD				-40°C to 85°C (P version)
R5F64185NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64185DFB				-40°C to 85°C (D version)
R5F64185PFB				-40°C to 85°C (P version)
R5F64186NFD (P)	PLQP0144KA-A	512 Kbytes + 8 Kbytes		-20°C to 85°C (N version)
R5F64186DFD				-40°C to 85°C (D version)
R5F64186PFD				-40°C to 85°C (P version)
R5F64186NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64186DFB				-40°C to 85°C (D version)
R5F64186PFB				-40°C to 85°C (P version)
R5F64187NFD (P)	PLQP0144KA-A	640 Kbytes + 8 Kbytes	48 Kbytes	-20°C to 85°C (N version)
R5F64187DFD				-40°C to 85°C (D version)
R5F64187PFD				-40°C to 85°C (P version)
R5F64187NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64187DFB				-40°C to 85°C (D version)
R5F64187PFB				-40°C to 85°C (P version)
R5F64188NFD (P)	PLQP0144KA-A	768 Kbytes + 8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64188DFD				-40°C to 85°C (D version)
R5F64188PFD				-40°C to 85°C (P version)
R5F64188NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64188DFB				-40°C to 85°C (D version)
R5F64188PFB				-40°C to 85°C (P version)
R5F64189NFD (P)	PLQP0144KA-A	1 Mbyte + 8 Kbytes		-20°C to 85°C (N version)
R5F64189DFD				-40°C to 85°C (D version)
R5F64189PFD				-40°C to 85°C (P version)
R5F64189NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64189DFB				-40°C to 85°C (D version)
R5F64189PFB				-40°C to 85°C (P version)

(P): On planning phase

Notes:
1. The old package codes are as follows:
   PLQP0100KB-A: 100P6Q-A; PLQP0144KA-A: 144P6Q-A
2. “8 Kbytes” in the ROM capacity indicates the data flash memory capacity.

1.5 Pin Definitions and Functions

Tables 1.14 to 1.18 list the pin definitions and functions.

Table 1.14 Pin Definitions and Functions (1/4)

Function	Symbol	I/O	Description
Power supply	VCC, VSS	I	Applicable as follows: VCC = 3.0 to 5.5 V, VSS = 0 V
Connecting pins for decoupling capacitor	VDC0, VDC1	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC and VSS, respectively
Reset input	$\overline{\text{RESET}}$	I	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	This pin is to communicate with a debugger. It should be connected to VCC via a resistor of 1 to 4.7 kΩ
Main clock input	XIN	I	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOUT. An external clock should be input at the XCIN while leaving the XCOUT open
Sub clock output	XCOUT	O	
BCLK output	BCLK	O	BCLK output
Clock output	CLKOUT	O	Output of the clock with the same frequency as low speed clocks, f8, or f32
External interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT8}}$ (1)	I	Input for external interrupts
NMI input	P8_5/$\overline{\text{NMI}}$	I	Input for NMI
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input for the key input interrupt
Bus control pins	D0 to D7	I/O	Input/output of data (D0 to D7) while accessing an external memory space with a separate bus
	D8 to D15	I/O	Input/output of data (D8 to D15) while accessing an external memory space with 16-bit or 32-bit separate bus
	D16 to D31 (2)	I/O	Input/output of data (D16 to D31) while accessing an external memory space with 32-bit separate bus
	A0 to A23	O	Output of address bits A0 to A23
	A0/D0 to A7/D7	I/O	Output of address bits (A0 to A7) and input/output of data (D0 to D7) by time-division while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	Output of address bits (A8 to A15) and input/output of data (D8 to D15) by time-division while accessing an external memory space with 16-bit or 32-bit multiplexed bus

Notes:
1. Pins $\overline{\text{INT6}}$ to $\overline{\text{INT8}}$ are available in the 144-pin package only.
2. Pins D16 to D31 are available in the 144-pin package only.

2. Central Processing Unit (CPU)

The CPU contains the registers shown below. There are two register banks each consisting of registers R2R0, R3R1, R6R4, R7R5, A0 to A3, SB, and FB.

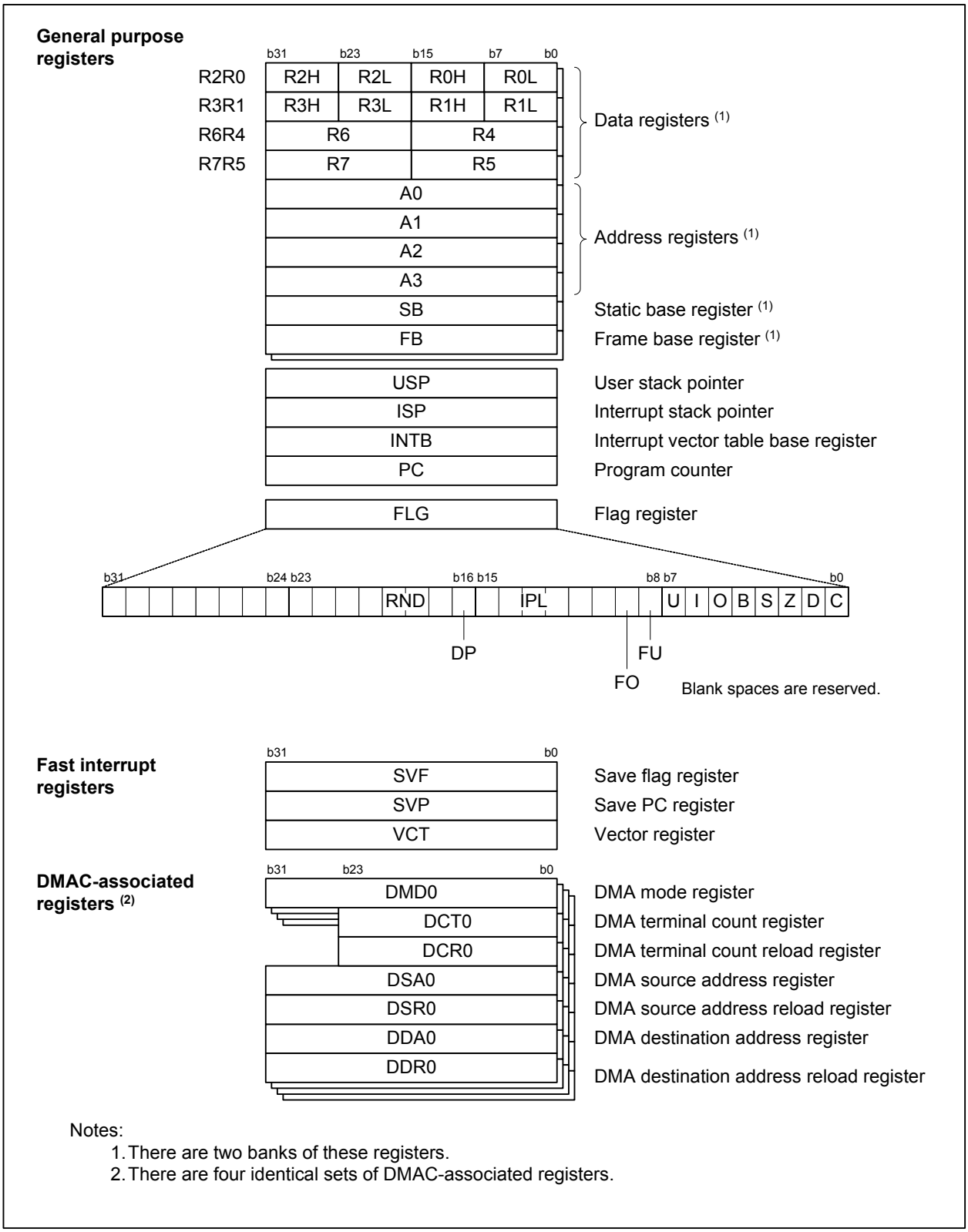


Figure 2.1 CPU Registers

Table 4.19 SFR List (19)

Address	Register	Symbol	Reset Value
040030h to 04003Fh			
040040h			
040041h			
040042h			
040043h			
040044h	Processor Mode Register 0 (1)	PM0	1000 0000b (CNVSS pin = Low) 0000 0011b (CNVSS pin = High)
040045h			
040046h	System Clock Control Register 0	CM0	0000 1000b
040047h	System Clock Control Register 1	CM1	0010 0000b
040048h	Processor Mode Register 3	PM3	00h
040049h			
04004Ah	Protect Register	PRCR	XXXX X000b
04004Bh			
04004Ch	Protect Register 3	PRCR3	0000 0000b
04004Dh	Oscillator Stop Detection Register	CM2	00h
04004Eh			
04004Fh			
040050h			
040051h			
040052h			
040053h	Processor Mode Register 2	PM2	00h
040054h	Chip Select Output Pin Setting Register 0	CSOP0	1000 XXXXb
040055h	Chip Select Output Pin Setting Register 1	CSOP1	01X0 XXXXb
040056h	Chip Select Output Pin Setting Register 2	CSOP2	XXXX 0000b
040057h			
040058h			
040059h			
04005Ah	Low Speed Mode Clock Control Register	CM3	XXXX XX00b
04005Bh			
04005Ch			
04005Dh			
04005Eh			
04005Fh			
040060h	Voltage Regulator Control Register	VRCR	0000 0000b
040061h			
040062h	Low Voltage Detector Control Register	LVDC	0000 XX00b
040063h			
040064h	Detection Voltage Configuration Register	DVCR	0000 XXXXb
040065h			
040066h			
040067h			
040068h to 040093h			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. The value in the PM0 register is retained even after a software reset or watchdog timer reset.

Table 4.20 SFR List (20)

Address	Register	Symbol	Reset Value
040094h			
040095h			
040096h			
040097h	Three-phase Output Buffer Control Register	IOBC	0XXX XXXXb
040098h	Input Function Select Register 0	IFS0	X000 0000b
040099h	Input Function Select Register 1	IFS1	XXXX X0X0b
04009Ah	Input Function Select Register 2	IFS2	0000 00X0b
04009Bh	Input Function Select Register 3	IFS3	XXXX XX00b
04009Ch			
04009Dh			
04009Eh			
04009Fh			
0400A0h	Port P0_0 Function Select Register	P0_0S	0XXX X000b
0400A1h	Port P1_0 Function Select Register	P1_0S	XXXX X000b
0400A2h	Port P0_1 Function Select Register	P0_1S	0XXX X000b
0400A3h	Port P1_1 Function Select Register	P1_1S	XXXX X000b
0400A4h	Port P0_2 Function Select Register	P0_2S	0XXX X000b
0400A5h	Port P1_2 Function Select Register	P1_2S	XXXX X000b
0400A6h	Port P0_3 Function Select Register	P0_3S	0XXX X000b
0400A7h	Port P1_3 Function Select Register	P1_3S	XXXX X000b
0400A8h	Port P0_4 Function Select Register	P0_4S	0XXX X000b
0400A9h	Port P1_4 Function Select Register	P1_4S	XXXX X000b
0400AAh	Port P0_5 Function Select Register	P0_5S	0XXX X000b
0400ABh	Port P1_5 Function Select Register	P1_5S	XXXX X000b
0400ACh	Port P0_6 Function Select Register	P0_6S	0XXX X000b
0400ADh	Port P1_6 Function Select Register	P1_6S	XXXX X000b
0400AEh	Port P0_7 Function Select Register	P0_7S	0XXX X000b
0400AFh	Port P1_7 Function Select Register	P1_7S	XXXX X000b
0400B0h	Port P2_0 Function Select Register	P2_0S	0XXX X000b
0400B1h	Port P3_0 Function Select Register	P3_0S	XXXX X000b
0400B2h	Port P2_1 Function Select Register	P2_1S	0XXX X000b
0400B3h	Port P3_1 Function Select Register	P3_1S	XXXX X000b
0400B4h	Port P2_2 Function Select Register	P2_2S	0XXX X000b
0400B5h	Port P3_2 Function Select Register	P3_2S	XXXX X000b
0400B6h	Port P2_3 Function Select Register	P2_3S	0XXX X000b
0400B7h	Port P3_3 Function Select Register	P3_3S	XXXX X000b
0400B8h	Port P2_4 Function Select Register	P2_4S	0XXX X000b
0400B9h	Port P3_4 Function Select Register	P3_4S	XXXX X000b
0400BAh	Port P2_5 Function Select Register	P2_5S	0XXX X000b
0400BBh	Port P3_5 Function Select Register	P3_5S	XXXX X000b
0400BCh	Port P2_6 Function Select Register	P2_6S	0XXX X000b
0400BDh	Port P3_6 Function Select Register	P3_6S	XXXX X000b
0400BEh	Port P2_7 Function Select Register	P2_7S	0XXX X000b
0400BFh	Port P3_7 Function Select Register	P3_7S	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.27 SFR List (27)

Address	Register	Symbol	Reset Value
047830h	CAN1 Mailbox 3: Message Identifier	C1MB3	XXXX XXXXh
047831h			
047832h			
047833h			
047834h			
047835h	CAN1 Mailbox 3: Data Length		XXh
047836h	CAN1 Mailbox 3: Data Field		XXXX XXXX
047837h			XXXX XXXXh
047838h			
047839h			
04783Ah			
04783Bh			
04783Ch			
04783Dh			
04783Eh	CAN1 Mailbox 3: Time Stamp		XXXXh
04783Fh			
047840h	CAN1 Mailbox 4: Message Identifier	C1MB4	XXXX XXXXh
047841h			
047842h			
047843h			
047844h			
047845h	CAN1 Mailbox 4: Data Length		XXh
047846h	CAN1 Mailbox 4: Data Field		XXXX XXXX
047847h			XXXX XXXXh
047848h			
047849h			
04784Ah			
04784Bh			
04784Ch			
04784Dh			
04784Eh	CAN1 Mailbox 4: Time Stamp		XXXXh
04784Fh			
047850h	CAN1 Mailbox 5: Message Identifier	C1MB5	XXXX XXXXh
047851h			
047852h			
047853h			
047854h			
047855h	CAN1 Mailbox 5: Data Length		XXh
047856h	CAN1 Mailbox 5: Data Field		XXXX XXXX
047857h			XXXX XXXXh
047858h			
047859h			
04785Ah			
04785Bh			
04785Ch			
04785Dh			
04785Eh	CAN1 Mailbox 5: Time Stamp		XXXXh
04785Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.28 SFR List (28)

Address	Register	Symbol	Reset Value
047860h	CAN1 Mailbox 6: Message Identifier	C1MB6	XXXX XXXXh
047861h			
047862h			
047863h			
047864h			
047865h	CAN1 Mailbox 6: Data Length		XXh
047866h	CAN1 Mailbox 6: Data Field		XXXX XXXX
047867h			XXXX XXXXh
047868h			
047869h			
04786Ah			
04786Bh			
04786Ch			
04786Dh			
04786Eh	CAN1 Mailbox 6: Time Stamp		XXXXh
04786Fh			
047870h	CAN1 Mailbox 7: Message Identifier	C1MB7	XXXX XXXXh
047871h			
047872h			
047873h			
047874h			
047875h	CAN1 Mailbox 7: Data Length		XXh
047876h	CAN1 Mailbox 7: Data Field		XXXX XXXX
047877h			XXXX XXXXh
047878h			
047879h			
04787Ah			
04787Bh			
04787Ch			
04787Dh			
04787Eh	CAN1 Mailbox 7: Time Stamp		XXXXh
04787Fh			
047880h	CAN1 Mailbox 8: Message Identifier	C1MB8	XXXX XXXXh
047881h			
047882h			
047883h			
047884h			
047885h	CAN1 Mailbox 8: Data Length		XXh
047886h	CAN1 Mailbox 8: Data Field		XXXX XXXX
047887h			XXXX XXXXh
047888h			
047889h			
04788Ah			
04788Bh			
04788Ch			
04788Dh			
04788Eh	CAN1 Mailbox 8: Time Stamp		XXXXh
04788Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.33 SFR List (33)

Address	Register	Symbol	Reset Value
047950h	CAN1 Mailbox 21: Message Identifier	C1MB21	XXXX XXXXh
047951h			
047952h			
047953h			
047954h			
047955h	CAN1 Mailbox 21: Data Length		XXh
047956h	CAN1 Mailbox 21: Data Field		XXXX XXXX
047957h			XXXX XXXXh
047958h			
047959h			
04795Ah			
04795Bh			
04795Ch			
04795Dh			
04795Eh	CAN1 Mailbox 21: Time Stamp		XXXXh
04795Fh			
047960h	CAN1 Mailbox 22: Identifier	C1MB22	XXXX XXXXh
047961h			
047962h			
047963h			
047964h			
047965h	CAN1 Mailbox 22: Data Length		XXh
047966h	CAN1 Mailbox 22: Data Field		XXXX XXXX
047967h			XXXX XXXXh
047968h			
047969h			
04796Ah			
04796Bh			
04796Ch			
04796Dh			
04796Eh	CAN1 Mailbox 22: Time Stamp		XXXXh
04796Fh			
047970h	CAN1 Mailbox 23: Message Identifier	C1MB23	XXXX XXXXh
047971h			
047972h			
047973h			
047974h			
047975h	CAN1 Mailbox 23: Data Length		XXh
047976h	CAN1 Mailbox 23: Data Field		XXXX XXXX
047977h			XXXX XXXXh
047978h			
047979h			
04797Ah			
04797Bh			
04797Ch			
04797Dh			
04797Eh	CAN1 Mailbox 23: Time Stamp		XXXXh
04797Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.39 SFR List (39)

Address	Register	Symbol	Reset Value
047B40h	CAN1 Control Register	C1CTLR	0000 0101b
047B41h			0000 0000b
047B42h	CAN1 Status Register	C1STR	0000 0101b
047B43h			0000 0000b
047B44h	CAN1 Bit Configuration Register	C1BCR	00 0000h
047B45h			
047B46h			
047B47h	CAN1 Clock Select Register	C1CLKR	000X 0000b
047B48h	CAN1 Receive FIFO Control Register	C1RFCR	1000 0000b
047B49h	CAN1 Receive FIFO Pointer Control Register	C1RFPCR	XXh
047B4Ah	CAN1 Transmit FIFO Control Register	C1TFCR	1000 0000b
047B4Bh	CAN1 Transmit FIFO Pointer Control Register	C1TFPCR	XXh
047B4Ch	CAN1 Error Interrupt Enable Register	C1EIER	00h
047B4Dh	CAN1 Error Interrupt Factor Judge Register	C1EIFR	00h
047B4Eh	CAN1 Receive Error Count Register	C1RECR	00h
047B4Fh	CAN1 Transmit Error Count Register	C1TECR	00h
047B50h	CAN1 Error Code Store Register	C1ECSR	00h
047B51h	CAN1 Channel Search Support Register	C1CSSR	XXh
047B52h	CAN1 Mailbox Search Status Register	C1MSSR	1000 0000b
047B53h	CAN1 Mailbox Search Mode Register	C1MSMR	0000 0000b
047B54h	CAN1 Time Stamp Register	C1TSR	0000h
047B55h			
047B56h	CAN1 Acceptance Filter Support Register	C1AFSR	XXXXh
047B57h			
047B58h	CAN1 Test Control Register	C1TCR	00h
047B59h			
047B5Ah			
047B5Bh			
047B5Ch			
047B5Dh			
047B5Eh			
047B5Fh			
047B60h to 047BFFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.43 SFR List (43)

Address	Register	Symbol	Reset Value
047C90h	CAN0 Mailbox 9: Message Identifier	C0MB9	XXXX XXXXh
047C91h			
047C92h			
047C93h			
047C94h			
047C95h	CAN0 Mailbox 9: Data Length		XXh
047C96h	CAN0 Mailbox 9: Data Field		XXXX XXXX
047C97h			XXXX XXXXh
047C98h			
047C99h			
047C9Ah			
047C9Bh			
047C9Ch			
047C9Dh			
047C9Eh	CAN0 Mailbox 9: Time Stamp		XXXXh
047C9Fh			
047CA0h	CAN0 Mailbox 10: Message Identifier	C0MB10	XXXX XXXXh
047CA1h			
047CA2h			
047CA3h			
047CA4h			
047CA5h	CAN0 Mailbox 10: Data Length		XXh
047CA6h	CAN0 Mailbox 10: Data Field		XXXX XXXX
047CA7h			XXXX XXXXh
047CA8h			
047CA9h			
047CAAh			
047CABh			
047CACh			
047CADh			
047CAEh	CAN0 Mailbox 10: Time Stamp		XXXXh
047CAFh			
047CB0h	CAN0 Mailbox 11: Message Identifier	C0MB11	XXXX XXXXh
047CB1h			
047CB2h			
047CB3h			
047CB4h			
047CB5h	CAN0 Mailbox 11: Data Length		XXh
047CB6h	CAN0 Mailbox 11: Data Field		XXXX XXXX
047CB7h			XXXX XXXXh
047CB8h			
047CB9h			
047CBAh			
047CBBh			
047CBCh			
047CBDh			
047CBEh	CAN0 Mailbox 11: Time Stamp		XXXXh
047CBFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.53 SFR List (53)

Address	Register	Symbol	Reset Value
047F40h	CAN0 Control Register	C0CTLR	0000 0101b
047F41h			0000 0000b
047F42h	CAN0 Status Register	C0STR	0000 0101b
047F43h			0000 0000b
047F44h	CAN0 Bit Configuration Register	C0BCR	00 0000h
047F45h			
047F46h			
047F47h	CAN0 Clock Select Register	C0CLKR	000X 0000b
047F48h	CAN0 Receive FIFO Control Register	C0RFCR	1000 0000b
047F49h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	XXh
047F4Ah	CAN0 Transmit FIFO Control Register	C0TFCR	1000 0000b
047F4Bh	CAN0 Transmit FIFO Pointer Control Register	C0TFPCR	XXh
047F4Ch	CAN0 Error Interrupt Enable Register	C0EIER	00h
047F4Dh	CAN0 Error Interrupt Factor Judge Register	C0EIFR	00h
047F4Eh	CAN0 Receive Error Count Register	C0RECR	00h
047F4Fh	CAN0 Transmit Error Count Register	C0TECR	00h
047F50h	CAN0 Error Code Store Register	C0ECSR	00h
047F51h	CAN0 Channel Search Support Register	C0CSSR	XXh
047F52h	CAN0 Mailbox Search Status Register	C0MSSR	1000 0000b
047F53h	CAN0 Mailbox Search Mode Register	C0MSMR	0000 0000b
047F54h	CAN0 Time Stamp Register	C0TSR	0000h
047F55h			
047F56h	CAN0 Acceptance Filter Support Register	C0AFSR	XXXXh
047F57h			
047F58h	CAN0 Test Control Register	C0TCR	00h
047F59h			
047F5Ah			
047F5Bh			
047F5Ch			
047F5Dh			
047F5Eh			
047F5Fh			
047F60h to 047FFFh			
048000h to 04FFFFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 5.6 Operating Conditions (5/5)
(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable ripple voltage	V_{CC} = 5.0 V			0.5	Vp-p
		V_{CC} = 3.0 V			0.3	Vp-p
$dV_{r(VCC)}/dt$	Ripple voltage gradient	V_{CC} = 5.0 V			±0.3	V/ms
		V_{CC} = 3.0 V			±0.3	V/ms
$f_{r(VCC)}$	Allowable ripple frequency				10	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

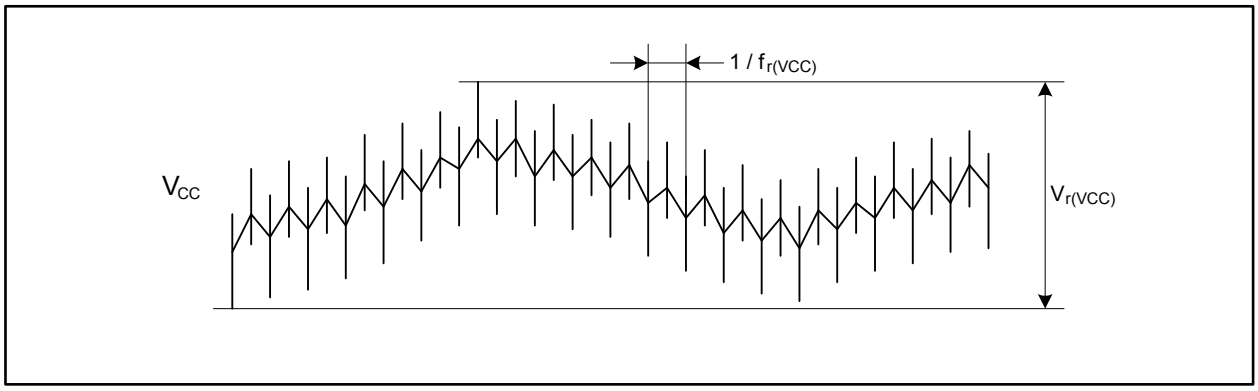


Figure 5.2 Ripple Waveform

V_{CC} = 5 V

Table 5.18 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = T_{opr}, and $f_{(BCLK)}$ = 32 MHz, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}				10	Bits
—	Absolute error	V_{REF} = V_{CC} = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 (1)			±3	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	V_{REF} = V_{CC} = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 (1)			±3	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error					±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	V_{REF} = V_{CC}		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		2.06			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.69			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		1.75			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.06			µs
t_{SAMP}	Sampling time	ϕ_{AD} = 16 MHz		0.188			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function		0.25		16	MHz
		With sample and hold function		1		16	MHz

Note:
1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.27 Timer B Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time (one edge counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{c(TB)}$	TBiIN input clock cycle time (both edges counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.28 Timer B Input (pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.29 Timer B Input (pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

V_{CC} = 3.3 V

Table 5.41 Electrical Characteristics (1/3) (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, T_a = T_{opr}, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	I_{OH} = -1 mA	V_{CC} - 0.6		V_{CC}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	I_{OL} = 1 mA			0.5	V

Note:
1. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

V_{CC} = 3.3 V

Table 5.44 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 3.0 to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_a = T_{opr}, and $f_{(BCLK)}$ = 32 MHz, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}				10	Bits
—	Absolute error	V_{REF} = V_{CC} = 3.3 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 (1)			±5	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	V_{REF} = V_{CC} = 3.3 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 (1)			±5	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error	V_{REF} = V_{CC} = 3.3 V				±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	V_{REF} = V_{CC}		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		3.3			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 10 MHz, with sample and hold function		2.8			µs
t_{SAMP}	Sampling time	ϕ_{AD} = 10 MHz		0.3			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function		0.25		10	MHz
		With sample and hold function		1		10	MHz

Note:
1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.

V_{CC} = 3.3 V

Timing Requirements (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.60 Multi-master I^2C-bus Interface

Symbol	Characteristic	Value				Unit
		Standard-mode		Fast-mode		
		Min.	Max.	Min.	Max.	
$t_{w(SCLH)}$	MSCL input high level pulse width	600		600		ns
$t_{w(SCLL)}$	MSCL input low level pulse width	600		600		ns
$t_{r(SCL)}$	MSCL input rise time		1000		300	ns
$t_{f(SCL)}$	MSCL input fall time		300		300	ns
$t_{r(SDA)}$	MSDA input rise time		1000		300	ns
$t_{f(SDA)}$	MSDA input fall time		300		300	ns
$t_{h(SDA-SCL)S}$	MSCL high level hold time after START condition/repeated START condition	(1)		2 × $t_{c(\phi IIC)}$ + 40		ns
$t_{su(SCL-SDA)P}$	MSCL high level setup time for repeated START condition/STOP condition	(1)		2 × $t_{c(\phi IIC)}$ + 40		ns
$t_{w(SDAH)P}$	MSDA high level pulse width after STOP condition	(1)		4 × $t_{c(\phi IIC)}$ + 40		ns
$t_{su(SDA-SCL)}$	MSDA input setup time	100		100		ns
$t_{h(SCL-SDA)}$	MSDA input hold time	0		0		ns

Note:

1. The value is calculated using the formulas below based on a value SSC set by bits SSC4 to SSC0 in the I2CSSCR register:

   $t_{h(SDA-SCL)S}$ = SSC ÷ 2 × $t_{c(\phi IIC)}$ + 40 [ns]

   $t_{su(SCL-SDA)P}$ = (SSC ÷ 2 + 1) × $t_{c(\phi IIC)}$ + 40 [ns]

   $t_{w(SDAH)P}$ = (SSC + 1) × $t_{c(\phi IIC)}$ + 40 [ns]

V_{CC} = 3.3 V

Switching Characteristics (V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.63 Serial Interface

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	Refer to Figure 5.6		80	ns
$t_{h(C-Q)}$	TXDi output hold time		0		ns

Table 5.64 Intelligent I/O

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(ISCLK2-TXD)}$	ISTXD2 output delay time	Refer to Figure 5.6		180	ns
$t_{h(ISCLK2-RXD)}$	ISTXD2 output hold time		0		ns

Table 5.65 Multi-master I²C-bus Interface (Standard-mode)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{f(SCL)}$	MSCL output fall time	Refer to Figure 5.6	2		ns
$t_{f(SDA)}$	MSDA output fall time		2		ns
$t_{d(SDA-SCL)S}$	MSCL output delay time after START condition/repeated START condition		$20 \times t_{c(\phi IIC)} - 120$	$52 \times t_{c(\phi IIC)} - 40$	ns
$t_{d(SCL-SDA)P}$	Repeated START condition/STOP condition output delay time after MSCL becomes high		$20 \times t_{c(\phi IIC)} + 40$	$52 \times t_{c(\phi IIC)} + 120$	ns
$t_{d(SCL-SDA)}$	MSDA output delay time		$2 \times t_{c(\phi IIC)} + 40$	$3 \times t_{c(\phi IIC)} + 120$	ns

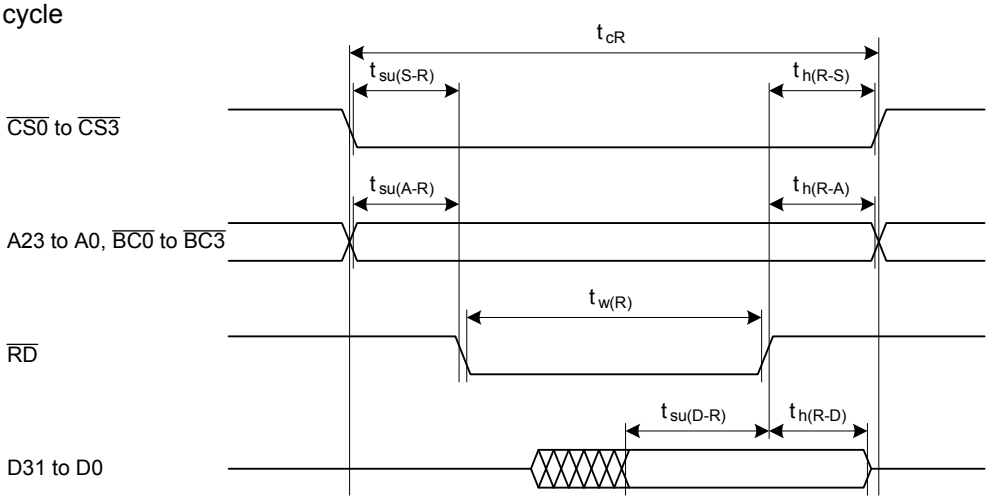
Table 5.66 Multi-master I²C-bus Interface (Fast-mode)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{f(SCL)}$	MSCL output fall time	Refer to Figure 5.6	2 (1)		ns
$t_{f(SDA)}$	MSDA output fall time		2 (1)		ns
$t_{d(SDA-SCL)S}$	MSCL output delay time after START condition/repeated START condition		$10 \times t_{c(\phi IIC)} - 120$	$26 \times t_{c(\phi IIC)} - 40$	ns
$t_{d(SCL-SDA)P}$	Repeated START condition/STOP condition output delay time after MSCL becomes high		$10 \times t_{c(\phi IIC)} + 40$	$26 \times t_{c(\phi IIC)} + 120$	ns
$t_{d(SCL-SDA)}$	MSDA output delay time		$2 \times t_{c(\phi IIC)} + 40$	$3 \times t_{c(\phi IIC)} + 120$	ns

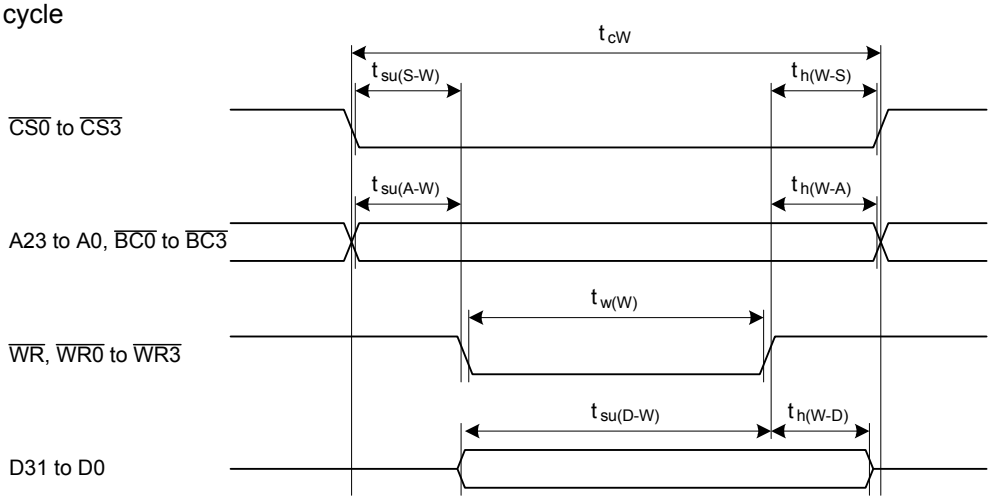
Note:
1. External circuits are required to satisfy the I²C-bus specification.

External bus timing (separate bus)

Read cycle



Write cycle



Measurement conditions

Item		V_{CC} = 4.2 to 5.5 V	V_{CC} = 3.0 to 3.6 V
Criterion for input voltage	V_{IH}	2.5 V	1.5 V
	V_{IL}	0.8 V	0.5 V
Criterion for output voltage	V_{OH}	2.0 V	2.4 V
	V_{OL}	0.8 V	0.5 V

Figure 5.8 External Bus Timing for Separate Bus

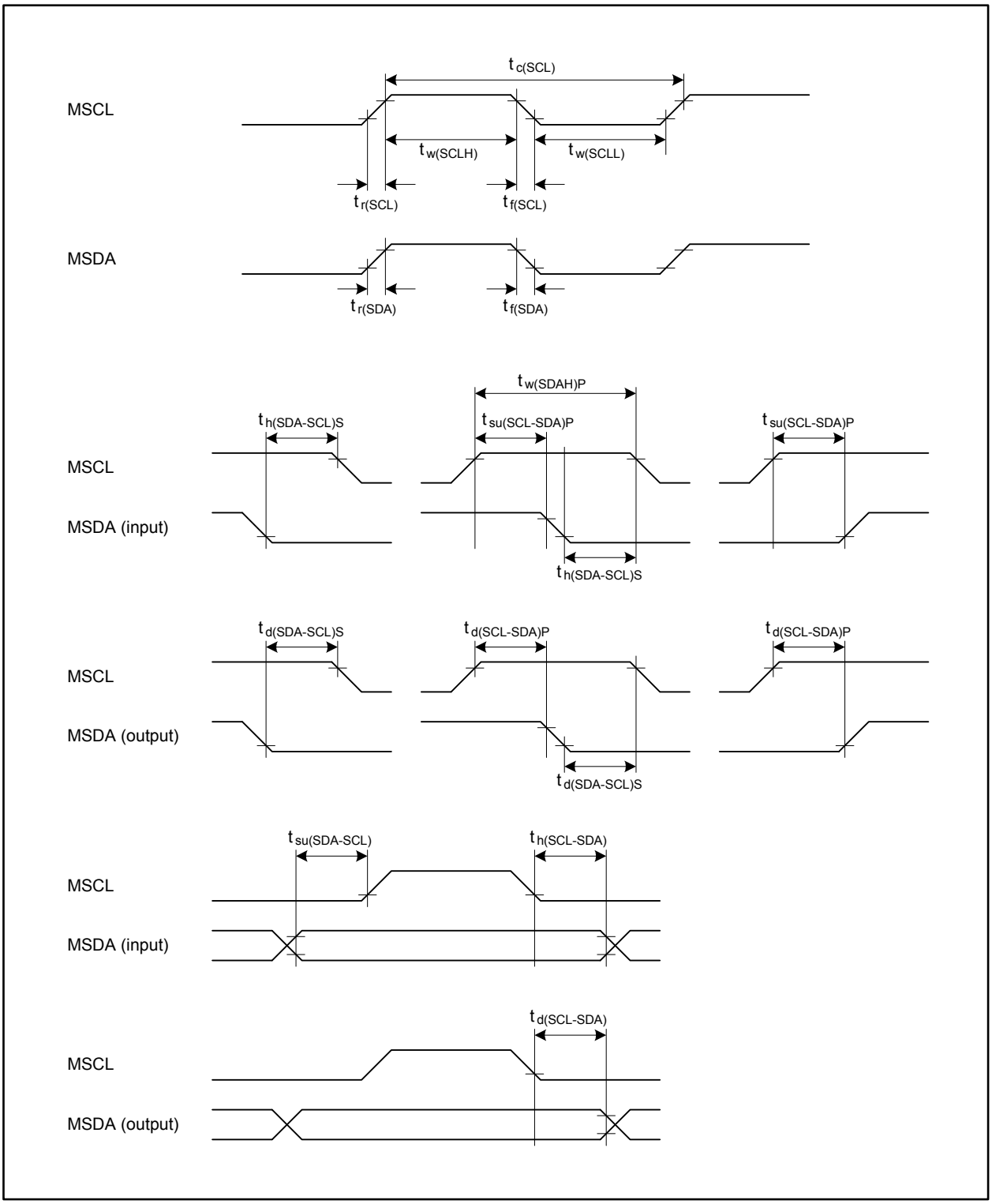


Figure 5.11 Timing of Multi-master I²C-bus Interface