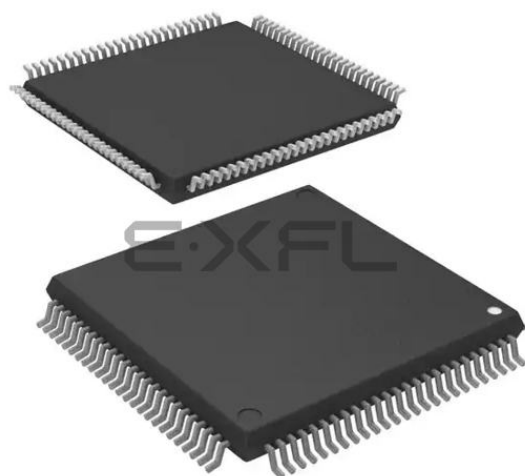




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Details

Product Status	Obsolete
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I ² C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	640KB (640K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64187dfb-u0

Table 1.7 Pin Characteristics for the 144-pin Package (1/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Module Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
1		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2		P9_5			CLK4/CAN1IN/ CAN1WU		ANEX0	
3		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
4		P9_3		TB3IN	CTS3/RTS3/SS3		DA0	
5		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/ISTXD2/ IEOUT		
6		P9_1		TB1IN	RXD3/SCL3/STXD3	ISRXD2/IEIN		
7		P9_0		TB0IN	CLK3			
8		P14_6	INT8					
9		P14_5	INT7					
10		P14_4	INT6					
11		P14_3						
12	VDC0							
13		P14_1						
14	VDC1							
15	NSD							
16	CNVSS							
17	XCIN	P8_7						
18	XCOU	P8_6						
19	RESET							
20	XOUT							
21	VSS							
22	XIN							
23	VCC							
24		P8_5	NMI					
25		P8_4	INT2					
26		P8_3	INT1		CAN0IN/CAN0WU/ CAN1IN/CAN1WU			
27		P8_2	INT0		CAN0OUT/CAN1OUT			
28		P8_1		TA4IN/U	CTS5/RTS5/SS5	IIO1_5/UD0B/UD1B		
29		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A		
30		P7_7		TA3IN	CLK5/CAN0IN/ CAN0WU	IIO1_4/UD0B/UD1B		
31		P7_6		TA3OUT	TXD5/SDA5/SRXD5/ CTS8/RTS8/CAN0OUT	IIO1_3/UD0A/UD1A		
32		P7_5		TA2IN/W	RXD8	IIO1_2		
33		P7_4		TA2OUT/W	CLK8	IIO1_1		
34		P7_3		TA1IN/V	CTS2/RTS2/SS2/TXD8	IIO1_0		
35		P7_2		TA1OUT/V	CLK2			
36		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2/ MSCL	IIO1_7/OUTC2_2/ ISRXD2/IEIN		

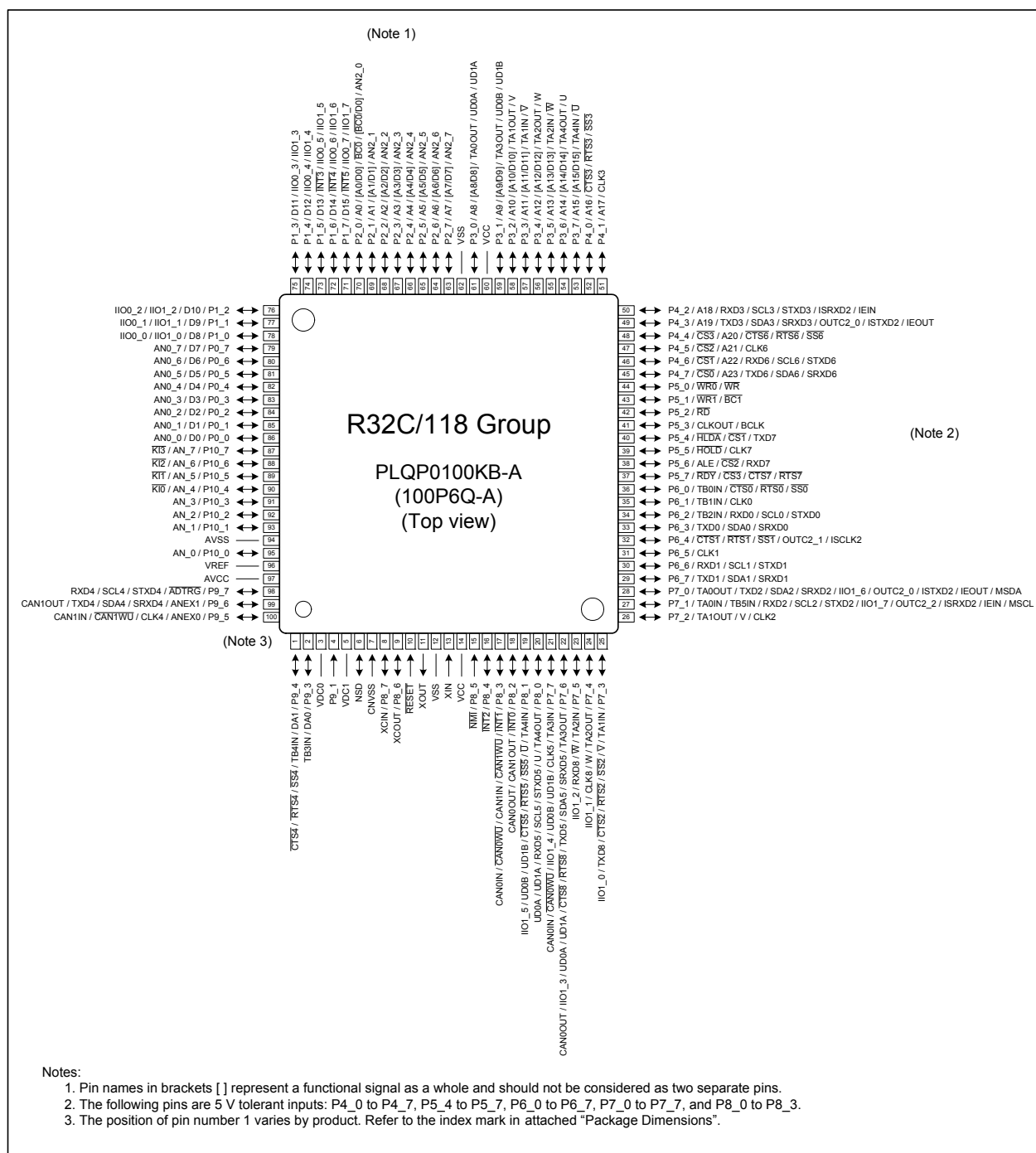


Figure 1.4 Pin Assignment for the 100-pin Package (top view)

Table 1.12 Pin Characteristics for the 100-pin Package (2/3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Module Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
39		P5_5			CLK7			HOLD
40		P5_4			TXD7			HLDA/CS1
41		P5_3						CLKOUT/ BCLK
42		P5_2						RD
43		P5_1						WR1/BC1
44		P5_0						WR0/WR
45		P4_7			TXD6/SDA6/SRXD6			CS0/A23
46		P4_6			RXD6/SCL6/STXD6			CS1/A22
47		P4_5			CLK6			CS2/A21
48		P4_4			CTS6/RTS6/SS6			CS3/A20
49		P4_3			TXD3/SDA3/SRXD3	OUTC2_0/ISTXD2/ IEOUT		A19
50		P4_2			RXD3/SCL3/STXD3	ISRXD2/IEIN		A18
51		P4_1			CLK3			A17
52		P4_0			CTS3/RTS3/SS3			A16
53		P3_7		TA4IN/U				A15/(D15)
54		P3_6		TA4OUT/U				A14/(D14)
55		P3_5		TA2IN/W				A13/(D13)
56		P3_4		TA2OUT/W				A12/(D12)
57		P3_3		TA1IN/V				A11/(D11)
58		P3_2		TA1OUT/V				A10/(D10)
59		P3_1		TA3OUT		UD0B/UD1B		A9/(D9)
60	VCC							
61		P3_0		TA0OUT		UD0A/UD1A		A8/(D8)
62	VSS							
63		P2_7					AN2_7	A7/(D7)
64		P2_6					AN2_6	A6/(D6)
65		P2_5					AN2_5	A5/(D5)
66		P2_4					AN2_4	A4/(D4)
67		P2_3					AN2_3	A3/(D3)
68		P2_2					AN2_2	A2/(D2)
69		P2_1					AN2_1	A1/(D1)
70		P2_0					AN2_0	A0/(D0)/ BC0/(D0)
71		P1_7	INT5			IIO0_7/IIO1_7		D15
72		P1_6	INT4			IIO0_6/IIO1_6		D14
73		P1_5	INT3			IIO0_5/IIO1_5		D13
74		P1_4				IIO0_4/IIO1_4		D12
75		P1_3				IIO0_3/IIO1_3		D11

Table 1.16 Pin Definitions and Functions (3/4)

Function	Symbol	I/O	Description
I/O port (1, 2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7	I/O	I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. Some ports are 5 V tolerant inputs. Pull-up resistors and N-channel open drain setting can be enabled on some ports. Refer to Table 1.18 "Pin Specifications" for details
Input port (2)	P9_1 (for 100-pin package) P14_1 (for 144-pin package)	I	Input port in CMOS Pull-up resistor is selectable. Refer to Table 1.18 "Pin Specifications" for details
Timer A	TA0OUT to TA4OUT	I/O	Timers A0 to A4 input/output
	TA0IN to TA4IN	I	Timers A0 to A4 input
Timer B	TB0IN to TB5IN	I	Timers B0 to B5 input
Three-phase motor control timer output	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	Three-phase motor control timer output
Serial interface	CTS0 to CTS8	I	Handshake input
	RTS0 to RTS8	O	Handshake output
	CLK0 to CLK8	I/O	Transmit/receive clock input/output
	RXD0 to RXD8	I	Serial data input
	TXD0 to TXD8	O	Serial data output
I ² C-bus (simplified)	SDA0 to SDA6	I/O	Serial data input/output
	SCL0 to SCL6	I/O	Transmit/receive clock input/output
Serial interface special functions	STXD0 to STXD6	O	Serial data output in slave mode
	SRXD0 to SRXD6	I	Serial data input in slave mode
	SS0 to SS6	I	Input to control serial interface special functions

Notes:

1. Port P9_1 in the 100-pin package is an input-only port.
2. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only.

4. Special Function Registers (SFRs)

SFRs are memory-mapped peripheral registers that control the operation of peripherals. Table 4.1 SFR List (1) to Table 4.53 SFR List (53) list the SFR details.

Table 4.1 SFR List (1)

Address	Register	Symbol	Reset Value
000000h			
000001h			
000002h			
000003h			
000004h	Clock Control Register	CCR	0001 1000b
000005h			
000006h	Flash Memory Control Register	FMCR	0000 0001b
000007h	Protect Release Register	PRR	00h
000008h			
000009h			
00000Ah			
00000Bh			
00000Ch			
00000Dh			
00000Eh			
00000Fh			
000010h	External Bus Control Register 3/Flash Memory Rewrite Bus	EBC3/FEBC3	0000h
000011h	Control Register 3		
000012h	Chip Selects 2 and 3 Boundary Setting Register	CB23	00h
000013h			
000014h	External Bus Control Register 2	EBC2	0000h
000015h			
000016h	Chip Selects 1 and 2 Boundary Setting Register	CB12	00h
000017h			
000018h	External Bus Control Register 1	EBC1	0000h
000019h			
00001Ah	Chip Selects 0 and 1 Boundary Setting Register	CB01	00h
00001Bh			
00001Ch	External Bus Control Register 0/Flash Memory Rewrite Bus	EBC0/FEBC0	0000h
00001Dh	Control Register 0		
00001Eh	Peripheral Bus Control Register	PBC	0504h
00001Fh			
000020h to 00005Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.11 SFR List (11)

Address	Register	Symbol	Reset Value
000200h to 0002BFh			
0002C0h 0002C1h	X0 Register/Y0 Register	X0R/Y0R	XXXXh
0002C2h 0002C3h	X1 Register/Y1 Register	X1R/Y1R	XXXXh
0002C4h 0002C5h	X2 Register/Y2 Register	X2R/Y2R	XXXXh
0002C6h 0002C7h	X3 Register/Y3 Register	X3R/Y3R	XXXXh
0002C8h 0002C9h	X4 Register/Y4 Register	X4R/Y4R	XXXXh
0002CAh 0002CBh	X5 Register/Y5 Register	X5R/Y5R	XXXXh
0002CCh 0002CDh	X6 Register/Y6 Register	X6R/Y6R	XXXXh
0002CEh 0002CFh	X7 Register/Y7 Register	X7R/Y7R	XXXXh
0002D0h 0002D1h	X8 Register/Y8 Register	X8R/Y8R	XXXXh
0002D2h 0002D3h	X9 Register/Y9 Register	X9R/Y9R	XXXXh
0002D4h 0002D5h	X10 Register/Y10 Register	X10R/Y10R	XXXXh
0002D6h 0002D7h	X11 Register/Y11 Register	X11R/Y11R	XXXXh
0002D8h 0002D9h	X12 Register/Y12 Register	X12R/Y12R	XXXXh
0002DAh 0002DBh	X13 Register/Y13 Register	X13R/Y13R	XXXXh
0002DCh 0002DDh	X14 Register/Y14 Register	X14R/Y14R	XXXXh
0002DEh 0002DFh	X15 Register/Y15 Register	X15R/Y15R	XXXXh
0002E0h	X-Y Control Register	XYC	XXXX XX00b
0002E1h			
0002E2h			
0002E3h			
0002E4h	UART1 Special Mode Register 4	U1SMR4	00h
0002E5h	UART1 Special Mode Register 3	U1SMR3	00h
0002E6h	UART1 Special Mode Register 2	U1SMR2	00h
0002E7h	UART1 Special Mode Register	U1SMR	00h
0002E8h	UART1 Transmit/Receive Mode Register	U1MR	00h
0002E9h	UART1 Bit Rate Register	U1BRG	XXh
0002EAh 0002EBh	UART1 Transmit Buffer Register	U1TB	XXXXh
0002ECh	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
0002EDh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
0002EEh 0002EFh	UART1 Receive Buffer Register	U1RB	XXXXh

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.13 SFR List (13)

Address	Register	Symbol	Reset Value
000320h			
000321h			
000322h			
000323h			
000324h	UART3 Special Mode Register 4	U3SMR4	00h
000325h	UART3 Special Mode Register 3	U3SMR3	00h
000326h	UART3 Special Mode Register 2	U3SMR2	00h
000327h	UART3 Special Mode Register	U3SMR	00h
000328h	UART3 Transmit/Receive Mode Register	U3MR	00h
000329h	UART3 Bit Rate Register	U3BRG	XXh
00032Ah	UART3 Transmit Buffer Register	U3TB	XXXXh
00032Bh			
00032Ch	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
00032Dh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
00032Eh	UART3 Receive Buffer Register	U3RB	XXXXh
00032Fh			
000330h			
000331h			
000332h			
000333h			
000334h	UART2 Special Mode Register 4	U2SMR4	00h
000335h	UART2 Special Mode Register 3	U2SMR3	00h
000336h	UART2 Special Mode Register 2	U2SMR2	00h
000337h	UART2 Special Mode Register	U2SMR	00h
000338h	UART2 Transmit/Receive Mode Register	U2MR	00h
000339h	UART2 Bit Rate Register	U2BRG	XXh
00033Ah	UART2 Transmit Buffer Register	U2TB	XXXXh
00033Bh			
00033Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
00033Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
00033Eh	UART2 Receive Buffer Register	U2RB	XXXXh
00033Fh			
000340h	Count Start Register	TABSR	0000 0000b
000341h	Clock Prescaler Reset Register	CPSRF	0XXX XXXXb
000342h	One-shot Start Register	ONSF	0000 0000b
000343h	Trigger Select Register	TRGSR	0000 0000b
000344h	Increment/Decrement Select Register	UDF	0000 0000b
000345h			
000346h	Timer A0 Register	TA0	XXXXh
000347h			
000348h	Timer A1 Register	TA1	XXXXh
000349h			
00034Ah	Timer A2 Register	TA2	XXXXh
00034Bh			
00034Ch	Timer A3 Register	TA3	XXXXh
00034Dh			
00034Eh	Timer A4 Register	TA4	XXXXh
00034Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.21 SFR List (21)

Address	Register	Symbol	Reset Value
0400C0h	Port P4_0 Function Select Register	P4_0S	X0XX X000b
0400C1h	Port P5_0 Function Select Register	P5_0S	XXXX X000b
0400C2h	Port P4_1 Function Select Register	P4_1S	X0XX X000b
0400C3h	Port P5_1 Function Select Register	P5_1S	XXXX X000b
0400C4h	Port P4_2 Function Select Register	P4_2S	X0XX X000b
0400C5h	Port P5_2 Function Select Register	P5_2S	XXXX X000b
0400C6h	Port P4_3 Function Select Register	P4_3S	X0XX X000b
0400C7h	Port P5_3 Function Select Register	P5_3S	XXXX X000b
0400C8h	Port P4_4 Function Select Register	P4_4S	X0XX X000b
0400C9h	Port P5_4 Function Select Register	P5_4S	X0XX X000b
0400CAh	Port P4_5 Function Select Register	P4_5S	X0XX X000b
0400CBh	Port P5_5 Function Select Register	P5_5S	X0XX X000b
0400CCh	Port P4_6 Function Select Register	P4_6S	X0XX X000b
0400CDh	Port P5_6 Function Select Register	P5_6S	X0XX X000b
0400CEh	Port P4_7 Function Select Register	P4_7S	X0XX X000b
0400CFh	Port P5_7 Function Select Register	P5_7S	X0XX X000b
0400D0h	Port P6_0 Function Select Register	P6_0S	X0XX X000b
0400D1h	Port P7_0 Function Select Register	P7_0S	X0XX X000b
0400D2h	Port P6_1 Function Select Register	P6_1S	X0XX X000b
0400D3h	Port P7_1 Function Select Register	P7_1S	X0XX X000b
0400D4h	Port P6_2 Function Select Register	P6_2S	X0XX X000b
0400D5h	Port P7_2 Function Select Register	P7_2S	X0XX X000b
0400D6h	Port P6_3 Function Select Register	P6_3S	X0XX X000b
0400D7h	Port P7_3 Function Select Register	P7_3S	X0XX X000b
0400D8h	Port P6_4 Function Select Register	P6_4S	X0XX X000b
0400D9h	Port P7_4 Function Select Register	P7_4S	X0XX X000b
0400DAh	Port P6_5 Function Select Register	P6_5S	X0XX X000b
0400DBh	Port P7_5 Function Select Register	P7_5S	X0XX X000b
0400DCh	Port P6_6 Function Select Register	P6_6S	X0XX X000b
0400DDh	Port P7_6 Function Select Register	P7_6S	X0XX X000b
0400DEh	Port P6_7 Function Select Register	P6_7S	X0XX X000b
0400DFh	Port P7_7 Function Select Register	P7_7S	X0XX X000b
0400E0h	Port P8_0 Function Select Register	P8_0S	X0XX X000b
0400E1h	Port P9_0 Function Select Register	P9_0S	X0XX X000b
0400E2h	Port P8_1 Function Select Register	P8_1S	X0XX X000b
0400E3h	Port P9_1 Function Select Register	P9_1S	X0XX X000b
0400E4h	Port P8_2 Function Select Register	P8_2S	X0XX X000b
0400E5h	Port P9_2 Function Select Register	P9_2S	X0XX X000b
0400E6h	Port P8_3 Function Select Register	P8_3S	X0XX X000b
0400E7h	Port P9_3 Function Select Register	P9_3S	00XX X000b
0400E8h	Port P8_4 Function Select Register	P8_4S	XXXX X000b
0400E9h	Port P9_4 Function Select Register	P9_4S	00XX X000b
0400EAh			
0400EBh	Port P9_5 Function Select Register	P9_5S	00XX X000b
0400ECh	Port P8_6 Function Select Register	P8_6S	XXXX X000b
0400EDh	Port P9_6 Function Select Register	P9_6S	00XX X000b
0400EEh	Port P8_7 Function Select Register	P8_7S	XXXX X000b
0400EFh	Port P9_7 Function Select Register	P9_7S	X0XX X000b

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.29 SFR List (29)

Address	Register	Symbol	Reset Value
047890h	CAN1 Mailbox 9: Message Identifier	C1MB9	XXXX XXXXh
047891h			
047892h			
047893h			
047894h			
047895h	CAN1 Mailbox 9: Data Length		XXh
047896h	CAN1 Mailbox 9: Data Field		XXXX XXXX XXXX XXXXh
047897h			
047898h			
047899h			
04789Ah			
04789Bh			
04789Ch			
04789Dh			
04789Eh	CAN1 Mailbox 9: Time Stamp		XXXXh
04789Fh			
0478A0h	CAN1 Mailbox 10: Message Identifier	C1MB10	XXXX XXXXh
0478A1h			
0478A2h			
0478A3h			
0478A4h			
0478A5h	CAN1 Mailbox 10: Data Length		XXh
0478A6h	CAN1 Mailbox 10: Data Field		XXXX XXXX XXXX XXXXh
0478A7h			
0478A8h			
0478A9h			
0478AAh			
0478ABh			
0478ACh			
0478ADh			
0478AEh	CAN1 Mailbox 10: Time Stamp		XXXXh
0478AFh			
0478B0h	CAN1 Mailbox 11: Message Identifier	C1MB11	XXXX XXXXh
0478B1h			
0478B2h			
0478B3h			
0478B4h			
0478B5h	CAN1 Mailbox 11: Data Length		XXh
0478B6h	CAN1 Mailbox 11: Data Field		XXXX XXXX XXXX XXXXh
0478B7h			
0478B8h			
0478B9h			
0478BAh			
0478BBh			
0478BCh			
0478BDh			
0478BEh	CAN1 Mailbox 11: Time Stamp		XXXXh
0478BFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.31 SFR List (31)

Address	Register	Symbol	Reset Value
0478F0h	CAN1 Mailbox 15: Message Identifier	C1MB15	XXXX XXXXh
0478F1h			
0478F2h			
0478F3h			
0478F4h			
0478F5h	CAN1 Mailbox 15: Data Length		XXh
0478F6h	CAN1 Mailbox 15: Data Field		XXXX XXXX XXXX XXXXh
0478F7h			
0478F8h			
0478F9h			
0478FAh			
0478FBh			
0478FCh			
0478FDh			
0478FEh	CAN1 Mailbox 15: Time Stamp		XXXXh
0478FFh			
047900h	CAN1 Mailbox 16: Message Identifier	C1MB16	XXXX XXXXh
047901h			
047902h			
047903h			
047904h			
047905h	CAN1 Mailbox 16: Data Length		XXh
047906h	CAN1 Mailbox 16: Data Field		XXXX XXXX XXXX XXXXh
047907h			
047908h			
047909h			
04790Ah			
04790Bh			
04790Ch			
04790Dh			
04790Eh	CAN1 Mailbox 16: Time Stamp		XXXXh
04790Fh			
047910h	CAN1 Mailbox 17: Message Identifier	C1MB17	XXXX XXXXh
047911h			
047912h			
047913h			
047914h			
047915h	CAN1 Mailbox 17: Data Length		XXh
047916h	CAN1 Mailbox 17: Data Field		XXXX XXXX XXXX XXXXh
047917h			
047918h			
047919h			
04791Ah			
04791Bh			
04791Ch			
04791Dh			
04791Eh	CAN1 Mailbox 17: Time Stamp		XXXXh
04791Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.36 SFR List (36)

Address	Register	Symbol	Reset Value
0479E0h	CAN1 Mailbox 30: Message Identifier	C1MB30	XXXX XXXXh
0479E1h			
0479E2h			
0479E3h			
0479E4h			
0479E5h	CAN1 Mailbox 30: Data Length		XXh
0479E6h	CAN1 Mailbox 30: Data Field		XXXX XXXX XXXX XXXXh
0479E7h			
0479E8h			
0479E9h			
0479EAh			
0479EBh			
0479ECh			
0479EDh			
0479EEh	CAN1 Mailbox 30: Time Stamp	XXXXh	
0479EFh			
0479F0h	CAN1 Mailbox 31: Message Identifier	C1MB31	XXXX XXXXh
0479F1h			
0479F2h			
0479F3h			
0479F4h			
0479F5h	CAN1 Mailbox 31: Data Length		XXh
0479F6h	CAN1 Mailbox 31: Data Field		XXXX XXXX XXXX XXXXh
0479F7h			
0479F8h			
0479F9h			
0479FAh			
0479FBh			
0479FCh			
0479FDh			
0479FEh	CAN1 Mailbox 31: Time Stamp	XXXXh	
0479FFh			
047A00h	CAN1 Mask Register 0	C1MKR0	XXXX XXXXh
047A01h			
047A02h			
047A03h			
047A04h	CAN1 Mask Register 1	C1MKR1	XXXX XXXXh
047A05h			
047A06h			
047A07h			
047A08h	CAN1 Mask Register 2	C1MKR2	XXXX XXXXh
047A09h			
047A0Ah			
047A0Bh			
047A0Ch	CAN1 Mask Register 3	C1MKR3	XXXX XXXXh
047A0Dh			
047A0Eh			
047A0Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 5.3 Operating Conditions (2/5)
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted) ⁽¹⁾

Symbol	Characteristic		Value (2)			Unit
			Min.	Typ.	Max.	
C_{VDC}	Decoupling capacitance for voltage regulator	Inter-pin voltage: 1.5 V	2.4		10.0	μF

Notes:

1. The device is operationally guaranteed under these operating conditions.
2. This value should be met with due consideration to the following conditions: operating temperature, DC bias, aging, etc.

Table 5.4 Operating Conditions (3/5)**($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted) ⁽¹⁾**

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$I_{OH(peak)}$	High level peak output current ⁽²⁾ P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 ⁽³⁾			-10.0	mA
$I_{OH(avg)}$	High level average output current ⁽⁴⁾ P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 ⁽³⁾			-5.0	mA
$I_{OL(peak)}$	Low level peak output current ⁽²⁾ P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 ⁽³⁾			10.0	mA
$I_{OL(avg)}$	Low level average output current ⁽⁴⁾ P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 ⁽³⁾			5.0	mA

Notes:

- The device is operationally guaranteed under these operating conditions.
- The following conditions should be satisfied:
 - The sum of $I_{OL(peak)}$ of ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14, and P15 is 80 mA or less.
 - The sum of $I_{OL(peak)}$ of ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 is 80 mA or less.
 - The sum of $I_{OH(peak)}$ of ports P0, P1, P2, and P11 is -40 mA or less.
 - The sum of $I_{OH(peak)}$ of ports P8_6, P8_7, P9, P10, P14, and P15 is -40 mA or less.
 - The sum of $I_{OH(peak)}$ of ports P3, P4, P5, P12, and P13 is -40 mA or less.
 - The sum of $I_{OH(peak)}$ of ports P6, P7, and P8_0 to P8_4 is -40 mA or less.
- Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.
- Average value within 100 ms.

Table 5.12 Electrical Characteristics of Oscillator
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$f_{SO(PLL)}$	PLL clock self-oscillation frequency		35	50	65	MHz
$t_{LOCK(PLL)}$	PLL lock time ⁽¹⁾				1	ms
$t_{jitter(p-p)}$	PLL jitter period (p-p)				2.0	ns
$f_{(OCO)}$	On-chip oscillator frequency		62.5	125	250	kHz

Note:

1. This value is applicable only when the main clock oscillation is stable.

Table 5.13 Electrical Characteristics of Clock Circuitry
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$t_{rec(WAIT)}$	Recovery time from wait mode to low power mode				225	μ s
$t_{rec(STOP)}$	Recovery time from stop mode ⁽¹⁾				225	μ s

Note:

1. The recovery time from stop mode does not include the main clock oscillation stabilization time. The CPU starts operating before the oscillator is stabilized.

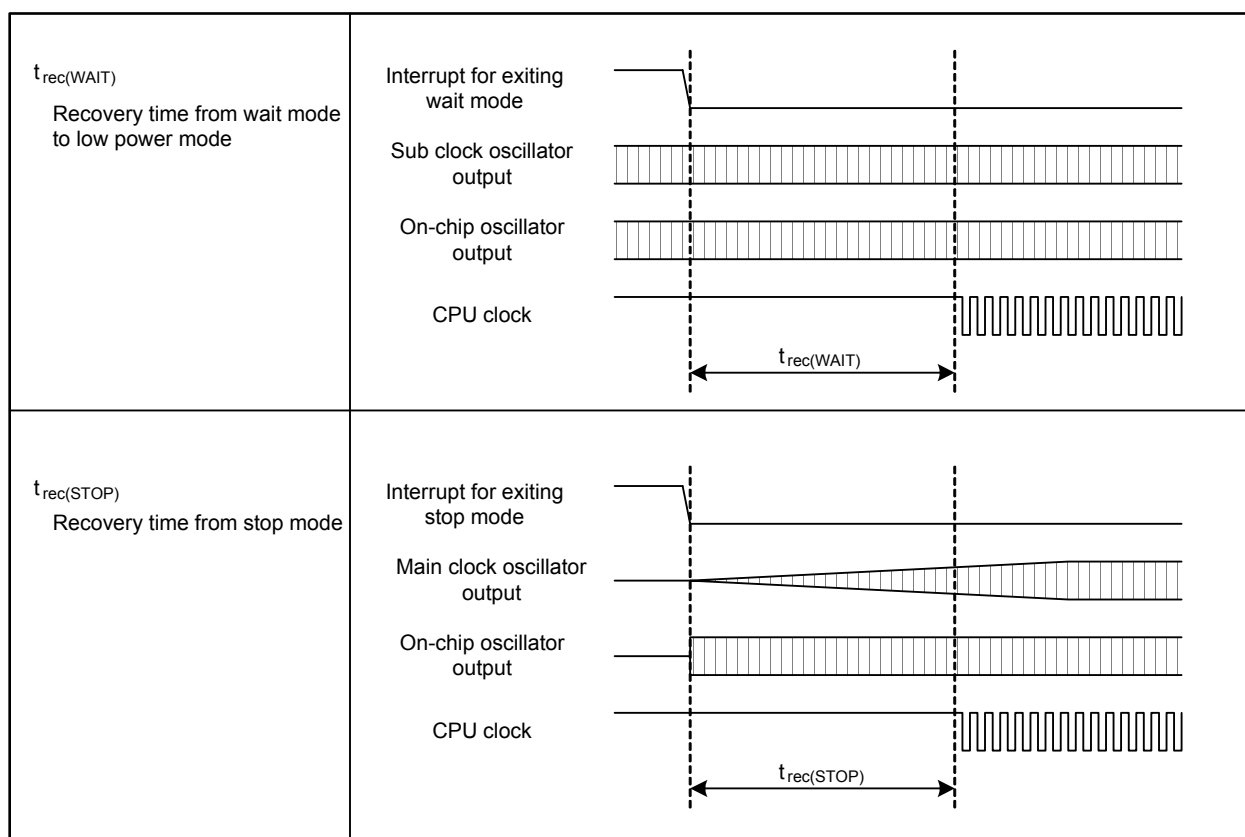


Figure 5.4 Clock Circuit Timing

$$V_{CC} = 5\text{ V}$$

Table 5.16 Electrical Characteristics (2/3)(V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, T_a = T_{opr}, and f_(CPU) = 64 MHz, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
V _{T+} - V _{T-}	Hysteresis	HOLD, RDY, NMI, INT0 to INT8, KI0 to KI3, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, CTS0 to CTS8, CLK0 to CLK8, RXD0 to RXD8, SCL0 to SCL6, SDA0 to SDA6, SS0 to SS6, SRXD0 to SRXD6, ADTRG, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, ISCLK2, ISRXD2, IEIN, MSCL, MSDA, CAN0IN, CAN1IN, CAN0WU, CAN1WU (1)	0.2		1.0	V
	RESET		0.2		1.8	V
I _{IH}	High level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7 (2)	V _I = 5 V			5.0 μA
I _{IL}	Low level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7 (2)	V _I = 0 V			-5.0 μA
R _{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7 (2)	V _I = 0 V			30 50 170 kΩ
R _{fXIN}	Feedback resistor	XIN		1.5		MΩ
R _{fXCIN}	Feedback resistor	XCIN		15		MΩ

Notes:

1. Pins INT6 to INT8 are available in the 144-pin package only.
2. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

$$V_{CC} = 5\text{ V}$$

Timing Requirements ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.22 Timer A Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	200		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.23 Timer A Input (gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	400		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.24 Timer A Input (external trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	200		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.25 Timer A Input (external trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.26 Timer A Input (increment/decrement switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{W(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{W(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{Su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.48 Timer A Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.49 Timer A Input (gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.50 Timer A Input (external trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.51 Timer A Input (external trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.52 Timer A Input (increment/decrement switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_h(TIN-UP)$	TAiOUT input hold time	400		ns

$$V_{CC} = 3.3 \text{ V}$$

Switching Characteristics ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.62 External Bus Timing (multiplexed bus)

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{su(S-ALE)}$	Chip-select setup time before ALE	Refer to Figure 5.6	(1)		ns
$t_{h(R-S)}$	Chip-select hold time after read		$1.5 \times t_{c(Base)} - 15$		ns
$t_{su(A-ALE)}$	Address setup time before ALE		(1)		ns
$t_{h(ALE-A)}$	Address hold time after ALE		$0.5 \times t_{c(Base)} - 5$		ns
$t_{h(R-A)}$	Address hold time after read		$1.5 \times t_{c(Base)} - 15$		ns
$t_{d(ALE-R)}$	ALE-read delay time		$0.5 \times t_{c(Base)} - 5$	$0.5 \times t_{c(Base)} + 10$	ns
$t_{w(ALE)}$	ALE pulse width		(1)		ns
$t_{dis(R-A)}$	Address disable time after read			8	ns
$t_{w(R)}$	Read pulse width		(1)		ns
$t_{h(W-S)}$	Chip-select hold time after write		$1.5 \times t_{c(Base)} - 15$		ns
$t_{h(W-A)}$	Address hold time after write		$1.5 \times t_{c(Base)} - 15$		ns
$t_{d(ALE-W)}$	ALE-write delay time		$0.5 \times t_{c(Base)} - 5$	$0.5 \times t_{c(Base)} + 10$	ns
$t_{w(W)}$	Write pulse width		(1)		ns
$t_{su(D-W)}$	Data setup time before write		(1)		ns
$t_{h(W-D)}$	Data hold time after write		$0.5 \times t_{c(Base)}$		ns

Note:

1. The value is calculated using the formulas below based on the base clock cycles ($t_{c(Base)}$) and respective cycles of $T_{su(A-R)}$, $T_{w(R)}$, $T_{su(A-W)}$, and $T_{w(W)}$ set by registers EBC0 to EBC3. If the calculation results in a negative value, modify the value to be set. For details on how to set values, refer to the User's manual.

$$t_{su(S-ALE)} = t_{su(A-ALE)} = (T_{su(A-R)} - 0.5) \times t_{c(Base)} - 15 \text{ [ns]}$$

$$t_{w(ALE)} = (T_{su(A-R)} - 0.5) \times t_{c(Base)} - 20 \text{ [ns]}$$

$$t_{w(R)} = T_{w(R)} \times t_{c(Base)} - 10 \text{ [ns]}$$

$$t_{w(W)} = t_{su(D-W)} = T_{w(W)} \times t_{c(Base)} - 10 \text{ [ns]}$$

Revision History	R32C/118 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
		2, 4	• Modified expressions “Main clock oscillator stop/re-oscillation detection”, “calculation transfer”, “chained transfer”, and “inputs/ outputs” in Tables 1.1 and 1.3 to “Main clock oscillator stop/restart detection”, “calculation result transfer”, “chain transfer”, and “I/O ports”, respectively
		7	• Completed “under development” phase of versions D and P products in Table 1.6
		10, 15	• Changed order of signals in Figures 1.3 and 1.4
		11, 16	• Changed order of timer pins “TB5IN/TA0IN” in Tables 1.7 and 1.11 to “TA0IN/TB5IN”
		21	• Changed expression “I ² C bus” in Table 1.16 to “I ² C-bus”
		23	• Modified Note 1 of Table 1.18
		Chapter 2. CPU	
		—	• Modified wording and enhanced description in this chapter
		25	• Corrected a typo “R3R0” in line 3 of 2.1.1 to “R3R1”
		Chapter 3. Memory	
		—	• Modified wording and enhanced description in this chapter
		Chapter 4. SFRs	
		—	• Changed expressions “I ² C Bus” and “I ² C-Bus” to “I ² C-bus”
		34, 35, 37	• Changed hexadecimal format of reset values for registers G1BCR0, G2BCR0, and G0BCR0 in Tables 4.6, 4.7, and 4.9 to binary
		41	• Changed register name “Increment/Decrement Counting Select Register” in Table 4.13 to “Increment/Decrement Select Register”
		43	• Corrected reset value “X00X X000b” for AD0CON2 register in Table 4.15 to “XX0X X000b”
		53	• Modified register name “I ² C Bus START Condition/STOP Condition Control Register” in Table 4.25 to “I ² C-bus START and STOP Conditions Control Register”; Corrected reset values for the following registers in: I2CSSCR, I2CCR1, I2CCR2, I2CSR, and I2CMR
		64, 65, 78, 79	• Changed register name “CANi Acceptance Mask Register k” in Tables 4.36, 4.37, 4.50, and 4.51 to “CANi Mask Register k”
		67, 81	• Corrected reset value “XXXX XX00b” for CiMSMR register in Tables 4.39 and 4.53 to “0000 0000b”
		Chapter 5. Electrical Characteristics	
		—	• Modified wording and enhanced description in this chapter
		88	• Changed expression “Programming and erasure endurance of flash memory” in Table 5.8 to “Program/erase cycles”; Changed its unit “times” to “Cycles”
		93, 106	• Added “MSCL” and “MSDA” to Tables 5.16 and 5.42
		94, 107	• Modified description “Drive power” in Tables 5.17 and 5.43 to “Drive strength”
		100, 113	• Corrected “INTi” in the title of Tables 5.32 and 5.58 to “ $\overline{\text{INTi}}$ ”
		101, 104, 114, 117	• Changed expression “restart condition” in Tables 5.34, 5.39, 5.40, 5.60, 5.65, and 5.66 to “repeated START condition”

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.