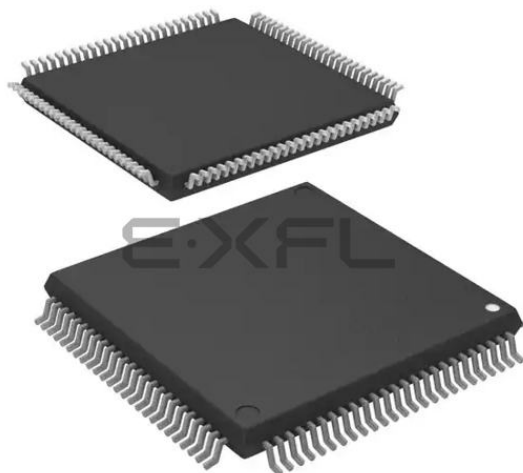




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Details

Product Status	Active
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I ² C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	63K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64189dfb-ub

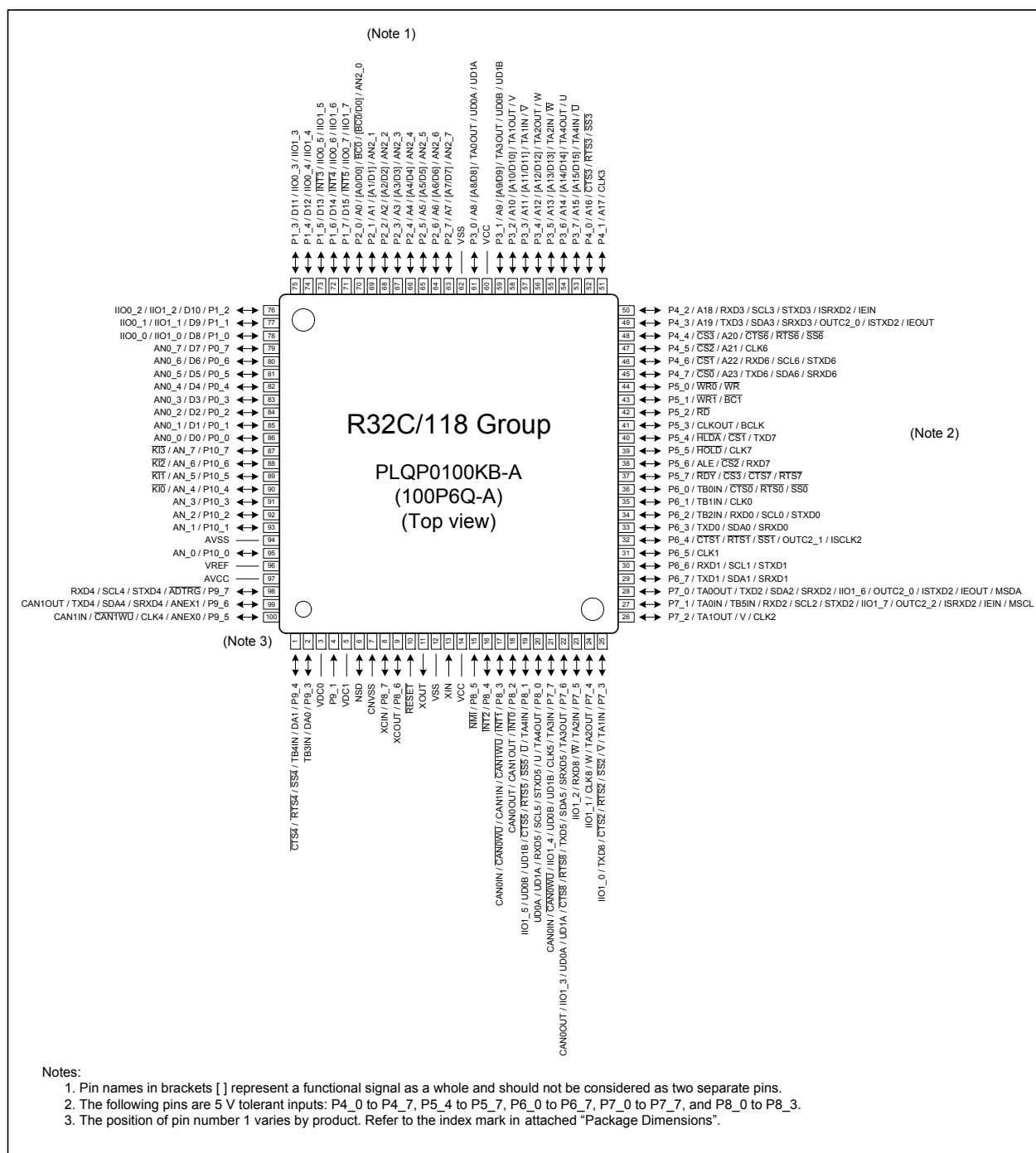


Figure 1.4 Pin Assignment for the 100-pin Package (top view)

Table 1.11 Pin Characteristics for the 100-pin Package (1/3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Module Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
2		P9_3		TB3IN			DA0	
3	VDC0							
4		P9_1						
5	VDC1							
6	NSD							
7	CNVSS							
8	XCIN	P8_7						
9	XCOUT	P8_6						
10	RESET							
11	XOUT							
12	VSS							
13	XIN							
14	VCC							
15		P8_5	NMI					
16		P8_4	INT2					
17		P8_3	INT1		CAN0IN/CAN0WU/ CAN1IN/CAN1WU			
18		P8_2	INT0		CAN0OUT/CAN1OUT			
19		P8_1		TA4IN/U	CTS5/RTS5/SS5	IIO1_5/UD0B/UD1B		
20		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A		
21		P7_7		TA3IN	CLK5/CAN0IN/ CAN0WU	IIO1_4/UD0B/UD1B		
22		P7_6		TA3OUT	TXD5/SDA5/SRXD5/ CTS8/RTS8/CAN0OUT	IIO1_3/UD0A/UD1A		
23		P7_5		TA2IN/W	RXD8	IIO1_2		
24		P7_4		TA2OUT/W	CLK8	IIO1_1		
25		P7_3		TA1IN/V	CTS2/RTS2/SS2/TXD8	IIO1_0		
26		P7_2		TA1OUT/V	CLK2			
27		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2/ MSCL	IIO1_7/OUTC2_2/ ISRXD2/IEIN		
28		P7_0		TA0OUT	TXD2/SDA2/SRXD2/ MSDA	IIO1_6/OUTC2_0/ ISTXD2/IEOUT		
29		P6_7			TXD1/SDA1/SRXD1			
30		P6_6			RXD1/SCL1/STXD1			
31		P6_5			CLK1			
32		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
33		P6_3			TXD0/SDA0/SRXD0			
34		P6_2		TB2IN	RXD0/SCL0/STXD0			
35		P6_1		TB1IN	CLK0			
36		P6_0		TB0IN	CTS0/RTS0/SS0			
37		P5_7			CTS7/RTS7			RDY/CS3
38		P5_6			RXD7			ALE/CS2

1.5 Pin Definitions and Functions

Tables 1.14 to 1.18 list the pin definitions and functions.

Table 1.14 Pin Definitions and Functions (1/4)

Function	Symbol	I/O	Description
Power supply	VCC, VSS	I	Applicable as follows: VCC = 3.0 to 5.5 V, VSS = 0 V
Connecting pins for decoupling capacitor	VDC0, VDC1	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC and VSS, respectively
Reset input	$\overline{\text{RESET}}$	I	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	This pin is to communicate with a debugger. It should be connected to VCC via a resistor of 1 to 4.7 k Ω
Main clock input	XIN	I	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOU. An external clock should be input at the XCIN while leaving the XCOU open
Sub clock output	XCOU	O	
BCLK output	BCLK	O	BCLK output
Clock output	CLKOUT	O	Output of the clock with the same frequency as low speed clocks, f8, or f32
External interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT8}}$ ⁽¹⁾	I	Input for external interrupts
NMI input	P8_5/ $\overline{\text{NMI}}$	I	Input for NMI
Key input interrupt	KI0 to KI3	I	Input for the key input interrupt
Bus control pins	D0 to D7	I/O	Input/output of data (D0 to D7) while accessing an external memory space with a separate bus
	D8 to D15	I/O	Input/output of data (D8 to D15) while accessing an external memory space with 16-bit or 32-bit separate bus
	D16 to D31 ⁽²⁾	I/O	Input/output of data (D16 to D31) while accessing an external memory space with 32-bit separate bus
	A0 to A23	O	Output of address bits A0 to A23
	A0/D0 to A7/D7	I/O	Output of address bits (A0 to A7) and input/output of data (D0 to D7) by time-division while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	Output of address bits (A8 to A15) and input/output of data (D8 to D15) by time-division while accessing an external memory space with 16-bit or 32-bit multiplexed bus

Notes:

1. Pins $\overline{\text{INT6}}$ to $\overline{\text{INT8}}$ are available in the 144-pin package only.
2. Pins D16 to D31 are available in the 144-pin package only.

Table 1.15 Pin Definitions and Functions (2/4)

Function	Symbol	I/O	Description
Bus control pins	$\overline{BC0}/D0$, $\overline{BC2}/D1$ (1)	I/O	Output of byte control ($\overline{BC0}$ and $\overline{BC2}$) and input/output of data (D0 and D1) by time-division while accessing an external memory space with multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	Chip select output
	$\overline{WR0}/\overline{WR1}/\overline{WR2}/\overline{WR3}$, $\overline{WR}/\overline{BC0}/\overline{BC1}/\overline{BC2}/\overline{BC3}$, $\overline{RD}$ (1)	O	Output of write, byte control, and read signals. Either $\overline{WRx}$ or $\overline{WR}$ and $\overline{BCx}$ can be selected by a program. Data is read when $\overline{RD}$ is low. - When $\overline{WR0}$, $\overline{WR1}$, $\overline{WR2}$, $\overline{WR3}$, and $\overline{RD}$ are selected, data is written to the following address: $4n+0$, when $\overline{WR0}$ is low $4n+1$, when $\overline{WR1}$ is low $4n+2$, when $\overline{WR2}$ is low $4n+3$, when $\overline{WR3}$ is low on 32-bit external data bus - or - an even address, when $\overline{WR0}$ is low - an odd address, when $\overline{WR1}$ is low on 16-bit external data bus - When $\overline{WR}$, $\overline{BC0}$, $\overline{BC1}$, $\overline{BC2}$, $\overline{BC3}$, and $\overline{RD}$ are selected, data is written, when $\overline{WR}$ is low and the following address is accessed: $4n+0$, when $\overline{BC0}$ is low $4n+1$, when $\overline{BC1}$ is low $4n+2$, when $\overline{BC2}$ is low $4n+3$, when $\overline{BC3}$ is low on 32-bit external data bus - or - an even address, when $\overline{BC0}$ is low - an odd address, when $\overline{BC1}$ is low on 16-bit external data bus
	ALE	O	Latch enable signal in multiplexed bus format
	$\overline{HOLD}$	I	The MCU is in a hold state while this pin is held low
	$\overline{HLDA}$	O	This pin is driven low while the MCU is held in a hold state
	$\overline{RDY}$	I	Bus cycle is extended by the CPU if this pin is low on the falling edge of BCLK

Note:

1. Pins $\overline{BC2}/D1$, $\overline{WR2}$, $\overline{WR3}$, $\overline{BC2}$, and $\overline{BC3}$ are available in the 144-pin package only.

4. Special Function Registers (SFRs)

SFRs are memory-mapped peripheral registers that control the operation of peripherals. Table 4.1 SFR List (1) to Table 4.53 SFR List (53) list the SFR details.

Table 4.1 SFR List (1)

Address	Register	Symbol	Reset Value
000000h			
000001h			
000002h			
000003h			
000004h	Clock Control Register	CCR	0001 1000b
000005h			
000006h	Flash Memory Control Register	FMCR	0000 0001b
000007h	Protect Release Register	PRR	00h
000008h			
000009h			
00000Ah			
00000Bh			
00000Ch			
00000Dh			
00000Eh			
00000Fh			
000010h	External Bus Control Register 3/Flash Memory Rewrite Bus	EBC3/FEBC3	0000h
000011h	Control Register 3		
000012h	Chip Selects 2 and 3 Boundary Setting Register	CB23	00h
000013h			
000014h	External Bus Control Register 2	EBC2	0000h
000015h			
000016h	Chip Selects 1 and 2 Boundary Setting Register	CB12	00h
000017h			
000018h	External Bus Control Register 1	EBC1	0000h
000019h			
00001Ah	Chip Selects 0 and 1 Boundary Setting Register	CB01	00h
00001Bh			
00001Ch	External Bus Control Register 0/Flash Memory Rewrite Bus	EBC0/FEBC0	0000h
00001Dh	Control Register 0		
00001Eh	Peripheral Bus Control Register	PBC	0504h
00001Fh			
000020h to 00005Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.3 SFR List (3)

Address	Register	Symbol	Reset Value
000088h	DMA1 Transfer Complete Interrupt Control Register	DM1IC	XXXX X000b
000089h	UART1/4 Bus Collision, START Condition/STOP Condition Detection Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000b
00008Ah	DMA3 Transfer Complete Interrupt Control Register	DM3IC	XXXX X000b
00008Bh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
00008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
00008Dh	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000b
00008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
00008Fh	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000b
000090h	UART0 Transmit/NACK Interrupt Control Register	S0TIC	XXXX X000b
000091h	Intelligent I/O Interrupt Control Register 5	IIO5IC	XXXX X000b
000092h	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000b
000093h	Intelligent I/O Interrupt Control Register 7	IIO7IC	XXXX X000b
000094h	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
000095h	Intelligent I/O Interrupt Control Register 9	IIO9IC	XXXX X000b
000096h	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
000097h	Intelligent I/O Interrupt Control Register 11	IIO11IC	XXXX X000b
000098h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
000099h			
00009Ah	INT4 Interrupt Control Register	INT4IC	XX00 X000b
00009Bh	CAN1 Wake-up Interrupt Control Register	C1WIC	XXXX X000b
00009Ch	INT2 Interrupt Control Register	INT2IC	XX00 X000b
00009Dh			
00009Eh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
00009Fh			
0000A0h	Intelligent I/O Interrupt Request Register 0	IIO0IR	0000 0XX1b
0000A1h	Intelligent I/O Interrupt Request Register 1	IIO1IR	0000 0XX1b
0000A2h	Intelligent I/O Interrupt Request Register 2	IIO2IR	0000 0X01b
0000A3h	Intelligent I/O Interrupt Request Register 3	IIO3IR	0000 XXX1b
0000A4h	Intelligent I/O Interrupt Request Register 4	IIO4IR	000X 0XX1b
0000A5h	Intelligent I/O Interrupt Request Register 5	IIO5IR	000X 0XX1b
0000A6h	Intelligent I/O Interrupt Request Register 6	IIO6IR	000X 0XX1b
0000A7h	Intelligent I/O Interrupt Request Register 7	IIO7IR	X00X 0XX1b
0000A8h	Intelligent I/O Interrupt Request Register 8	IIO8IR	XX0X 0XX1b
0000A9h	Intelligent I/O Interrupt Request Register 9	IIO9IR	0X00 0XX1b
0000AAh	Intelligent I/O Interrupt Request Register 10	IIO10IR	0X00 0XX1b
0000ABh	Intelligent I/O Interrupt Request Register 11	IIO11IR	0X00 0XX1b
0000ACh			
0000ADh			
0000AEh			
0000AFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.4 SFR List (4)

Address	Register	Symbol	Reset Value
0000B0h	Intelligent I/O Interrupt Enable Register 0	IIO0IE	00h
0000B1h	Intelligent I/O Interrupt Enable Register 1	IIO1IE	00h
0000B2h	Intelligent I/O Interrupt Enable Register 2	IIO2IE	00h
0000B3h	Intelligent I/O Interrupt Enable Register 3	IIO3IE	00h
0000B4h	Intelligent I/O Interrupt Enable Register 4	IIO4IE	00h
0000B5h	Intelligent I/O Interrupt Enable Register 5	IIO5IE	00h
0000B6h	Intelligent I/O Interrupt Enable Register 6	IIO6IE	00h
0000B7h	Intelligent I/O Interrupt Enable Register 7	IIO7IE	00h
0000B8h	Intelligent I/O Interrupt Enable Register 8	IIO8IE	00h
0000B9h	Intelligent I/O Interrupt Enable Register 9	IIO9IE	00h
0000BAh	Intelligent I/O Interrupt Enable Register 10	IIO10IE	00h
0000BBh	Intelligent I/O Interrupt Enable Register 11	IIO11IE	00h
0000BCh			
0000BDh			
0000BEh			
0000BFh			
0000C0h			
0000C1h	CAN0 Transmit Interrupt Control Register	C0TIC	XXXX X000b
0000C2h			
0000C3h	CAN0 Error Interrupt Control Register	C0EIC	XXXX X000b
0000C4h			
0000C5h	CAN1 Receive Interrupt Control Register	C1RIC	XXXX X000b
0000C6h			
0000C7h			
0000C8h			
0000C9h			
0000CAh			
0000CBh			
0000CCh			
0000CDh			
0000CEh			
0000CFh			
0000D0h	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	XXXX X000b
0000D1h			
0000D2h	CAN1 Transmit FIFO Interrupt Control Register	C1FTIC	XXXX X000b
0000D3h			
0000D4h			
0000D5h			
0000D6h			
0000D7h			
0000D8h			
0000D9h			
0000DAh			
0000DBh			
0000DCh			
0000DDh	UART7 Transmit Interrupt Control Register	S7TIC	XXXX X000b
0000DEh	INT7 Interrupt Control Register	INT7IC	XX00 X000b
0000DFh	UART8 Transmit Interrupt Control Register	S8TIC	XXXX X000b

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.12 SFR List (12)

Address	Register	Symbol	Reset Value
0002F0h			
0002F1h			
0002F2h			
0002F3h			
0002F4h	UART4 Special Mode Register 4	U4SMR4	00h
0002F5h	UART4 Special Mode Register 3	U4SMR3	00h
0002F6h	UART4 Special Mode Register 2	U4SMR2	00h
0002F7h	UART4 Special Mode Register	U4SMR	00h
0002F8h	UART4 Transmit/Receive Mode Register	U4MR	00h
0002F9h	UART4 Bit Rate Register	U4BRG	XXh
0002FAh	UART4 Transmit Buffer Register	U4TB	XXXXh
0002FBh			
0002FCh	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
0002FDh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
0002FEh	UART4 Receive Buffer Register	U4RB	XXXXh
0002FFh			
000300h	Count Start Register for Timers B3, B4, and B5	TBSR	000X XXXXb
000301h			
000302h	Timer A1-1 Register	TA11	XXXXh
000303h			
000304h	Timer A2-1 Register	TA21	XXXXh
000305h			
000306h	Timer A4-1 Register	TA41	XXXXh
000307h			
000308h	Three-phase PWM Control Register 0	INVC0	00h
000309h	Three-phase PWM Control Register 1	INVC1	00h
00030Ah	Three-phase Output Buffer Register 0	IDB0	XX11 1111b
00030Bh	Three-phase Output Buffer Register 1	IDB1	XX11 1111b
00030Ch	Dead Time Timer	DTT	XXh
00030Dh	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XXh
00030Eh			
00030Fh			
000310h	Timer B3 Register	TB3	XXXXh
000311h			
000312h	Timer B4 Register	TB4	XXXXh
000313h			
000314h	Timer B5 Register	TB5	XXXXh
000315h			
000316h			
000317h			
000318h			
000319h			
00031Ah			
00031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
00031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
00031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
00031Eh			
00031Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.18 SFR List (18)

Address	Register	Symbol	Reset Value
040000h	Flash Memory Control Register 0	FMR0	0X01 XX00b
040001h	Flash Memory Status Register 0	FMSR0	1000 0000b
040002h			
040003h			
040004h			
040005h			
040006h			
040007h			
040008h	Flash Register Protection Unlock Register 0	FPR0	00h
040009h	Flash Memory Control Register 1	FMR1	0000 0010b
04000Ah	Block Protect Bit Monitor Register 0	FBPM0	??X? ???b (1)
04000Bh	Block Protect Bit Monitor Register 1	FBPM1	XXX? ???b (1)
04000Ch			
04000Dh			
04000Eh			
04000Fh			
040010h			
040011h	Block Protect Bit Monitor Register 2	FBPM2	???? ???b (1)
040012h			
040013h			
040014h			
040015h			
040016h			
040017h			
040018h			
040019h			
04001Ah			
04001Bh			
04001Ch			
04001Dh			
04001Eh			
04001Fh			
040020h	PLL Control Register 0	PLC0	0000 0001b
040021h	PLL Control Register 1	PLC1	0001 1111b
040022h			
040023h			
040024h			
040025h			
040026h			
040027h			
040028h			
040029h			
04002Ah			
04002Bh			
04002Ch			
04002Dh			
04002Eh			
04002Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Note:

1. The reset value reflects the value of the protect bit for each block in the flash memory.

Table 4.32 SFR List (32)

Address	Register	Symbol	Reset Value
047920h	CAN1 Mailbox 18: Message Identifier	C1MB18	XXXX XXXXh
047921h			
047922h			
047923h			
047924h			
047925h	CAN1 Mailbox 18: Data Length		XXh
047926h	CAN1 Mailbox 18: Data Field		XXXX XXXX XXXX XXXXh
047927h			
047928h			
047929h			
04792Ah			
04792Bh			
04792Ch			
04792Dh			
04792Eh	CAN1 Mailbox18: Time Stamp		XXXXh
04792Fh			
047930h	CAN1 Mailbox 19: Message Identifier	C1MB19	XXXX XXXXh
047931h			
047932h			
047933h			
047934h			
047935h	CAN1 Mailbox 19: Data Length		XXh
047936h	CAN1 Mailbox 19: Data Field		XXXX XXXX XXXX XXXXh
047937h			
047938h			
047939h			
04793Ah			
04793Bh			
04793Ch			
04793Dh			
04793Eh	CAN1 Mailbox 19: Time Stamp		XXXXh
04793Fh			
047940h	CAN1 Mailbox 20: Message Identifier	C1MB20	XXXX XXXXh
047941h			
047942h			
047943h			
047944h			
047945h	CAN1 Mailbox 20: Data Length		XXh
047946h	CAN1 Mailbox 20: Data Field		XXXX XXXX XXXX XXXXh
047947h			
047948h			
047949h			
04794Ah			
04794Bh			
04794Ch			
04794Dh			
04794Eh	CAN1 Mailbox 20: Time Stamp		XXXXh
04794Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.34 SFR List (34)

Address	Register	Symbol	Reset Value
047980h	CAN1 Mailbox 24: Message Identifier	C1MB24	XXXX XXXXh
047981h			
047982h			
047983h			
047984h			
047985h	CAN1 Mailbox 24: Data Length		XXh
047986h	CAN1 Mailbox 24: Data Field		XXXX XXXX XXXX XXXXh
047987h			
047988h			
047989h			
04798Ah			
04798Bh			
04798Ch			
04798Dh			
04798Eh	CAN1 Mailbox 24: Time Stamp		XXXXh
04798Fh			
047990h	CAN1 Mailbox 25: Message Identifier	C1MB25	XXXX XXXXh
047991h			
047992h			
047993h			
047994h			
047995h	CAN1 Mailbox 25: Data Length		XXh
047996h	CAN1 Mailbox 25: Data Field		XXXX XXXX XXXX XXXXh
047997h			
047998h			
047999h			
04799Ah			
04799Bh			
04799Ch			
04799Dh			
04799Eh	CAN1 Mailbox 25: Time Stamp		XXXXh
04799Fh			
0479A0h	CAN1 Mailbox 26: Message Identifier	C1MB26	XXXX XXXXh
0479A1h			
0479A2h			
0479A3h			
0479A4h			
0479A5h	CAN1 Mailbox 26: Data Length		XXh
0479A6h	CAN1 Mailbox 26: Data Field		XXXX XXXX XXXX XXXXh
0479A7h			
0479A8h			
0479A9h			
0479AAh			
0479ABh			
0479ACh			
0479ADh			
0479AEh	CAN1 Mailbox 26: Time Stamp		XXXXh
0479AFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.44 SFR List (44)

Address	Register	Symbol	Reset Value
047CC0h	CAN0 Mailbox 12: Message Identifier	C0MB12	XXXX XXXXh
047CC1h			
047CC2h			
047CC3h			
047CC4h			
047CC5h	CAN0 Mailbox 12: Data Length		XXh
047CC6h	CAN0 Mailbox 12: Data Field		XXXX XXXX XXXX XXXXh
047CC7h			
047CC8h			
047CC9h			
047CCAh			
047CCBh			
047CCCh			
047CCDh			
047CCEh	CAN0 Mailbox 12: Time Stamp		XXXXh
047CCFh			
047CD0h	CAN0 Mailbox 13: Message Identifier	C0MB13	XXXX XXXXh
047CD1h			
047CD2h			
047CD3h			
047CD4h			
047CD5h	CAN0 Mailbox 13: Data Length		XXh
047CD6h	CAN0 Mailbox 13: Data Field		XXXX XXXX XXXX XXXXh
047CD7h			
047CD8h			
047CD9h			
047CDAh			
047CDBh			
047CDCh			
047CDDh			
047CDEh	CAN0 Mailbox 13: Time Stamp		XXXXh
047CDFh			
047CE0h	CAN0 Mailbox 14: Message Identifier	C0MB14	XXXX XXXXh
047CE1h			
047CE2h			
047CE3h			
047CE4h			
047CE5h	CAN0 Mailbox 14: Data Length		XXh
047CE6h	CAN0 Mailbox 14: Data Field		XXXX XXXX XXXX XXXXh
047CE7h			
047CE8h			
047CE9h			
047CEAh			
047CEBh			
047CECh			
047CEDh			
047CEEh	CAN0 Mailbox 14: Time Stamp		XXXXh
047CEFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.53 SFR List (53)

Address	Register	Symbol	Reset Value
047F40h	CAN0 Control Register	C0CTLR	0000 0101b
047F41h			0000 0000b
047F42h	CAN0 Status Register	C0STR	0000 0101b
047F43h			0000 0000b
047F44h	CAN0 Bit Configuration Register	C0BCR	00 0000h
047F45h			
047F46h			
047F47h	CAN0 Clock Select Register	C0CLKR	000X 0000b
047F48h	CAN0 Receive FIFO Control Register	C0RFCR	1000 0000b
047F49h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	XXh
047F4Ah	CAN0 Transmit FIFO Control Register	C0TFCR	1000 0000b
047F4Bh	CAN0 Transmit FIFO Pointer Control Register	C0TFPCR	XXh
047F4Ch	CAN0 Error Interrupt Enable Register	C0EIER	00h
047F4Dh	CAN0 Error Interrupt Factor Judge Register	C0EIFR	00h
047F4Eh	CAN0 Receive Error Count Register	C0RECR	00h
047F4Fh	CAN0 Transmit Error Count Register	C0TECR	00h
047F50h	CAN0 Error Code Store Register	C0ECSR	00h
047F51h	CAN0 Channel Search Support Register	C0CSSR	XXh
047F52h	CAN0 Mailbox Search Status Register	C0MSSR	1000 0000b
047F53h	CAN0 Mailbox Search Mode Register	C0MSMR	0000 0000b
047F54h	CAN0 Time Stamp Register	C0TSR	0000h
047F55h			
047F56h	CAN0 Acceptance Filter Support Register	C0AFSR	XXXXh
047F57h			
047F58h	CAN0 Test Control Register	C0TCR	00h
047F59h			
047F5Ah			
047F5Bh			
047F5Ch			
047F5Dh			
047F5Eh			
047F5Fh			
047F60h to 047FFFh			
048000h to 04FFFFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 5.2 Operating Conditions (1/5) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
V_{CC}	Digital supply voltage		3.0	5.0	5.5	V
AV_{CC}	Analog supply voltage			V_{CC}		V
V_{REF}	Reference voltage		3.0		V_{CC}	V
V_{SS}	Digital ground voltage			0		V
AV_{SS}	Analog ground voltage			0		V
dV_{CC}/dt	V_{CC} ramp up rate ($V_{CC} < 2.0$ V)		0.05			V/ms
V_{IH}	High level input voltage	XIN, $\overline{RESET}$, CNVSS, NSD, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P14_1, P14_3 to P14_6, P15_0 to P15_7 (3)	$0.8 \times V_{CC}$		V_{CC}	V
		P4_0 to P4_7, P5_4 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_3	$0.8 \times V_{CC}$		6.0	V
		P0_0 to P0_7, P1_0 to P1_7, in single-chip mode	$0.8 \times V_{CC}$		V_{CC}	V
		P12_0 to P12_7, P13_0 to P13_7 (3), in memory expansion mode or microprocessor mode	$0.5 \times V_{CC}$		V_{CC}	V
V_{IL}	Low level input voltage	XIN, $\overline{RESET}$, CNVSS, NSD, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P14_1, P14_3 to P14_6, P15_0 to P15_7 (3)	0		$0.2 \times V_{CC}$	V
		P0_0 to P0_7, P1_0 to P1_7, in single-chip mode	0		$0.2 \times V_{CC}$	V
		P12_0 to P12_7, P13_0 to P13_7 (3), in memory expansion mode or microprocessor mode	0		$0.16 \times V_{CC}$	V
T_{opr}	Operating temperature range	N version	-20		85	°C
		D version	-40		85	°C
		P version	-40		85	°C

Notes:

1. The device is operationally guaranteed under these operating conditions.
2. V_{IH} and V_{IL} for P8_7 are specified for P8_7 as a programmable port. These values are not applicable for P8_7 as XCIN.
3. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

$$V_{CC} = 5 \text{ V}$$

Table 5.18 A/D Conversion Characteristics ($V_{CC} = AV_{CC} = V_{REF} = 4.2 \text{ to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{(BCLK)} = 32 \text{ MHz}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
—	Absolute error	$V_{REF} = V_{CC} = 5 \text{ V}$			± 3	LSB
		AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 ⁽¹⁾ External op-amp connection mode			± 7	LSB
INL	Integral non-linearity error	$V_{REF} = V_{CC} = 5 \text{ V}$			± 3	LSB
		AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 ⁽¹⁾ External op-amp connection mode			± 7	LSB
DNL	Differential non-linearity error				± 1	LSB
—	Offset error				± 3	LSB
—	Gain error				± 3	LSB
R_{LADDER}	Resistor ladder	$V_{REF} = V_{CC}$	4		20	k Ω
t_{CONV}	Conversion time (10 bits)	$\phi_{AD} = 16 \text{ MHz}$, with sample and hold function	2.06			μs
		$\phi_{AD} = 16 \text{ MHz}$, without sample and hold function	3.69			μs
t_{CONV}	Conversion time (8 bits)	$\phi_{AD} = 16 \text{ MHz}$, with sample and hold function	1.75			μs
		$\phi_{AD} = 16 \text{ MHz}$, without sample and hold function	3.06			μs
t_{SAMP}	Sampling time	$\phi_{AD} = 16 \text{ MHz}$	0.188			μs
V_{IA}	Analog input voltage		0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function	0.25		16	MHz
		With sample and hold function	1		16	MHz

Note:

1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.

$$V_{CC} = 5\text{ V}$$

Timing Requirements ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.27 Timer B Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN input clock cycle time (one edge counting)	200		ns
$t_{W(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{W(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{C(TB)}$	TBiIN input clock cycle time (both edges counting)	200		ns
$t_{W(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{W(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.28 Timer B Input (pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN input clock cycle time	400		ns
$t_{W(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{W(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.29 Timer B Input (pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN input clock cycle time	400		ns
$t_{W(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{W(TBL)}$	TBiIN input low level pulse width	180		ns

$$V_{CC} = 3.3 \text{ V}$$

Table 5.43 Electrical Characteristics (3/3)(V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current	In single-chip mode, output pins are left open and others are connected to V _{SS}				
		f _(CPU) = 64 MHz, f _(BCLK) = 32 MHz, f _(XIN) = 8 MHz, Active: XIN, PLL, Stopped: XCIN, OCO		40	55	mA
		XIN-XOUT Drive strength: low		32	45	mA
		XCIN-XCOUT Drive strength: low				
		f _(CPU) = f _{SO(PLL)} /24 MHz, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO		9		mA
		f _(CPU) = f _(BCLK) = f _(XIN) /256 MHz, f _(XIN) = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO		670		μA
		f _(CPU) = f _(BCLK) = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown		180		μA
		f _(CPU) = f _(BCLK) = f _(OCO) /4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown		190		μA
		f _(CPU) = f _(BCLK) = f _(XIN) /256 MHz, f _(XIN) = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO, T _a = 25°C, Wait mode		500	900	μA
		f _(CPU) = f _(BCLK) = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, T _a = 25°C, Wait mode		8	140	μA
		f _(CPU) = f _(BCLK) = f _(OCO) /4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, T _a = 25°C, Wait mode		10	150	μA
		Stopped: all clocks, Main regulator: shutdown, T _a = 25°C		5	70	μA

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

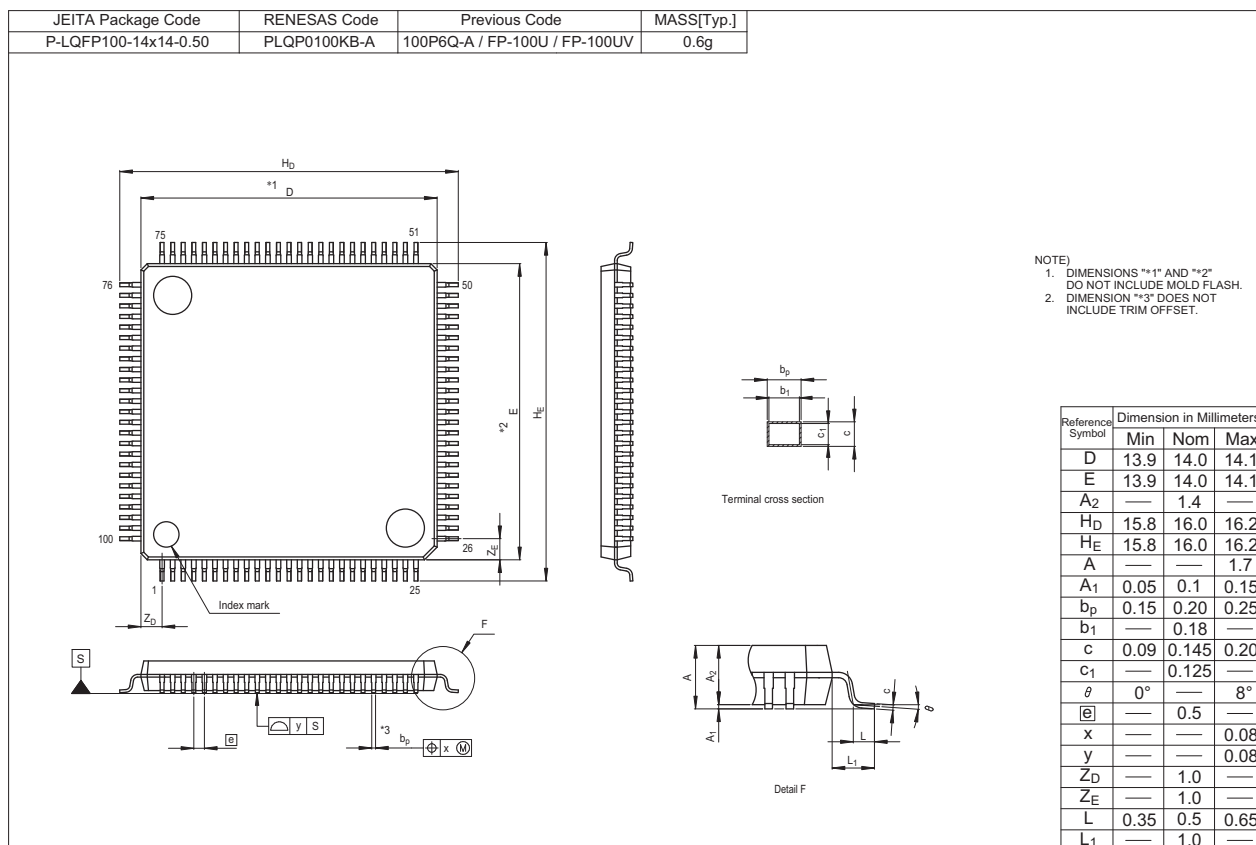
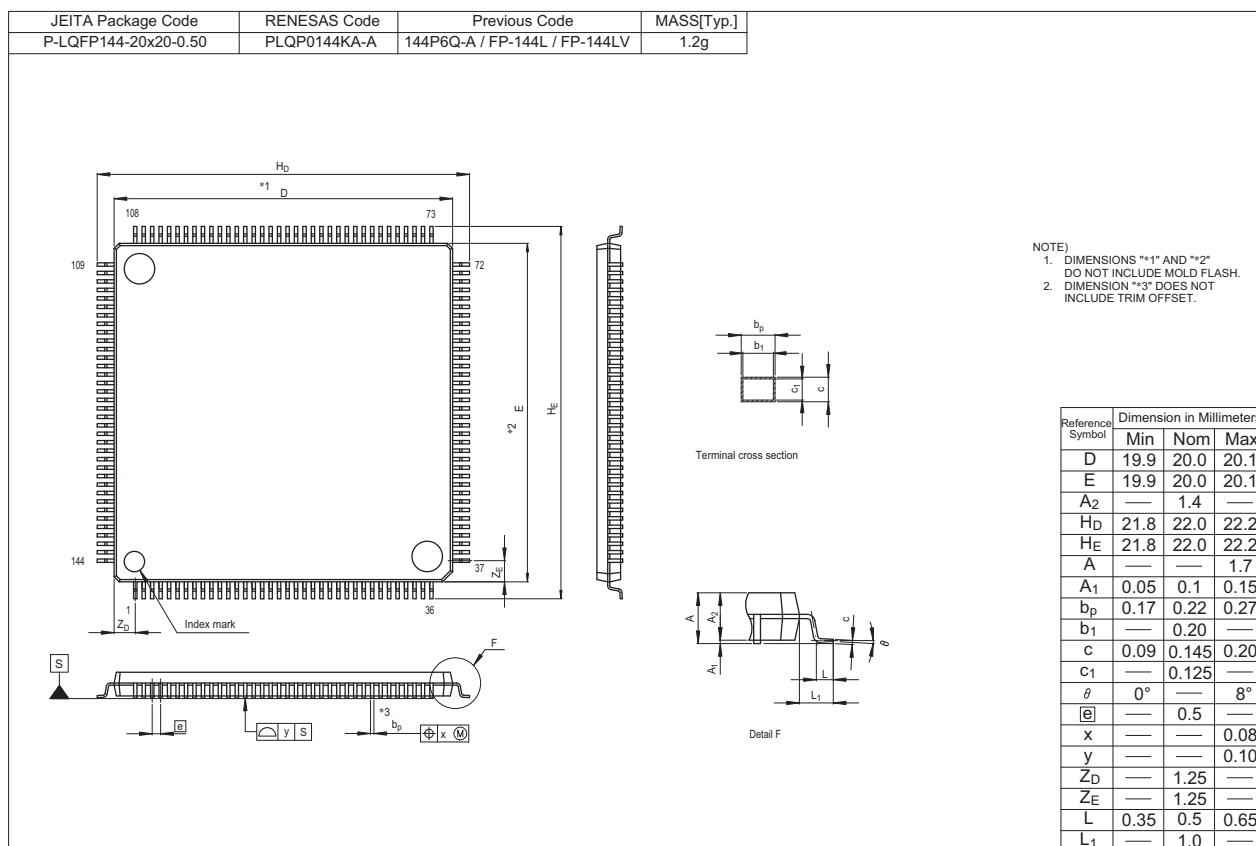
Table 5.46 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(X)}$	External clock input period	62.5	250	ns
$t_{W(XH)}$	External clock input high level pulse width	25		ns
$t_{W(XL)}$	External clock input low level pulse width	25		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_W / t_C	External clock input duty	40	60	%

Table 5.47 External Bus Timing

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{su(D-R)}$	Data setup time before read	40		ns
$t_{h(R-D)}$	Data hold time after read	0		ns
$t_{dis(R-D)}$	Data disable time after read		$0.5 \times t_{C(Base)} + 10$	ns

Appendix 1. Package Dimensions



Revision History	R32C/118 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Nov 19, 2009	—	Initial release
1.10	Jun 23, 2010	—	Second edition released
		—	This manual in general • Applied new Renesas templates and formats to the manual • Changed company name to “Renesas Electronics Corporation” and changed related descriptions due to business merger of Renesas Technology Corporation and NEC Electronics Corporation (under Chapters 1 and 5) • Added specifications of 64 MHz version
		3, 5	Chapter 1. Overview
		9	• Deleted Note 1 from Tables 1.2 and 1.4
		19	• Deleted Note 4 from Figure 1.2
			• Modified expression “fC” in Table 1.14 to “low speed clocks”
		34, 37	Chapter 4. SFRs
			• Changed register name “Group i Timer Measurement Prescaler Register” in Tables 4.6 and 4.9 to “Group i Time Measurement Prescaler Register”
		39	• Modified expression “XY Control Register” in Table 4.11 to “X-Y Control Register”
		41	• Changed register name “UART2 Transmission/Receive Mode Register” in Table 4.13 to “UART2 Transmit/Receive Mode Register”; Changed hexadecimal format of reset values for registers TABSR, ONSF, and TRGSR to binary
1.20	Feb 6, 2013	52	• Changed register name “External Interrupt Source Select Register i” in Table 4.24 to “External Interrupt Request Source Select Register i”
		67, 81	• Modified register names “CANi Reception Error Count Register” and “CANi Transmission Error Count Register” in Tables 4.39 and 4.53 to “CANi Receive Error Count Register” and “CANi Transmit Error Count Register”, respectively
		91	Chapter 5. Electrical Characteristics
			• Changed expressions “CS0” and “A23 to A0, BC3 to BC0” in Figure 5.5 to “Chip select” and “Address”, respectively
		123	Appendix 1. Package Dimensions
			• Added a seating plane to the drawing of package dimension
1.20	Feb 6, 2013	—	Third edition released
		—	This manual in general • Changed document number “REJ03B0255-0110” to “R01DS0065EJ0120” • Modified expressions “version N”, “version D”, and “version P” to “N version”, “D version”, and “P version”, respectively (under Chapters 1 and 5)
		—	Chapter 1. Overview
			• Modified wording and enhanced description in this chapter