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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	64MHz
Connectivity	CANbus, EBI/EMI, I ² C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	63K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64189hdfd-ua

Table 1.4 Performance Overview for the 100-pin Package (2/2)

Unit	Function	Explanation
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer
Serial Interface	UART0 to UART8	Asynchronous/synchronous serial interface × 9 channels • I ² C-bus (UART0 to UART6) • Special mode 2 (UART0 to UART6) • IEBus (optional ⁽¹⁾) (UART0 to UART6)
A/D Converter		10-bit resolution × 26 channels Sample and hold functionality integrated
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 16 Waveform generation (output compare): 16 bits × 19 Serial interface: Variable-length synchronous serial I/O mode, IEBus mode (optional ⁽¹⁾)
Multi-master I ² C-bus Interface		1 channel
CAN Module		2 channels CAN functionality compliant with ISO 11898-1 32 mailboxes
Flash Memory		Programming and erasure supply voltage: VCC = 3.0 to 5.5 V Minimum endurance: 1,000 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
Operating Frequency/Supply Voltage		64 MHz (high speed version)/VCC = 3.0 to 5.5 V 50 MHz (normal speed version)/VCC = 3.0 to 5.5 V
Operating Temperature		-20°C to 85°C (N version) -40°C to 85°C (D version) -40°C to 85°C (P version)
Current Consumption		45 mA (VCC = 5.0 V, f(CPU) = 64 MHz) 35 mA (VCC = 5.0 V, f(CPU) = 50 MHz) 8 μA (VCC = 3.3 V, f(XCIN) = 32.768 kHz, in wait mode)
Package		100-pin plastic molded LQFP (PLQP0100KB-A)

Note:

1. Contact a Renesas Electronics sales office to use the optional features.

Table 1.6 R32C/118 Group Product List for High Speed Version (2/2) As of February, 2013

Part Number	Package Code (1)	ROM Capacity (2)	RAM Capacity	Remarks
R5F64185HNFD (P)	PLQP0144KA-A	384 Kbytes + 8 Kbytes	40 Kbytes	-20°C to 85°C (N version)
R5F64185HDFD				-40°C to 85°C (D version)
R5F64185HPFD				-40°C to 85°C (P version)
R5F64185HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64185HDFB				-40°C to 85°C (D version)
R5F64185HPFB				-40°C to 85°C (P version)
R5F64186HNFD (P)	PLQP0144KA-A	512 Kbytes + 8 Kbytes	40 Kbytes	-20°C to 85°C (N version)
R5F64186HDFD				-40°C to 85°C (D version)
R5F64186HPFD				-40°C to 85°C (P version)
R5F64186HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64186HDFB				-40°C to 85°C (D version)
R5F64186HPFB				-40°C to 85°C (P version)
R5F64187HNFD (P)	PLQP0144KA-A	640 Kbytes + 8 Kbytes	48 Kbytes	-20°C to 85°C (N version)
R5F64187HDFD				-40°C to 85°C (D version)
R5F64187HPFD				-40°C to 85°C (P version)
R5F64187HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64187HDFB				-40°C to 85°C (D version)
R5F64187HPFB				-40°C to 85°C (P version)
R5F64188HNFD (P)	PLQP0144KA-A	768 Kbytes + 8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64188HDFD				-40°C to 85°C (D version)
R5F64188HPFD				-40°C to 85°C (P version)
R5F64188HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64188HDFB				-40°C to 85°C (D version)
R5F64188HPFB				-40°C to 85°C (P version)
R5F64189HNFD (P)	PLQP0144KA-A	1 Mbyte + 8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64189HDFD				-40°C to 85°C (D version)
R5F64189HPFD				-40°C to 85°C (P version)
R5F64189HNFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64189HDFB				-40°C to 85°C (D version)
R5F64189HPFB				-40°C to 85°C (P version)

(P): On planning phase

Notes:

- The old package codes are as follows:
PLQP0100KB-A: 100P6Q-A; PLQP0144KA-A: 144P6Q-A
- "8 Kbytes" in the ROM capacity indicates the data flash memory capacity.

Table 1.13 Pin Characteristics for the 100-pin Package (3/3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Module Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
76		P1_2				IIO0_2/IIO1_2		D10
77		P1_1				IIO0_1/IIO1_1		D9
78		P1_0				IIO0_0/IIO1_0		D8
79		P0_7					AN0_7	D7
80		P0_6					AN0_6	D6
81		P0_5					AN0_5	D5
82		P0_4					AN0_4	D4
83		P0_3					AN0_3	D3
84		P0_2					AN0_2	D2
85		P0_1					AN0_1	D1
86		P0_0					AN0_0	D0
87		P10_7	KI3				AN_7	
88		P10_6	KI2				AN_6	
89		P10_5	KI1				AN_5	
90		P10_4	KI0				AN_4	
91		P10_3					AN_3	
92		P10_2					AN_2	
93		P10_1					AN_1	
94	AVSS							
95		P10_0					AN_0	
96	VREF							
97	AVCC							
98		P9_7			RXD4/SCL4/STXD4		ADTRG	
99		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
100		P9_5			CLK4/CAN1IN/ CAN1WU		ANEX0	

Table 4.13 SFR List (13)

Address	Register	Symbol	Reset Value
000320h			
000321h			
000322h			
000323h			
000324h	UART3 Special Mode Register 4	U3SMR4	00h
000325h	UART3 Special Mode Register 3	U3SMR3	00h
000326h	UART3 Special Mode Register 2	U3SMR2	00h
000327h	UART3 Special Mode Register	U3SMR	00h
000328h	UART3 Transmit/Receive Mode Register	U3MR	00h
000329h	UART3 Bit Rate Register	U3BRG	XXh
00032Ah	UART3 Transmit Buffer Register	U3TB	XXXXh
00032Bh			
00032Ch	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
00032Dh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
00032Eh	UART3 Receive Buffer Register	U3RB	XXXXh
00032Fh			
000330h			
000331h			
000332h			
000333h			
000334h	UART2 Special Mode Register 4	U2SMR4	00h
000335h	UART2 Special Mode Register 3	U2SMR3	00h
000336h	UART2 Special Mode Register 2	U2SMR2	00h
000337h	UART2 Special Mode Register	U2SMR	00h
000338h	UART2 Transmit/Receive Mode Register	U2MR	00h
000339h	UART2 Bit Rate Register	U2BRG	XXh
00033Ah	UART2 Transmit Buffer Register	U2TB	XXXXh
00033Bh			
00033Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
00033Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
00033Eh	UART2 Receive Buffer Register	U2RB	XXXXh
00033Fh			
000340h	Count Start Register	TABSR	0000 0000b
000341h	Clock Prescaler Reset Register	CPSRF	0XXX XXXXb
000342h	One-shot Start Register	ONSF	0000 0000b
000343h	Trigger Select Register	TRGSR	0000 0000b
000344h	Increment/Decrement Select Register	UDF	0000 0000b
000345h			
000346h	Timer A0 Register	TA0	XXXXh
000347h			
000348h	Timer A1 Register	TA1	XXXXh
000349h			
00034Ah	Timer A2 Register	TA2	XXXXh
00034Bh			
00034Ch	Timer A3 Register	TA3	XXXXh
00034Dh			
00034Eh	Timer A4 Register	TA4	XXXXh
00034Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.19 SFR List (19)

Address	Register	Symbol	Reset Value
040030h to 04003Fh			
040040h			
040041h			
040042h			
040043h			
040044h	Processor Mode Register 0 ⁽¹⁾	PM0	1000 0000b (CNVSS pin = Low) 0000 0011b (CNVSS pin = High)
040045h			
040046h	System Clock Control Register 0	CM0	0000 1000b
040047h	System Clock Control Register 1	CM1	0010 0000b
040048h	Processor Mode Register 3	PM3	00h
040049h			
04004Ah	Protect Register	PRCR	XXXX X000b
04004Bh			
04004Ch	Protect Register 3	PRCR3	0000 0000b
04004Dh	Oscillator Stop Detection Register	CM2	00h
04004Eh			
04004Fh			
040050h			
040051h			
040052h			
040053h	Processor Mode Register 2	PM2	00h
040054h	Chip Select Output Pin Setting Register 0	CSOP0	1000 XXXXb
040055h	Chip Select Output Pin Setting Register 1	CSOP1	01X0 XXXXb
040056h	Chip Select Output Pin Setting Register 2	CSOP2	XXXX 0000b
040057h			
040058h			
040059h			
04005Ah	Low Speed Mode Clock Control Register	CM3	XXXX XX00b
04005Bh			
04005Ch			
04005Dh			
04005Eh			
04005Fh			
040060h	Voltage Regulator Control Register	VRCR	0000 0000b
040061h			
040062h	Low Voltage Detector Control Register	LVDC	0000 XX00b
040063h			
040064h	Detection Voltage Configuration Register	DVCR	0000 XXXXb
040065h			
040066h			
040067h			
040068h to 040093h			

X: Undefined

Blanks are reserved. No access is allowed.

Note:

1. The value in the PM0 register is retained even after a software reset or watchdog timer reset.

Table 4.20 SFR List (20)

Address	Register	Symbol	Reset Value
040094h			
040095h			
040096h			
040097h	Three-phase Output Buffer Control Register	IOBC	0XXX XXXXb
040098h	Input Function Select Register 0	IFS0	X000 0000b
040099h	Input Function Select Register 1	IFS1	XXXX X0X0b
04009Ah	Input Function Select Register 2	IFS2	0000 00X0b
04009Bh	Input Function Select Register 3	IFS3	XXXX XX00b
04009Ch			
04009Dh			
04009Eh			
04009Fh			
0400A0h	Port P0_0 Function Select Register	P0_0S	0XXX X000b
0400A1h	Port P1_0 Function Select Register	P1_0S	XXXX X000b
0400A2h	Port P0_1 Function Select Register	P0_1S	0XXX X000b
0400A3h	Port P1_1 Function Select Register	P1_1S	XXXX X000b
0400A4h	Port P0_2 Function Select Register	P0_2S	0XXX X000b
0400A5h	Port P1_2 Function Select Register	P1_2S	XXXX X000b
0400A6h	Port P0_3 Function Select Register	P0_3S	0XXX X000b
0400A7h	Port P1_3 Function Select Register	P1_3S	XXXX X000b
0400A8h	Port P0_4 Function Select Register	P0_4S	0XXX X000b
0400A9h	Port P1_4 Function Select Register	P1_4S	XXXX X000b
0400AAh	Port P0_5 Function Select Register	P0_5S	0XXX X000b
0400ABh	Port P1_5 Function Select Register	P1_5S	XXXX X000b
0400ACh	Port P0_6 Function Select Register	P0_6S	0XXX X000b
0400ADh	Port P1_6 Function Select Register	P1_6S	XXXX X000b
0400AEh	Port P0_7 Function Select Register	P0_7S	0XXX X000b
0400AFh	Port P1_7 Function Select Register	P1_7S	XXXX X000b
0400B0h	Port P2_0 Function Select Register	P2_0S	0XXX X000b
0400B1h	Port P3_0 Function Select Register	P3_0S	XXXX X000b
0400B2h	Port P2_1 Function Select Register	P2_1S	0XXX X000b
0400B3h	Port P3_1 Function Select Register	P3_1S	XXXX X000b
0400B4h	Port P2_2 Function Select Register	P2_2S	0XXX X000b
0400B5h	Port P3_2 Function Select Register	P3_2S	XXXX X000b
0400B6h	Port P2_3 Function Select Register	P2_3S	0XXX X000b
0400B7h	Port P3_3 Function Select Register	P3_3S	XXXX X000b
0400B8h	Port P2_4 Function Select Register	P2_4S	0XXX X000b
0400B9h	Port P3_4 Function Select Register	P3_4S	XXXX X000b
0400BAh	Port P2_5 Function Select Register	P2_5S	0XXX X000b
0400BBh	Port P3_5 Function Select Register	P3_5S	XXXX X000b
0400BCh	Port P2_6 Function Select Register	P2_6S	0XXX X000b
0400BDh	Port P3_6 Function Select Register	P3_6S	XXXX X000b
0400BEh	Port P2_7 Function Select Register	P2_7S	0XXX X000b
0400BFh	Port P3_7 Function Select Register	P3_7S	XXXX X000b

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.24 SFR List (24)

Address	Register	Symbol	Reset Value
044060h			
044061h			
044062h			
044063h			
044064h			
044065h			
044066h			
044067h			
044068h			
044069h			
04406Ah			
04406Bh			
04406Ch			
04406Dh	External Interrupt Request Source Select Register 1	IFSR1	X0XX X000b
04406Eh			
04406Fh	External Interrupt Request Source Select Register 0	IFSR0	0000 0000b
044070h	DMA0 Request Source Select Register 2	DM0SL2	XX00 0000b
044071h	DMA1 Request Source Select Register 2	DM1SL2	XX00 0000b
044072h	DMA2 Request Source Select Register 2	DM2SL2	XX00 0000b
044073h	DMA3 Request Source Select Register 2	DM3SL2	XX00 0000b
044074h			
044075h			
044076h			
044077h			
044078h	DMA0 Request Source Select Register	DM0SL	XXX0 0000b
044079h	DMA1 Request Source Select Register	DM1SL	XXX0 0000b
04407Ah	DMA2 Request Source Select Register	DM2SL	XXX0 0000b
04407Bh	DMA3 Request Source Select Register	DM3SL	XXX0 0000b
04407Ch			
04407Dh	Wake-up IPL Setting Register 2	RIPL2	XX0X 0000b
04407Eh			
04407Fh	Wake-up IPL Setting Register 1	RIPL1	XX0X 0000b
044080h			
044081h			
044082h			
044083h			
044084h			
044085h			
044086h			
044087h			
044088h			
044089h			
04408Ah			
04408Bh			
04408Ch			
04408Dh			
04408Eh			
04408Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.32 SFR List (32)

Address	Register	Symbol	Reset Value
047920h	CAN1 Mailbox 18: Message Identifier	C1MB18	XXXX XXXXh
047921h			
047922h			
047923h			
047924h			
047925h	CAN1 Mailbox 18: Data Length		XXh
047926h	CAN1 Mailbox 18: Data Field		XXXX XXXX XXXX XXXXh
047927h			
047928h			
047929h			
04792Ah			
04792Bh			
04792Ch			
04792Dh			
04792Eh	CAN1 Mailbox18: Time Stamp		XXXXh
04792Fh			
047930h	CAN1 Mailbox 19: Message Identifier	C1MB19	XXXX XXXXh
047931h			
047932h			
047933h			
047934h			
047935h	CAN1 Mailbox 19: Data Length		XXh
047936h	CAN1 Mailbox 19: Data Field		XXXX XXXX XXXX XXXXh
047937h			
047938h			
047939h			
04793Ah			
04793Bh			
04793Ch			
04793Dh			
04793Eh	CAN1 Mailbox 19: Time Stamp		XXXXh
04793Fh			
047940h	CAN1 Mailbox 20: Message Identifier	C1MB20	XXXX XXXXh
047941h			
047942h			
047943h			
047944h			
047945h	CAN1 Mailbox 20: Data Length		XXh
047946h	CAN1 Mailbox 20: Data Field		XXXX XXXX XXXX XXXXh
047947h			
047948h			
047949h			
04794Ah			
04794Bh			
04794Ch			
04794Dh			
04794Eh	CAN1 Mailbox 20: Time Stamp		XXXXh
04794Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.35 SFR List (35)

Address	Register	Symbol	Reset Value
0479B0h	CAN1 Mailbox 27: Message Identifier	C1MB27	XXXX XXXXh
0479B1h			
0479B2h			
0479B3h			
0479B4h			
0479B5h	CAN1 Mailbox 27: Data Length		XXh
0479B6h	CAN1 Mailbox 27: Data Field		XXXX XXXX XXXX XXXXh
0479B7h			
0479B8h			
0479B9h			
0479BAh			
0479BBh			
0479BCh			
0479BDh			
0479BEh	CAN1 Mailbox 27: Time Stamp		XXXXh
0479BFh			
0479C0h	CAN1 Mailbox 28: Message Identifier	C1MB28	XXXX XXXXh
0479C1h			
0479C2h			
0479C3h			
0479C4h			
0479C5h	CAN1 Mailbox 28: Data Length		XXh
0479C6h	CAN1 Mailbox 28: Data Field		XXXX XXXX XXXX XXXXh
0479C7h			
0479C8h			
0479C9h			
0479CAh			
0479CBh			
0479CCh			
0479CDh			
0479CEh	CAN1 Mailbox 28: Time Stamp		XXXXh
0479CFh			
0479D0h	CAN1 Mailbox 29: Message Identifier	C1MB29	XXXX XXXXh
0479D1h			
0479D2h			
0479D3h			
0479D4h			
0479D5h	CAN1 Mailbox 29: Data Length		XXh
0479D6h	CAN1 Mailbox 29: Data Field		XXXX XXXX XXXX XXXXh
0479D7h			
0479D8h			
0479D9h			
0479DAh			
0479DBh			
0479DCh			
0479DDh			
0479DEh	CAN1 Mailbox 29: Time Stamp		XXXXh
0479DFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.39 SFR List (39)

Address	Register	Symbol	Reset Value
047B40h	CAN1 Control Register	C1CTLR	0000 0101b
047B41h			0000 0000b
047B42h	CAN1 Status Register	C1STR	0000 0101b
047B43h			0000 0000b
047B44h	CAN1 Bit Configuration Register	C1BCR	00 0000h
047B45h			
047B46h			
047B47h	CAN1 Clock Select Register	C1CLKR	000X 0000b
047B48h	CAN1 Receive FIFO Control Register	C1RFCR	1000 0000b
047B49h	CAN1 Receive FIFO Pointer Control Register	C1RFPCR	XXh
047B4Ah	CAN1 Transmit FIFO Control Register	C1TFCR	1000 0000b
047B4Bh	CAN1 Transmit FIFO Pointer Control Register	C1TFPCR	XXh
047B4Ch	CAN1 Error Interrupt Enable Register	C1EIER	00h
047B4Dh	CAN1 Error Interrupt Factor Judge Register	C1EIFR	00h
047B4Eh	CAN1 Receive Error Count Register	C1RECR	00h
047B4Fh	CAN1 Transmit Error Count Register	C1TECR	00h
047B50h	CAN1 Error Code Store Register	C1ECSR	00h
047B51h	CAN1 Channel Search Support Register	C1CSSR	XXh
047B52h	CAN1 Mailbox Search Status Register	C1MSSR	1000 0000b
047B53h	CAN1 Mailbox Search Mode Register	C1MSMR	0000 0000b
047B54h	CAN1 Time Stamp Register	C1TSR	0000h
047B55h			
047B56h	CAN1 Acceptance Filter Support Register	C1AFSR	XXXXh
047B57h			
047B58h	CAN1 Test Control Register	C1TCR	00h
047B59h			
047B5Ah			
047B5Bh			
047B5Ch			
047B5Dh			
047B5Eh			
047B5Fh			
047B60h to 047BFFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.45 SFR List (45)

Address	Register	Symbol	Reset Value
047CF0h	CAN0 Mailbox 15: Message Identifier	C0MB15	XXXX XXXXh
047CF1h			
047CF2h			
047CF3h			
047CF4h			
047CF5h	CAN0 Mailbox 15: Data Length		XXh
047CF6h	CAN0 Mailbox 15: Data Field		XXXX XXXX XXXX XXXXh
047CF7h			
047CF8h			
047CF9h			
047CFAh			
047CFBh			
047CFCh			
047CFDh			
047CFEh	CAN0 Mailbox 15: Time Stamp		XXXXh
047CFFh			
047D00h	CAN0 Mailbox 16: Message Identifier	C0MB16	XXXX XXXXh
047D01h			
047D02h			
047D03h			
047D04h			
047D05h	CAN0 Mailbox 16: Data Length		XXh
047D06h	CAN0 Mailbox 16: Data Field		XXXX XXXX XXXX XXXXh
047D07h			
047D08h			
047D09h			
047D0Ah			
047D0Bh			
047D0Ch			
047D0Dh			
047D0Eh	CAN0 Mailbox 16: Time Stamp		XXXXh
047D0Fh			
047D10h	CAN0 Mailbox 17: Message Identifier	C0MB17	XXXX XXXXh
047D11h			
047D12h			
047D13h			
047D14h			
047D15h	CAN0 Mailbox 17: Data Length		XXh
047D16h	CAN0 Mailbox 17: Data Field		XXXX XXXX XXXX XXXXh
047D17h			
047D18h			
047D19h			
047D1Ah			
047D1Bh			
047D1Ch			
047D1Dh			
047D1Eh	CAN0 Mailbox 17: Time Stamp		XXXXh
047D1Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.49 SFR List (49)

Address	Register	Symbol	Reset Value
047DB0h	CAN0 Mailbox 27: Message Identifier	C0MB27	XXXX XXXXh
047DB1h			
047DB2h			
047DB3h			
047DB4h			
047DB5h	CAN0 Mailbox 27: Data Length		XXh
047DB6h	CAN0 Mailbox 27: Data Field		XXXX XXXX XXXX XXXXh
047DB7h			
047DB8h			
047DB9h			
047DBAh			
047DBBh			
047DBCh			
047DBDh			
047DBEh	CAN0 Mailbox 27: Time Stamp		XXXXh
047DBFh			
047DC0h	CAN0 Mailbox 28: Message Identifier	C0MB28	XXXX XXXXh
047DC1h			
047DC2h			
047DC3h			
047DC4h			
047DC5h	CAN0 Mailbox 28: Data Length		XXh
047DC6h	CAN0 Mailbox 28: Data Field		XXXX XXXX XXXX XXXXh
047DC7h			
047DC8h			
047DC9h			
047DCAh			
047DCBh			
047DCCCh			
047DCDh			
047DCEh	CAN0 Mailbox 28: Time Stamp		XXXXh
047DCFh			
047DD0h	CAN0 Mailbox 29: Message Identifier	C0MB29	XXXX XXXXh
047DD1h			
047DD2h			
047DD3h			
047DD4h			
047DD5h	CAN0 Mailbox 29: Data Length		XXh
047DD6h	CAN0 Mailbox 29: Data Field		XXXX XXXX XXXX XXXXh
047DD7h			
047DD8h			
047DD9h			
047DDAh			
047DDBh			
047DDCh			
047DDDh			
047DDEh	CAN0 Mailbox 29: Time Stamp		XXXXh
047DDFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.51 SFR List (51)

Address	Register	Symbol	Reset Value
047E10h	CAN0 Mask Register 4	C0MKR4	XXXX XXXXh
047E11h			
047E12h			
047E13h			
047E14h	CAN0 Mask Register 5	C0MKR5	XXXX XXXXh
047E15h			
047E16h			
047E17h			
047E18h	CAN0 Mask Register 6	C0MKR6	XXXX XXXXh
047E19h			
047E1Ah			
047E1Bh			
047E1Ch	CAN0 Mask Register 7	C0MKR7	XXXX XXXXh
047E1Dh			
047E1Eh			
047E1Fh			
047E20h	CAN0 FIFO Receive ID Compare Register 0	C0FIDCR0	XXXX XXXXh
047E21h			
047E22h			
047E23h			
047E24h	CAN0 FIFO Receive ID Compare Register 1	C0FIDCR1	XXXX XXXXh
047E25h			
047E26h			
047E27h			
047E28h	CAN0 Mask Invalid Register	C0MKIVLR	XXXX XXXXh
047E29h			
047E2Ah			
047E2Bh			
047E2Ch	CAN0 Mailbox Interrupt Enable Register	C0MIER	XXXX XXXXh
047E2Dh			
047E2Eh			
047E2Fh			
047E30h			
047E31h			
047E32h			
047E33h			
047E34h			
047E35h			
047E36h			
047E37h			
047E38h			
047E39h			
047E3Ah			
047E3Bh			
047E3Ch			
047E3Dh			
047E3Eh			
047E3Fh			
047E40h to 047F1Fh			

X: Undefined

Blanks are reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings ⁽¹⁾

Symbol	Characteristic		Condition	Value	Unit
V _{CC}	Supply voltage		V _{CC} = AV _{CC}	-0.3 to 6.0	V
AV _{CC}	Analog supply voltage		V _{CC} = AV _{CC}	-0.3 to 6.0	V
V _I	Input voltage	XIN, RESET, CNVSS, NSD, V _{REF} , P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_1, P14_3 to P14_6, P15_0 to P15_7 ⁽²⁾		-0.3 to V _{CC} + 0.3	V
		P4_0 to P4_7, P5_4 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_3		-0.3 to 6.0	V
V _O	Output voltage	XOUT, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 ⁽²⁾		-0.3 to V _{CC} + 0.3	V
P _d	Power consumption		T _a = 25°C	500	mW
—	Operating temperature range			-40 to 85	°C
T _{stg}	Storage temperature range			-65 to 150	°C

Notes:

- Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

Table 5.2 Operating Conditions (1/5) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
V_{CC}	Digital supply voltage		3.0	5.0	5.5	V
AV_{CC}	Analog supply voltage			V_{CC}		V
V_{REF}	Reference voltage		3.0		V_{CC}	V
V_{SS}	Digital ground voltage			0		V
AV_{SS}	Analog ground voltage			0		V
dV_{CC}/dt	V_{CC} ramp up rate ($V_{CC} < 2.0$ V)		0.05			V/ms
V_{IH}	High level input voltage	XIN, $\overline{RESET}$, CNVSS, NSD, P2_0 to P2_7, P3_0 to P3_7, P5_0 to P5_3, P8_4 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P14_1, P14_3 to P14_6, P15_0 to P15_7 (3)	$0.8 \times V_{CC}$		V_{CC}	V
		P4_0 to P4_7, P5_4 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_3	$0.8 \times V_{CC}$		6.0	V
		P0_0 to P0_7, P1_0 to P1_7, in single-chip mode	$0.8 \times V_{CC}$		V_{CC}	V
		P12_0 to P12_7, P13_0 to P13_7 (3), in memory expansion mode or microprocessor mode	$0.5 \times V_{CC}$		V_{CC}	V
V_{IL}	Low level input voltage	XIN, $\overline{RESET}$, CNVSS, NSD, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 (2), P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P14_1, P14_3 to P14_6, P15_0 to P15_7 (3)	0		$0.2 \times V_{CC}$	V
		P0_0 to P0_7, P1_0 to P1_7, in single-chip mode	0		$0.2 \times V_{CC}$	V
		P12_0 to P12_7, P13_0 to P13_7 (3), in memory expansion mode or microprocessor mode	0		$0.16 \times V_{CC}$	V
T_{opr}	Operating temperature range	N version	-20		85	°C
		D version	-40		85	°C
		P version	-40		85	°C

Notes:

1. The device is operationally guaranteed under these operating conditions.
2. V_{IH} and V_{IL} for P8_7 are specified for P8_7 as a programmable port. These values are not applicable for P8_7 as XCIN.
3. Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

Table 5.9 Power Supply Circuit Timing Characteristics
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply start-up stabilization time after the main power supply is turned on				2	ms

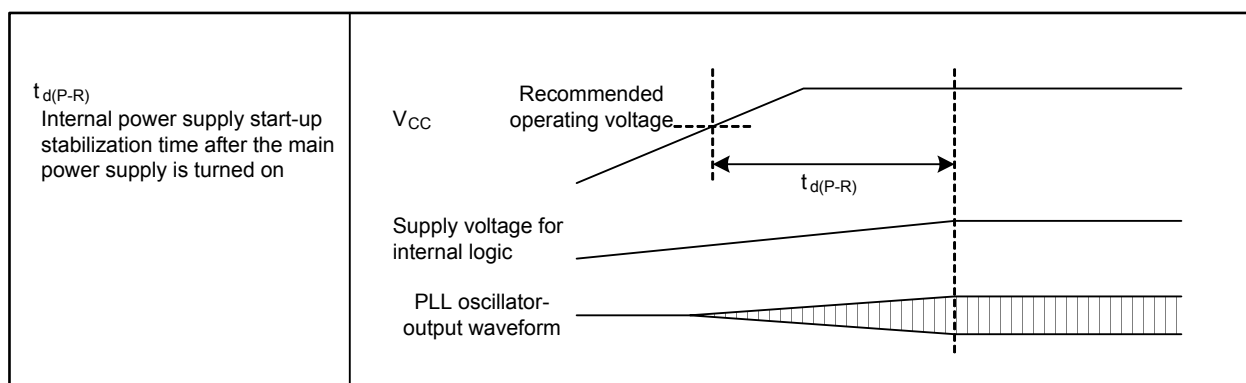


Figure 5.3 Power Supply Circuit Timing

Table 5.10 Electrical Characteristics of Voltage Regulator for Internal Logic
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
V_{VDC1}	Output voltage			1.5		V

Table 5.11 Electrical Characteristics of Low Voltage Detector
($V_{CC} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
ΔV_{det}	Detected voltage error				± 0.3	V
$V_{det(R)} - V_{det(F)}$	Hysteresis width		0			V
—	Self-consuming current	$V_{CC} = 5.0$ V, low voltage detector enabled		4		μA
$t_{d(E-A)}$	Operation start time of low voltage detector				150	μs

$$V_{CC} = 5 \text{ V}$$

Table 5.15 Electrical Characteristics (1/3)(V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V, T_a = T_{opr}, and f_(CPU) = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
V _{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	I _{OH} = -5 mA	V _{CC} - 2.0		V _{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	I _{OH} = -200 μA	V _{CC} - 0.3		V _{CC}	V
V _{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	I _{OL} = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_3 to P14_6, P15_0 to P15_7 (1)	I _{OL} = 200 μA			0.45	V

Note:

- Ports P9_0, P9_2, and P11 to P15 are available in the 144-pin package only. Port P9_1 is designated as input pin in the 100-pin package.

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.46 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(X)}$	External clock input period	62.5	250	ns
$t_{W(XH)}$	External clock input high level pulse width	25		ns
$t_{W(XL)}$	External clock input low level pulse width	25		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_W / t_C	External clock input duty	40	60	%

Table 5.47 External Bus Timing

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{su(D-R)}$	Data setup time before read	40		ns
$t_{h(R-D)}$	Data hold time after read	0		ns
$t_{dis(R-D)}$	Data disable time after read		$0.5 \times t_{C(Base)} + 10$	ns

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.48 Timer A Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.49 Timer A Input (gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.50 Timer A Input (external trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.51 Timer A Input (external trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.52 Timer A Input (increment/decrement switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_h(TIN-UP)$	TAiOUT input hold time	400		ns

Revision History	R32C/118 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Nov 19, 2009	—	Initial release
1.10	Jun 23, 2010	—	Second edition released
		—	This manual in general • Applied new Renesas templates and formats to the manual • Changed company name to “Renesas Electronics Corporation” and changed related descriptions due to business merger of Renesas Technology Corporation and NEC Electronics Corporation (under Chapters 1 and 5) • Added specifications of 64 MHz version
		3, 5 9 19	Chapter 1. Overview
			• Deleted Note 1 from Tables 1.2 and 1.4
			• Deleted Note 4 from Figure 1.2
			• Modified expression “fC” in Table 1.14 to “low speed clocks”
		34, 37 39 41 52 67, 81	Chapter 4. SFRs
			• Changed register name “Group i Timer Measurement Prescaler Register” in Tables 4.6 and 4.9 to “Group i Time Measurement Prescaler Register”
			• Modified expression “XY Control Register” in Table 4.11 to “X-Y Control Register”
			• Changed register name “UART2 Transmission/Receive Mode Register” in Table 4.13 to “UART2 Transmit/Receive Mode Register”; Changed hexadecimal format of reset values for registers TABSR, ONSF, and TRGSR to binary
			• Changed register name “External Interrupt Source Select Register i” in Table 4.24 to “External Interrupt Request Source Select Register i”
			• Modified register names “CANi Reception Error Count Register” and “CANi Transmission Error Count Register” in Tables 4.39 and 4.53 to “CANi Receive Error Count Register” and “CANi Transmit Error Count Register”, respectively
		91	Chapter 5. Electrical Characteristics
			• Changed expressions “CS0” and “A23 to A0, BC3 to BC0” in Figure 5.5 to “Chip select” and “Address”, respectively
		123	Appendix 1. Package Dimensions
			• Added a seating plane to the drawing of package dimension
1.20	Feb 6, 2013	—	Third edition released
		—	This manual in general • Changed document number “REJ03B0255-0110” to “R01DS0065EJ0120” • Modified expressions “version N”, “version D”, and “version P” to “N version”, “D version”, and “P version”, respectively (under Chapters 1 and 5)
		—	Chapter 1. Overview • Modified wording and enhanced description in this chapter