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Details

Product Status	Active
Core Processor	R32C/100
Core Size	16/32-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I ² C, IEBus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	63K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f64189pfd-ub

1.2 Product Information

Tables 1.5 and 1.6 list the product information and Figure 1.1 shows the details of the part number.

Table 1.5 R32C/118 Group Product List for Normal Speed Version (1/2) As of February, 2013

Part Number	Package Code ⁽¹⁾	ROM Capacity ⁽²⁾	RAM Capacity	Remarks
R5F64185NFD (P)	PLQP0144KA-A	384 Kbytes + 8 Kbytes	40 Kbytes	-20°C to 85°C (N version)
R5F64185DFD				-40°C to 85°C (D version)
R5F64185PFD				-40°C to 85°C (P version)
R5F64185NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64185DFB				-40°C to 85°C (D version)
R5F64185PFB				-40°C to 85°C (P version)
R5F64186NFD (P)	PLQP0144KA-A	-20°C to 85°C (N version)		
R5F64186DFD		-40°C to 85°C (D version)		
R5F64186PFD		-40°C to 85°C (P version)		
R5F64186NFB (P)	PLQP0100KB-A	-20°C to 85°C (N version)		
R5F64186DFB		-40°C to 85°C (D version)		
R5F64186PFB		-40°C to 85°C (P version)		
R5F64187NFD (P)	PLQP0144KA-A	640 Kbytes + 8 Kbytes	48 Kbytes	-20°C to 85°C (N version)
R5F64187DFD				-40°C to 85°C (D version)
R5F64187PFD				-40°C to 85°C (P version)
R5F64187NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64187DFB				-40°C to 85°C (D version)
R5F64187PFB				-40°C to 85°C (P version)
R5F64188NFD (P)	PLQP0144KA-A	768 Kbytes + 8 Kbytes	63 Kbytes	-20°C to 85°C (N version)
R5F64188DFD				-40°C to 85°C (D version)
R5F64188PFD				-40°C to 85°C (P version)
R5F64188NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64188DFB				-40°C to 85°C (D version)
R5F64188PFB				-40°C to 85°C (P version)
R5F64189NFD (P)	PLQP0144KA-A	1 Mbyte + 8 Kbytes		-20°C to 85°C (N version)
R5F64189DFD				-40°C to 85°C (D version)
R5F64189PFD				-40°C to 85°C (P version)
R5F64189NFB (P)	PLQP0100KB-A			-20°C to 85°C (N version)
R5F64189DFB				-40°C to 85°C (D version)
R5F64189PFB				-40°C to 85°C (P version)

(P): On planning phase

Notes:

- The old package codes are as follows:
PLQP0100KB-A: 100P6Q-A; PLQP0144KA-A: 144P6Q-A
- "8 Kbytes" in the ROM capacity indicates the data flash memory capacity.

Table 1.10 Pin Characteristics for the 144-pin Package (4/4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Module Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
115		P11_3			CTS8/RTS8	IIO1_3		CS3/WR2
116		P11_2			RXD8	IIO1_2		CS2
117		P11_1			CLK8	IIO1_1		CS1
118		P11_0			TXD8	IIO1_0		CS0
119		P0_3					AN0_3	D3
120		P0_2					AN0_2	D2
121		P0_1					AN0_1	D1
122		P0_0					AN0_0	D0
123		P15_7			CTS6/RTS6/SS6	IIO0_7	AN15_7	
124		P15_6			CLK6	IIO0_6	AN15_6	
125		P15_5			RXD6/SCL6/STXD6	IIO0_5	AN15_5	
126		P15_4			TXD6/SDA6/SRXD6	IIO0_4	AN15_4	
127		P15_3			CTS7/RTS7	IIO0_3	AN15_3	
128		P15_2			RXD7	IIO0_2	AN15_2	
129		P15_1			CLK7	IIO0_1	AN15_1	
130	VSS							
131		P15_0			TXD7	IIO0_0	AN15_0	
132	VCC							
133		P10_7	KI3				AN_7	
134		P10_6	KI2				AN_6	
135		P10_5	KI1				AN_5	
136		P10_4	KI0				AN_4	
137		P10_3					AN_3	
138		P10_2					AN_2	
139		P10_1					AN_1	
140	AVSS							
141		P10_0					AN_0	
142	VREF							
143	AVCC							
144		P9_7			RXD4/SCL4/STXD4		ADTRG	

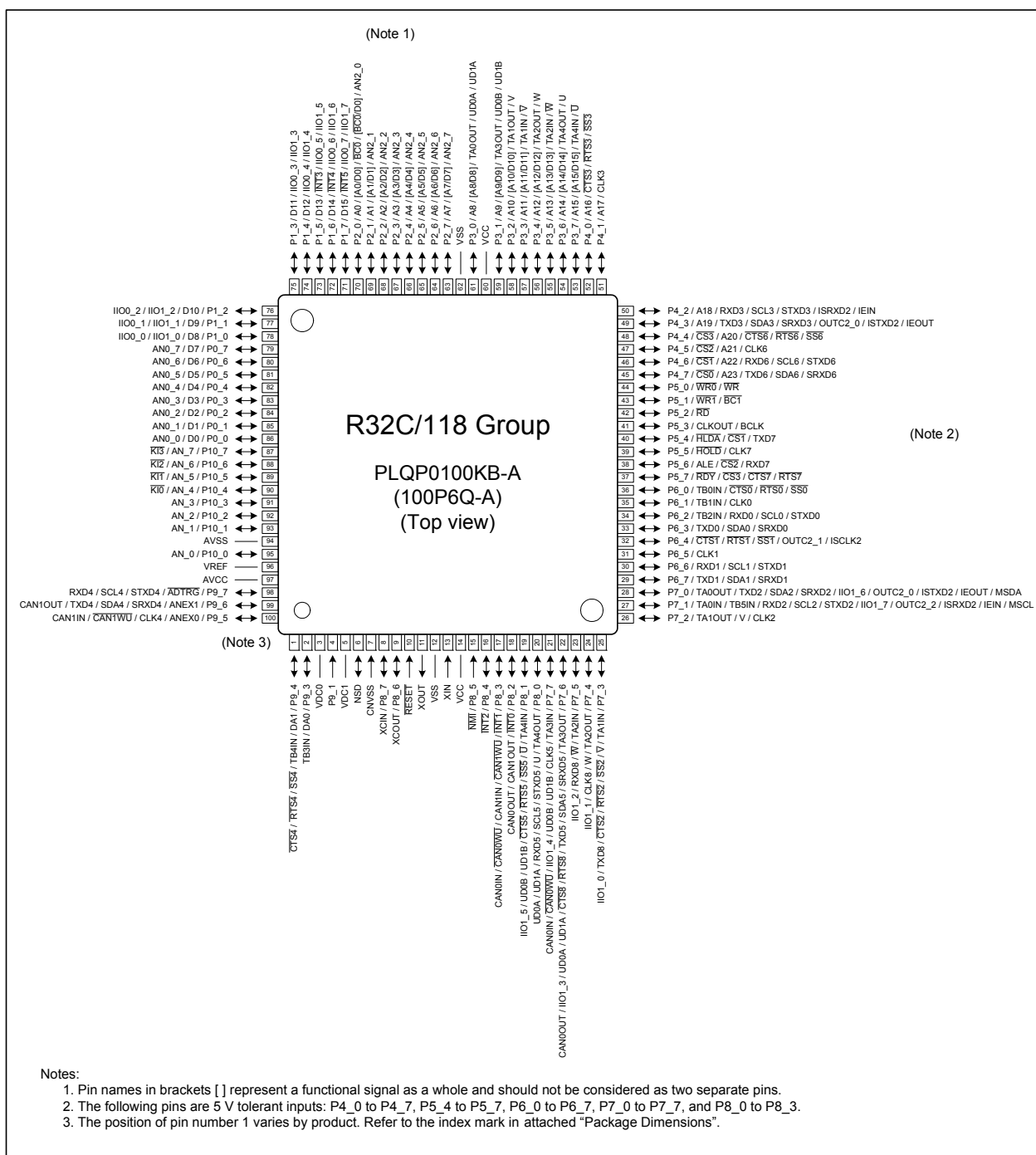


Figure 1.4 Pin Assignment for the 100-pin Package (top view)

Table 1.11 Pin Characteristics for the 100-pin Package (1/3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Module Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
2		P9_3		TB3IN			DA0	
3	VDC0							
4		P9_1						
5	VDC1							
6	NSD							
7	CNVSS							
8	XCIN	P8_7						
9	XCOUT	P8_6						
10	RESET							
11	XOUT							
12	VSS							
13	XIN							
14	VCC							
15		P8_5	NMI					
16		P8_4	INT2					
17		P8_3	INT1		CAN0IN/CAN0WU/ CAN1IN/CAN1WU			
18		P8_2	INT0		CAN0OUT/CAN1OUT			
19		P8_1		TA4IN/U	CTS5/RTS5/SS5	IIO1_5/UD0B/UD1B		
20		P8_0		TA4OUT/U	RXD5/SCL5/STXD5	UD0A/UD1A		
21		P7_7		TA3IN	CLK5/CAN0IN/ CAN0WU	IIO1_4/UD0B/UD1B		
22		P7_6		TA3OUT	TXD5/SDA5/SRXD5/ CTS8/RTS8/CAN0OUT	IIO1_3/UD0A/UD1A		
23		P7_5		TA2IN/W	RXD8	IIO1_2		
24		P7_4		TA2OUT/W	CLK8	IIO1_1		
25		P7_3		TA1IN/V	CTS2/RTS2/SS2/TXD8	IIO1_0		
26		P7_2		TA1OUT/V	CLK2			
27		P7_1		TA0IN/ TB5IN	RXD2/SCL2/STXD2/ MSCL	IIO1_7/OUTC2_2/ ISRXD2/IEIN		
28		P7_0		TA0OUT	TXD2/SDA2/SRXD2/ MSDA	IIO1_6/OUTC2_0/ ISTXD2/IEOUT		
29		P6_7			TXD1/SDA1/SRXD1			
30		P6_6			RXD1/SCL1/STXD1			
31		P6_5			CLK1			
32		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
33		P6_3			TXD0/SDA0/SRXD0			
34		P6_2		TB2IN	RXD0/SCL0/STXD0			
35		P6_1		TB1IN	CLK0			
36		P6_0		TB0IN	CTS0/RTS0/SS0			
37		P5_7			CTS7/RTS7			RDY/CS3
38		P5_6			RXD7			ALE/CS2

2.1 General Purpose Registers

2.1.1 Data Registers (R2R0, R3R1, R6R4, and R7R5)

These 32-bit registers are primarily used for transfers and arithmetic/logic operations.

Each of the registers can be divided into upper and lower 16-bit registers, e.g. R2R0 can be divided into R2 and R0, R3R1 can be divided into R3 and R1, etc.

Moreover, data registers R2R0 and R3R1 can be divided into four 8-bit data registers: upper (R2H and R3H), mid-upper (R2L and R3L), mid-lower (R0H and R1H), and lower (R0L and R1L).

2.1.2 Address Registers (A0, A1, A2, and A3)

These 32-bit registers have functions similar to data registers. They are also used for address register indirect addressing and address register relative addressing.

2.1.3 Static Base Register (SB)

This 32-bit register is used for SB relative addressing.

2.1.4 Frame Base Register (FB)

This 32-bit register is used for FB relative addressing.

2.1.5 Program Counter (PC)

This 32-bit counter indicates the address of the instruction to be executed next.

2.1.6 Interrupt Vector Table Base Register (INTB)

This 32-bit register indicates the start address of a relocatable vector table.

2.1.7 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Two types of 32-bit stack pointers (SPs) are provided: user stack pointer (USP) and interrupt stack pointer (ISP).

Use the stack pointer select flag (U flag) to select either the user stack pointer (USP) or the interrupt stack pointer (ISP). The U flag is bit 7 in the flag register (FLG). Refer to 2.1.8 "Flag Register (FLG)" for details.

To minimize the overhead of interrupt sequence due to less memory access, set the user stack pointer (USP) or the interrupt stack pointer (ISP) to a multiple of 4.

2.1.8 Flag Register (FLG)

This 32-bit register indicates the CPU status.

2.1.8.1 Carry Flag (C flag)

This flag retains a carry, borrow, or shifted-out bit generated by the arithmetic logic unit (ALU).

2.1.8.2 Debug Flag (D flag)

This flag is only for debugging. Only set this bit to 0.

2.1.8.3 Zero Flag (Z flag)

This flag becomes 1 when the result of an operation is 0; otherwise it is 0.

2.1.8.4 Sign Flag (S flag)

This flag becomes 1 when the result of an operation is a negative value; otherwise it is 0.

2.1.8.5 Register Bank Select Flag (B flag)

This flag selects a register bank. It indicates 0 when register bank 0 is selected, and 1 when register bank 1 is selected.

2.1.8.6 Overflow Flag (O flag)

This flag becomes 1 when the result of an operation overflows; otherwise it is 0.

2.1.8.7 Interrupt Enable Flag (I flag)

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

2.1.8.8 Stack Pointer Select Flag (U flag)

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.

It becomes 0 when a hardware interrupt is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

2.1.8.9 Floating-point Underflow Flag (FU flag)

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.10 Floating-point Overflow Flag (FO flag)

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.11 Processor Interrupt Priority Level (IPL)

The processor interrupt priority level (IPL), consisting of 3 bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is enabled when the interrupt request level is higher than the selected IPL.

When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to extract. It is used for the MULX instruction.

2.1.8.13 Floating-point Rounding Mode (RND)

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

2.1.8.14 Reserved

Only set this bit to 0. The read value is undefined.

2.2 Fast Interrupt Registers

The following three registers are provided to minimize the overhead of the interrupt sequence.

2.2.1 Save Flag Register (SVF)

This 32-bit register is used to save the flag register when a fast interrupt occurs.

2.2.2 Save PC Register (SVP)

This 32-bit register is used to save the program counter when a fast interrupt occurs.

2.2.3 Vector Register (VCT)

This 32-bit register is used to indicate a jump address when a fast interrupt occurs.

2.3 DMAC-associated Registers

There are seven types of DMAC-associated registers.

2.3.1 DMA Mode Registers (DMD0, DMD1, DMD2, and DMD3)

These 32-bit registers are used to set DMA transfer mode, bit rate, etc.

2.3.2 DMA Terminal Count Registers (DCT0, DCT1, DCT2, and DCT3)

These 24-bit registers are used to set the number of DMA transfers.

2.3.3 DMA Terminal Count Reload Registers (DCR0, DCR1, DCR2, and DCR3)

These 24-bit registers are used to set the reloaded values for DMA terminal count registers.

2.3.4 DMA Source Address Registers (DSA0, DSA1, DSA2, and DSA3)

These 32-bit registers are used to set DMA source addresses.

2.3.5 DMA Source Address Reload Registers (DSR0, DSR1, DSR2, and DSR3)

These 32-bit registers are used to set the reloaded values for DMA source address registers.

2.3.6 DMA Destination Address Registers (DDA0, DDA1, DDA2, and DDA3)

These 32-bit registers are used to set DMA destination addresses.

2.3.7 DMA Destination Address Reload Registers (DDR0, DDR1, DDR2, and DDR3)

These 32-bit registers are used to set reloaded values for DMA destination address registers.

4. Special Function Registers (SFRs)

SFRs are memory-mapped peripheral registers that control the operation of peripherals. Table 4.1 SFR List (1) to Table 4.53 SFR List (53) list the SFR details.

Table 4.1 SFR List (1)

Address	Register	Symbol	Reset Value
000000h			
000001h			
000002h			
000003h			
000004h	Clock Control Register	CCR	0001 1000b
000005h			
000006h	Flash Memory Control Register	FMCR	0000 0001b
000007h	Protect Release Register	PRR	00h
000008h			
000009h			
00000Ah			
00000Bh			
00000Ch			
00000Dh			
00000Eh			
00000Fh			
000010h	External Bus Control Register 3/Flash Memory Rewrite Bus	EBC3/FEBC3	0000h
000011h	Control Register 3		
000012h	Chip Selects 2 and 3 Boundary Setting Register	CB23	00h
000013h			
000014h	External Bus Control Register 2	EBC2	0000h
000015h			
000016h	Chip Selects 1 and 2 Boundary Setting Register	CB12	00h
000017h			
000018h	External Bus Control Register 1	EBC1	0000h
000019h			
00001Ah	Chip Selects 0 and 1 Boundary Setting Register	CB01	00h
00001Bh			
00001Ch	External Bus Control Register 0/Flash Memory Rewrite Bus	EBC0/FEBC0	0000h
00001Dh	Control Register 0		
00001Eh	Peripheral Bus Control Register	PBC	0504h
00001Fh			
000020h to 00005Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.12 SFR List (12)

Address	Register	Symbol	Reset Value
0002F0h			
0002F1h			
0002F2h			
0002F3h			
0002F4h	UART4 Special Mode Register 4	U4SMR4	00h
0002F5h	UART4 Special Mode Register 3	U4SMR3	00h
0002F6h	UART4 Special Mode Register 2	U4SMR2	00h
0002F7h	UART4 Special Mode Register	U4SMR	00h
0002F8h	UART4 Transmit/Receive Mode Register	U4MR	00h
0002F9h	UART4 Bit Rate Register	U4BRG	XXh
0002FAh	UART4 Transmit Buffer Register	U4TB	XXXXh
0002FBh			
0002FCh	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
0002FDh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
0002FEh	UART4 Receive Buffer Register	U4RB	XXXXh
0002FFh			
000300h	Count Start Register for Timers B3, B4, and B5	TBSR	000X XXXXb
000301h			
000302h	Timer A1-1 Register	TA11	XXXXh
000303h			
000304h	Timer A2-1 Register	TA21	XXXXh
000305h			
000306h	Timer A4-1 Register	TA41	XXXXh
000307h			
000308h	Three-phase PWM Control Register 0	INVC0	00h
000309h	Three-phase PWM Control Register 1	INVC1	00h
00030Ah	Three-phase Output Buffer Register 0	IDB0	XX11 1111b
00030Bh	Three-phase Output Buffer Register 1	IDB1	XX11 1111b
00030Ch	Dead Time Timer	DTT	XXh
00030Dh	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XXh
00030Eh			
00030Fh			
000310h	Timer B3 Register	TB3	XXXXh
000311h			
000312h	Timer B4 Register	TB4	XXXXh
000313h			
000314h	Timer B5 Register	TB5	XXXXh
000315h			
000316h			
000317h			
000318h			
000319h			
00031Ah			
00031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
00031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
00031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
00031Eh			
00031Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.17 SFR List (17)

Address	Register	Symbol	Reset Value
0003E0h			
0003E1h			
0003E2h			
0003E3h			
0003E4h			
0003E5h			
0003E6h			
0003E7h			
0003E8h			
0003E9h			
0003EAh			
0003EBh			
0003ECh			
0003EDh			
0003EEh			
0003EFh			
0003F0h	Pull-up Control Register 0	PUR0	0000 0000b
0003F1h	Pull-up Control Register 1	PUR1	XXXX X0XXb
0003F2h	Pull-up Control Register 2	PUR2	000X XXXXb
0003F3h	Pull-up Control Register 3	PUR3	0000 0000b
0003F4h	Pull-up Control Register 4	PUR4	XXXX 0000b
0003F5h			
0003F6h			
0003F7h			
0003F8h			
0003F9h			
0003FAh			
0003FBh			
0003FCh			
0003FDh			
0003FEh			
0003FFh	Port Control Register	PCR	0XXX XXX0b

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.24 SFR List (24)

Address	Register	Symbol	Reset Value
044060h			
044061h			
044062h			
044063h			
044064h			
044065h			
044066h			
044067h			
044068h			
044069h			
04406Ah			
04406Bh			
04406Ch			
04406Dh	External Interrupt Request Source Select Register 1	IFSR1	X0XX X000b
04406Eh			
04406Fh	External Interrupt Request Source Select Register 0	IFSR0	0000 0000b
044070h	DMA0 Request Source Select Register 2	DM0SL2	XX00 0000b
044071h	DMA1 Request Source Select Register 2	DM1SL2	XX00 0000b
044072h	DMA2 Request Source Select Register 2	DM2SL2	XX00 0000b
044073h	DMA3 Request Source Select Register 2	DM3SL2	XX00 0000b
044074h			
044075h			
044076h			
044077h			
044078h	DMA0 Request Source Select Register	DM0SL	XXX0 0000b
044079h	DMA1 Request Source Select Register	DM1SL	XXX0 0000b
04407Ah	DMA2 Request Source Select Register	DM2SL	XXX0 0000b
04407Bh	DMA3 Request Source Select Register	DM3SL	XXX0 0000b
04407Ch			
04407Dh	Wake-up IPL Setting Register 2	RIPL2	XX0X 0000b
04407Eh			
04407Fh	Wake-up IPL Setting Register 1	RIPL1	XX0X 0000b
044080h			
044081h			
044082h			
044083h			
044084h			
044085h			
044086h			
044087h			
044088h			
044089h			
04408Ah			
04408Bh			
04408Ch			
04408Dh			
04408Eh			
04408Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.32 SFR List (32)

Address	Register	Symbol	Reset Value
047920h	CAN1 Mailbox 18: Message Identifier	C1MB18	XXXX XXXXh
047921h			
047922h			
047923h			
047924h			
047925h	CAN1 Mailbox 18: Data Length		XXh
047926h	CAN1 Mailbox 18: Data Field		XXXX XXXX XXXX XXXXh
047927h			
047928h			
047929h			
04792Ah			
04792Bh			
04792Ch			
04792Dh			
04792Eh	CAN1 Mailbox18: Time Stamp		XXXXh
04792Fh			
047930h	CAN1 Mailbox 19: Message Identifier	C1MB19	XXXX XXXXh
047931h			
047932h			
047933h			
047934h			
047935h	CAN1 Mailbox 19: Data Length		XXh
047936h	CAN1 Mailbox 19: Data Field		XXXX XXXX XXXX XXXXh
047937h			
047938h			
047939h			
04793Ah			
04793Bh			
04793Ch			
04793Dh			
04793Eh	CAN1 Mailbox 19: Time Stamp		XXXXh
04793Fh			
047940h	CAN1 Mailbox 20: Message Identifier	C1MB20	XXXX XXXXh
047941h			
047942h			
047943h			
047944h			
047945h	CAN1 Mailbox 20: Data Length		XXh
047946h	CAN1 Mailbox 20: Data Field		XXXX XXXX XXXX XXXXh
047947h			
047948h			
047949h			
04794Ah			
04794Bh			
04794Ch			
04794Dh			
04794Eh	CAN1 Mailbox 20: Time Stamp		XXXXh
04794Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.33 SFR List (33)

Address	Register	Symbol	Reset Value
047950h	CAN1 Mailbox 21: Message Identifier	C1MB21	XXXX XXXXh
047951h			
047952h			
047953h			
047954h			
047955h	CAN1 Mailbox 21: Data Length		XXh
047956h	CAN1 Mailbox 21: Data Field		XXXX XXXX XXXX XXXXh
047957h			
047958h			
047959h			
04795Ah			
04795Bh			
04795Ch			
04795Dh			
04795Eh	CAN1 Mailbox 21: Time Stamp		XXXXh
04795Fh			
047960h	CAN1 Mailbox 22: Identifier	C1MB22	XXXX XXXXh
047961h			
047962h			
047963h			
047964h			
047965h	CAN1 Mailbox 22: Data Length		XXh
047966h	CAN1 Mailbox 22: Data Field		XXXX XXXX XXXX XXXXh
047967h			
047968h			
047969h			
04796Ah			
04796Bh			
04796Ch			
04796Dh			
04796Eh	CAN1 Mailbox 22: Time Stamp		XXXXh
04796Fh			
047970h	CAN1 Mailbox 23: Message Identifier	C1MB23	XXXX XXXXh
047971h			
047972h			
047973h			
047974h			
047975h	CAN1 Mailbox 23: Data Length		XXh
047976h	CAN1 Mailbox 23: Data Field		XXXX XXXX XXXX XXXXh
047977h			
047978h			
047979h			
04797Ah			
04797Bh			
04797Ch			
04797Dh			
04797Eh	CAN1 Mailbox 23: Time Stamp		XXXXh
04797Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.34 SFR List (34)

Address	Register	Symbol	Reset Value
047980h	CAN1 Mailbox 24: Message Identifier	C1MB24	XXXX XXXXh
047981h			
047982h			
047983h			
047984h			
047985h	CAN1 Mailbox 24: Data Length		XXh
047986h	CAN1 Mailbox 24: Data Field		XXXX XXXX
047987h			XXXX XXXXh
047988h			
047989h			
04798Ah			
04798Bh			
04798Ch			
04798Dh			
04798Eh	CAN1 Mailbox 24: Time Stamp		XXXXh
04798Fh			
047990h	CAN1 Mailbox 25: Message Identifier	C1MB25	XXXX XXXXh
047991h			
047992h			
047993h			
047994h			
047995h	CAN1 Mailbox 25: Data Length		XXh
047996h	CAN1 Mailbox 25: Data Field		XXXX XXXX
047997h			XXXX XXXXh
047998h			
047999h			
04799Ah			
04799Bh			
04799Ch			
04799Dh			
04799Eh	CAN1 Mailbox 25: Time Stamp		XXXXh
04799Fh			
0479A0h	CAN1 Mailbox 26: Message Identifier	C1MB26	XXXX XXXXh
0479A1h			
0479A2h			
0479A3h			
0479A4h			
0479A5h	CAN1 Mailbox 26: Data Length		XXh
0479A6h	CAN1 Mailbox 26: Data Field		XXXX XXXX
0479A7h			XXXX XXXXh
0479A8h			
0479A9h			
0479AAh			
0479ABh			
0479ACh			
0479ADh			
0479AEh	CAN1 Mailbox 26: Time Stamp		XXXXh
0479AFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.40 SFR List (40)

Address	Register	Symbol	Reset Value
047C00h	CAN0 Mailbox 0: Message Identifier	C0MB0	XXXX XXXXh
047C01h			
047C02h			
047C03h			
047C04h			
047C05h	CAN0 Mailbox 0: Data Length		XXh
047C06h	CAN0 Mailbox 0: Data Field		XXXX XXXX XXXX XXXXh
047C07h			
047C08h			
047C09h			
047C0Ah			
047C0Bh			
047C0Ch			
047C0Dh			
047C0Eh	CAN0 Mailbox 0: Time Stamp		XXXXh
047C0Fh			
047C10h	CAN0 Mailbox 1: Message Identifier	C0MB1	XXXX XXXXh
047C11h			
047C12h			
047C13h			
047C14h			
047C15h	CAN0 Mailbox 1: Data Length		XXh
047C16h	CAN0 Mailbox 1: Data Field		XXXX XXXX XXXX XXXXh
047C17h			
047C18h			
047C19h			
047C1Ah			
047C1Bh			
047C1Ch			
047C1Dh			
047C1Eh	CAN0 Mailbox 1: Time Stamp		XXXXh
047C1Fh			
047C20h	CAN0 Mailbox 2: Message Identifier	C0MB2	XXXX XXXXh
047C21h			
047C22h			
047C23h			
047C24h			
047C25h	CAN0 Mailbox 2: Data Length		XXh
047C26h	CAN0 Mailbox 2: Data Field		XXXX XXXX XXXX XXXXh
047C27h			
047C28h			
047C29h			
047C2Ah			
047C2Bh			
047C2Ch			
047C2Dh			
047C2Eh	CAN0 Mailbox 2: Time Stamp		XXXXh
047C2Fh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 4.48 SFR List (48)

Address	Register	Symbol	Reset Value
047D80h	CAN0 Mailbox 24: Message Identifier	C0MB24	XXXX XXXXh
047D81h			
047D82h			
047D83h			
047D84h			
047D85h	CAN0 Mailbox 24: Data Length		XXh
047D86h	CAN0 Mailbox 24: Data Field		XXXX XXXX XXXX XXXXh
047D87h			
047D88h			
047D89h			
047D8Ah			
047D8Bh			
047D8Ch			
047D8Dh			
047D8Eh	CAN0 Mailbox 24: Time Stamp		XXXXh
047D8Fh			
047D90h	CAN0 Mailbox 25: Message Identifier	C0MB25	XXXX XXXXh
047D91h			
047D92h			
047D93h			
047D94h			
047D95h	CAN0 Mailbox 25: Data Length		XXh
047D96h	CAN0 Mailbox 25: Data Field		XXXX XXXX XXXX XXXXh
047D97h			
047D98h			
047D99h			
047D9Ah			
047D9Bh			
047D9Ch			
047D9Dh			
047D9Eh	CAN0 Mailbox 25: Time Stamp		XXXXh
047D9Fh			
047DA0h	CAN0 Mailbox 26: Message Identifier	C0MB26	XXXX XXXXh
047DA1h			
047DA2h			
047DA3h			
047DA4h			
047DA5h	CAN0 Mailbox 26: Data Length		XXh
047DA6h	CAN0 Mailbox 26: Data Field		XXXX XXXX XXXX XXXXh
047DA7h			
047DA8h			
047DA9h			
047DAAh			
047DABh			
047DACH			
047DADh			
047DAEh	CAN0 Mailbox 26: Time Stamp		XXXXh
047DAFh			

X: Undefined

Blanks are reserved. No access is allowed.

Table 5.9 Power Supply Circuit Timing Characteristics
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply start-up stabilization time after the main power supply is turned on				2	ms

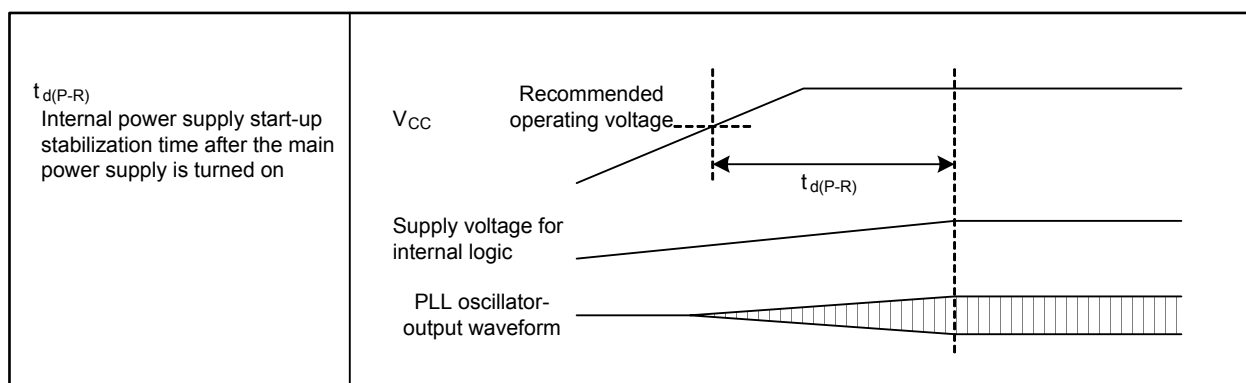


Figure 5.3 Power Supply Circuit Timing

Table 5.10 Electrical Characteristics of Voltage Regulator for Internal Logic
($V_{CC} = 3.0$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
V_{VDC1}	Output voltage			1.5		V

Table 5.11 Electrical Characteristics of Low Voltage Detector
($V_{CC} = 4.2$ to 5.5 V, $V_{SS} = 0$ V, and $T_a = T_{opr}$, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
ΔV_{det}	Detected voltage error				± 0.3	V
$V_{det(R)} - V_{det(F)}$	Hysteresis width		0			V
—	Self-consuming current	$V_{CC} = 5.0$ V, low voltage detector enabled		4		μA
$t_{d(E-A)}$	Operation start time of low voltage detector				150	μs

$$V_{CC} = 5 \text{ V}$$

Table 5.18 A/D Conversion Characteristics ($V_{CC} = AV_{CC} = V_{REF} = 4.2 \text{ to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = T_{opr}$, and $f_{(BCLK)} = 32 \text{ MHz}$, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
—	Absolute error	$V_{REF} = V_{CC} = 5 \text{ V}$ AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 ⁽¹⁾			± 3	LSB
		External op-amp connection mode			± 7	LSB
INL	Integral non-linearity error	$V_{REF} = V_{CC} = 5 \text{ V}$ AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1 ⁽¹⁾			± 3	LSB
		External op-amp connection mode			± 7	LSB
DNL	Differential non-linearity error				± 1	LSB
—	Offset error				± 3	LSB
—	Gain error				± 3	LSB
R_{LADDER}	Resistor ladder	$V_{REF} = V_{CC}$	4		20	k Ω
t_{CONV}	Conversion time (10 bits)	$\phi_{AD} = 16 \text{ MHz}$, with sample and hold function	2.06			μs
		$\phi_{AD} = 16 \text{ MHz}$, without sample and hold function	3.69			μs
t_{CONV}	Conversion time (8 bits)	$\phi_{AD} = 16 \text{ MHz}$, with sample and hold function	1.75			μs
		$\phi_{AD} = 16 \text{ MHz}$, without sample and hold function	3.06			μs
t_{SAMP}	Sampling time	$\phi_{AD} = 16 \text{ MHz}$	0.188			μs
V_{IA}	Analog input voltage		0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function	0.25		16	MHz
		With sample and hold function	1		16	MHz

Note:

1. Pins AN15_0 to AN15_7 are available in the 144-pin package only.

$$V_{CC} = 5\text{ V}$$

Timing Requirements ($V_{CC} = 4.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.22 Timer A Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	200		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.23 Timer A Input (gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	400		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.24 Timer A Input (external trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	200		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.25 Timer A Input (external trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.26 Timer A Input (increment/decrement switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{W(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{W(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{SU(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{H(TIN-UP)}$	TAiOUT input hold time	400		ns

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ($V_{CC} = 3.0$ to 3.6 V , $V_{SS} = 0 \text{ V}$, and $T_a = T_{opr}$, unless otherwise noted)

Table 5.48 Timer A Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.49 Timer A Input (gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.50 Timer A Input (external trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input clock cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.51 Timer A Input (external trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.52 Timer A Input (increment/decrement switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_h(TIN-UP)$	TAiOUT input hold time	400		ns