Infineon Technologies - TC1782F320F180HRBAKXUMA1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	ASC, CANbus, FlexRay, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	86
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	128K x 8
RAM Size	176K x 8
Voltage - Supply (Vcc/Vdd)	1.17V ~ 3.63V
Data Converters	A/D 8x10b, 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1782f320f180hrbakxuma1

  - One General Purpose Timer Array Module (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- 32 analog input lines for ADC
  - 2 independent kernels (ADC0 and ADC1)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 86 digital general purpose I/O lines (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1782ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

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2 System Overview of the TC1782

The TC1782 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1782 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1782 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1782 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1782 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1782, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB). Several I/O lines on the TC1782 ports are reserved for these peripheral units to communicate with the external world.

3 Pinning

Figure 4 is showing the TC1782 Logic Symbol.

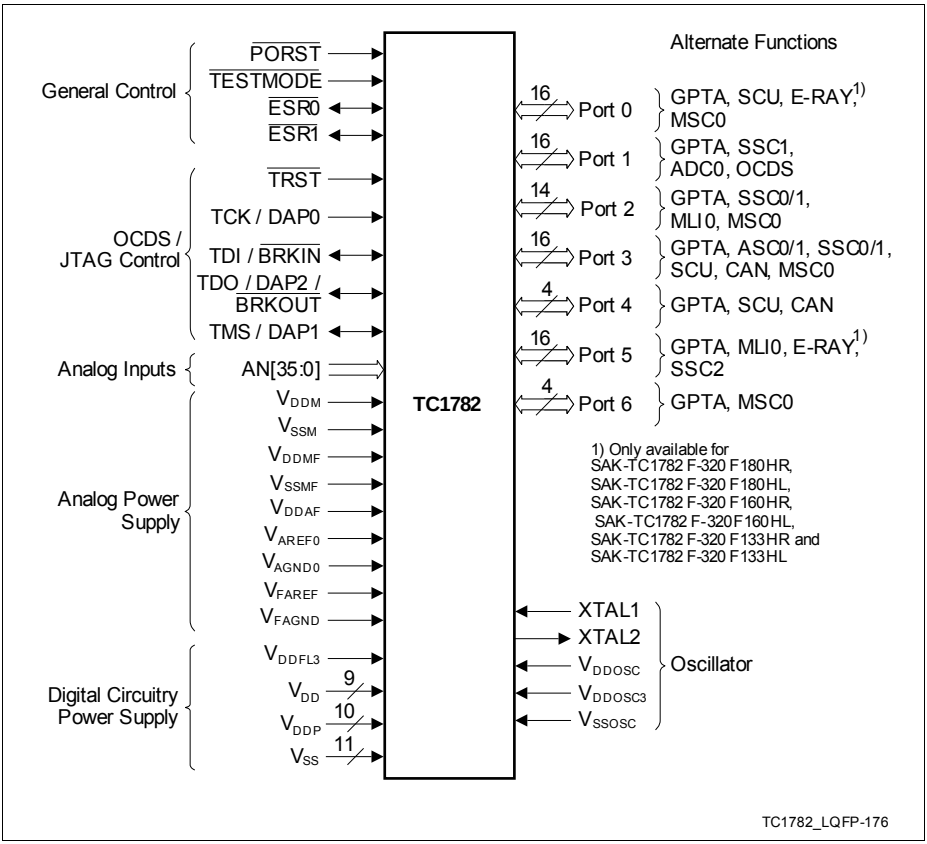

Figure 4 TC1782 Logic Symbol

Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
108	P1.5	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 35**
	IN21	I		**GPTA0 Input 21**
	IN21	I		**LTCA2 Input 21**
	OUT21	O1		**GPTA0 Output 21**
	OUT77	O2		**GPTA0 Output 77**
	OUT21	O3		**LTCA2 Output 21**
109	P1.6	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 6**
	IN22	I		**GPTA0 Input 22**
	IN22	I		**LTCA2 Input 22**
	OUT22	O1		**GPTA0 Output 22**
	OUT78	O2		**GPTA0 Output 78**
	OUT22	O3		**LTCA2 Output 22**
110	P1.7	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 7**
	IN23	I		**GPTA0 Input 23**
	IN23	I		**LTCA2 Input 23**
	OUT23	O1		**GPTA0 Output 23**
	OUT79	O2		**GPTA0 Output 79**
	OUT23	O3		**LTCA2 Output 23**
94	P1.8	I/O0	A1+/ PU	**Port 1 General Purpose I/O Line 8**
	IN24	I		**GPTA0 Input 24**
	IN48	I		**GPTA0 Input 48**
	MTSR1B	I		**SSC1 Slave Receive Input B (Slave Mode)**
	OUT24	O1		**GPTA0 Output 24**
	OUT48	O2		**GPTA0 Output 48**
	MTSR1B	O3		**SSC1 Master Transmit Output B (Master Mode)**

Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
71	P1.14	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 14**
	IN18	I		**LTCA2 Input 18**
	AD0EMUX2	O1		**ADC0 External Multiplexer Control Output 2**
	AD0EMUX2	O2		**ADC0 External Multiplexer Control Output 2**
	OUT18	O3		**LTCA2 Output 18**
117	P1.15	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 15**
	$\overline{\text{BRKIN}}$	I		**Break Input**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	$\overline{\text{BRKOUT}}$	O		**Break Output (controlled by OCDS module)**
Port 2				
74	P2.0	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 0**
	IN32	I		**GPTA0 Input 32**
	OUT32	O1		**GPTA0 Output 32**
	TCLK0	O2		**MLI0 Transmitter Clock Output 0**
	OUT28	O3		**LTCA2 Output 28**
75	P2.1	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 1**
	IN33	I		**GPTA0 Input 33**
	TREADY0A	I		**MLI0 Transmitter Ready Input A**
	OUT33	O1		**GPTA0 Output 33**
	SLSO03	O2		**SSC0 Slave Select Output Line 3**
	SLSO13	O3		**SSC1 Slave Select Output Line 3**
76	P2.2	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 2**
	IN34	I		**GPTA0 Input 34**
	OUT34	O1		**GPTA0 Output 34**
	TVALID0	O2		**MLI0 Transmitter Valid Output**
	OUT29	O3		**LTCA2 Output 29**

Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
77	P2.3	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 3**
	IN35	I		**GPTA0 Input 35**
	OUT35	O1		**GPTA0 Output 35**
	TDATA0	O2		**MLI0 Transmitter Data Output**
	OUT30	O3		**LTCA2 Output 30**
78	P2.4	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 4**
	IN36	I		**GPTA0 Input 36**
	RCLK0A	I		**MLI Receiver Clock Input A**
	OUT36	O1		**GPTA0 Output 36**
	OUT36	O2		**GPTA0 Output 36**
	OUT31	O3		**LTCA2 Output 31**
79	P2.5	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 5**
	IN37	I		**GPTA0 Input 37**
	OUT37	O1		**GPTA0 Output 37**
	RREADY0A	O2		**MLI0 Receiver Ready Output A**
	OUT110	O3		**LTCA2 Output 110**
80	P2.6	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 6**
	IN38	I		**GPTA0 Input 38**
	RVALID0A	I		**MLI Receiver Valid Input A**
	OUT38	O1		**GPTA0 Output 38**
	OUT38	O2		**GPTA0 Output 38**
	OUT111	O3		**LTCA2 Output 111**
81	P2.7	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 7**
	IN39	I		**GPTA0 Input 39**
	RDATA0A	I		**MLI Receiver Data Input A**
	OUT39	O1		**GPTA0 Output 39**
	OUT39	O2		**GPTA0 Output 39**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
133	P3.15	I/O0	A2/ PU	**Port 3 General Purpose I/O Line 15**
	TXDCAN1	O1		**CAN Node 1 Transmitter Output**
	TXD1	O2		**ASC1 Transmit Output**
	OUT97	O3		**GPTA0 Output 97**
Port 4				
86	P4.0	I/O0	A1+/ PU	**Port 4 General Purpose I/O Line 0**
	IN28	I		**GPTA0 Input 28**
	IN52	I		**GPTA0 Input 52**
	RXDCAN2	I		**CAN Node 2 Receiver Input**
	OUT28	O1		**GPTA0 Output 28**
	OUT52	O2		**GPTA0 Output 52**
	Reserved	O3		**-**
87	P4.1	I/O0	A1+/ PU	**Port 4 General Purpose I/O Line 1**
	IN29	I		**GPTA0 Input 29**
	IN53	I		**GPTA0 Input 53**
	OUT29	O1		**GPTA0 Output 29**
	OUT53	O2		**GPTA0 Output 53**
	TXDCAN2	O3		**CAN Node 2 Transmitter Output**
88	P4.2	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 2**
	IN30	I		**GPTA0 Input 30**
	IN54	I		**GPTA0 Input 54**
	OUT30	O1		**GPTA0 Output 30**
	OUT54	O2		**GPTA0 Output 54**
	EXTCLK1	O3		**External Clock 1 Output**
90	P4.3	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 3**
	IN31	I		**GPTA0 Input 31**
	IN55	I		**GPTA0 Input 55**
	OUT31	O1		**GPTA0 Output 31**
	OUT55	O2		**GPTA0 Output 55**
	EXTCLK0	O3		**External Clock 0 Output**

Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
5	P5.4	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 4**
	IN44	I		**GPTA0 Input 44**
	IN29	I		**LTCA2 Input 29**
	SLSI2A	I		**SSC2 Slave Select Input A**
	OUT44	O1		**GPTA0 Output 44**
	OUT12	O2		**LTCA2 Output 12**
	SLSO24	O3		**SSC2 Slave Select Output 4**
6	P5.5	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 5**
	IN45	I		**GPTA0 Input 45**
	IN30	I		**LTCA2 Input 30**
	MRST2A	I		**SSC2 Master Receive Input (Master Mode)**
	OUT45	O1		**GPTA0 Output 45**
	OUT13	O2		**LTCA2 Output 13**
	MRST2	O3		**SSC2 Master Transmit Input (Slave Mode)**
7	P5.6	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 6**
	IN46	I		**GPTA0 Input 46**
	IN31	I		**LTCA2 Input 31**
	MTSR2A	I		**SSC2 Slave Receive Input (Slave Mode)**
	OUT46	O1		**GPTA0 Output 46**
	OUT14	O2		**LTCA2 Output 14**
	MTSR2	O3		**SSC2 Master Transmit Output (Master Mode)**
8	P5.7	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 7**
	IN47	I		**GPTA0 Input 47**
	SCLK2A	I		**SSC2 Clock Input (Slave Mode)**
	OUT47	O1		**GPTA0 Output 47**
	OUT15	O2		**LTCA2 Output 15**
	SCLK2	O3		**SSC2 Clock Output (Master Mode)**

Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
40	AN24	I	D	**ADC1 Analog Input Channel 24**
39	AN25	I	D	**ADC1 Analog Input Channel 25**
38	AN26	I	D	**ADC1 Analog Input Channel 26**
37	AN27	I	D	**ADC1 Analog Input Channel 27**
35	AN28	I	D	**ADC1 / FADC Analog Input Channel 28**
34	AN29	I	D	**ADC1 / FADC Analog Input Channel 29**
33	AN30	I	D	**ADC1 / FADC Analog Input Channel 30**
32	AN31	I	D	**ADC1 / FADC Analog Input Channel 31**
31	AN32	I	D	**FADC Analog Input P Channel 0**
30	AN33	I	D	**FADC Analog Input N Channel 0**
29	AN34	I	D	**FADC Analog Input P Channel 1**
28	AN35	I	D	**FADC Analog Input N Channel 1**
54	V_{DDM}	-	-	**ADC Analog Part Power Supply (3.3V - 5V)**
53	V_{SSM}	-	-	**ADC Analog Part Ground**
52	V_{AREF0}	-	-	**ADC0 and ADC1 Reference Voltage**
51	V_{AGND0}	-	-	**ADC Reference Ground**
24	V_{DDMF}	-	-	**FADC Analog Part Power Supply (3.3V)**
23	V_{DDAF}	-	-	**FADC Analog Part Logic Power Supply (1.3V)**
25	V_{SSMF}	-	-	**FADC Analog Part Ground**
	V_{SSAF}	-	-	**FADC Analog Part Ground**
26	V_{FAREF}	-	-	**FADC Reference Voltage**
27	V_{FAGND}	-	-	**FADC Reference Ground**
10, 21[2)], 68, 84, 91, 99, 123, 153, 170 [2)]	V_{DD}	-	-	**Digital Core Power Supply (1.3V)**

Table 18 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FPI bus frequency	f_{FPI} SR	–	–	90	MHz	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782F-256F133HR / SAK-TC1782F-256F133HL / SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL
		–	–	80	MHz	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL

Table 18 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VDDP voltage to ensure defined pad states[5)]	V_{DDPPA} CC	0.65	–	–	V	
Digital ground voltage	V_{SS} SR	0	–	–	V	
Analog ground voltage for V_{DDM}	V_{SSM} SR	-0.1	0	0.1	V	
Analog core supply	V_{DDAF} SR	1.235	1.3	1.365[2)]	V	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL; for duration limitation see **Voltage Operating Timing Profiles**
		1.17	1.3	1.43[2)]	V	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL; for duration limitation see **Voltage Operating Timing Profiles**

Table 22 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of the class A1+ pad, medium driver	R_{DSONM} CC	–	–	155	Ohm	I_{OH}< -2 mA; P_MOS
		–	–	110	Ohm	I_{OL}< 2 mA; N_MOS
On-Resistance of the class A1+ pad, strong driver	R_{DSON1+} CC	–	–	100	Ohm	I_{OH}< -2 mA; P_MOS
		–	–	80	Ohm	I_{OL}< 2 mA; N_MOS
Fall time, pad type A1+	t_{FA1+} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	28	ns	C_L= 50 pF; edge= slow ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak

Table 22 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A1+	t_{RA1+} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	28	ns	C_L= 50 pF; edge= slow ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak
Input high voltage, Class A1+ pads	V_{IHA1+} SR	0.6 x V_{DDP}	–	*min(VDDP*+ 0.3,3.6)	V	
Input low voltage Class A1+ pads	V_{ILA1+} SR	-0.3	–	0.36 x V_{DDP}	V	
Ratio Vil/Vih, A1+ pads	V_{ILA1+} / V_{IHA1+} CC	0.6	–	–		

Table 23 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A2	t_{RA2} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	7.0	ns	C_L= 50 pF; edge= medium ; pin out driver= strong
		–	–	10	ns	C_L= 50 pF; edge= medium-minus ; pin out driver= strong
		–	–	3.7	ns	C_L= 50 pF; edge= sharp ; pin out driver= strong
		–	–	5	ns	C_L= 50 pF; edge= sharp-minus ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	7.5	ns	C_L= 100 pF; edge= sharp ; pin out driver= strong
		–	–	140	ns	C_L= 150 pF; pin out driver= medium

Table 23 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak
Input high voltage, class A2 pads	V_{IHA2} SR	0.6 x V_{DDP}	–	$min(V_{DDP}+0.3, 3.6)$	V	
Input low voltage Class A2 pads	V_{ILA2} SR	-0.3	–	0.36 x V_{DDP}	V	
Output voltage high class A2 pads	V_{OHA2} CC	V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= medium
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= strong
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= medium
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= strong
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -400 µA; pin out driver= weak
		2.4	–	–	V	I_{OH}≥ -500 µA; pin out driver= weak

5.2.2 Analog to Digital Converters (ADCx)

ADC parameter are valid for $V_{DD\,/\,DDAF}$ = 1.17 V to 1.43 V; V_{DDM} = 4.5 V to 5.5 V.

Table 27 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at the analog voltage inputs[1)]	C_{AINSW} CC	–	9	20	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	20	30	pF	
Switched capacitance at the positive reference voltage input[2)3)]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[2)]	$C_{AREFTOT}$ CC	–	20	40	pF	
Differential Non-Linearity Error[4)5)6)7)]	EA_{DNL} CC	-3	–	3	LSB	ADC resolution= 12-bit [8) 9)]
Gain Error[4)6)5)7)]	EA_{GAIN} CC	-3.5	–	3.5	LSB	ADC resolution= 12-bit [8) 9)]
Integral Non-Linearity[4)6)5)7)]	EA_{INL} CC	-3	–	3	LSB	ADC resolution= 12-bit [8) 9)]
Offset Error[4)6)5)7)]	EA_{OFF} CC	-4	–	4	LSB	ADC resolution= 12-bit [8) 9)]

5.2.3 Fast Analog to Digital Converter (FADC)

Table 29 FADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at VFAREF	I_{FAREF} CC	–	–	120	µA	
Input leakage current at VFAREF[1)]	I_{FOZ2} CC	-500	–	500	nA	$V_{FAREF} \leq V_{DDMF}$ V; $V_{FAREF} \geq 0$ V
Input leakage current at VFAGND	I_{FOZ3} CC	-500	–	500	nA	

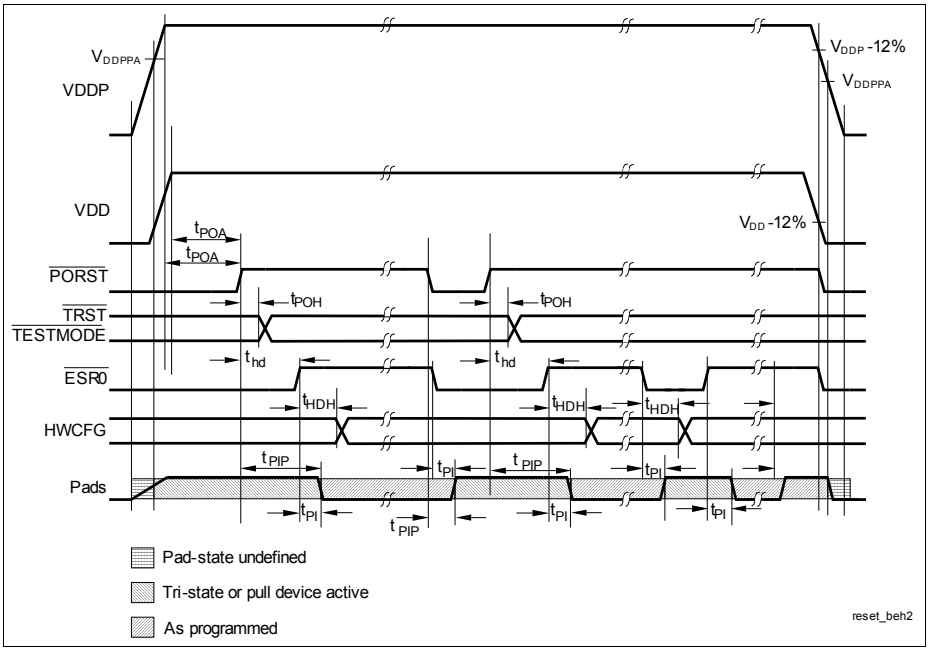

Figure 15 Power, Pad and Reset Timing

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