Infineon Technologies - TC1782F320F180HRBAKXUMA2 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	ASC, CANbus, FlexRay, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	86
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	128K x 8
RAM Size	176K x 8
Voltage - Supply (Vcc/Vdd)	1.17V ~ 3.63V
Data Converters	A/D 8x10b, 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1782f320f180hrbakxuma2

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32-Bit

Microcontroller

TC1782

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.4.1 2014-05

Microcontrollers

Table of Contents

1 Summary of Features

The **SAK-TC1782F-320F180HR** / **SAK-TC1782F-320F180HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 180 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 180 MHz operation at full temperature range
- Multiple on-chip memories
  - 2.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).

Table 10 SAK-TC1782F-320F160HL Identification Registers

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350$_H$	F000 0408$_H$	BA
CBS_JTAGID	1018 E083$_H$	F000 0464$_H$	BA
SCU_CHIPID	2500 9310$_H$	F000 0640$_H$	BA
SCU_MANID	0000 1820$_H$	F000 0644$_H$	BA
SCU_RTID	0000 0000$_H$	F000 0648$_H$	BA

Table 11 SAK-TC1782N-320F160HR Identification Registers

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Table 12 SAK-TC1782N-320F160HL Identification Registers

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SCU_MANID	0000 1820$_H$	F000 0644$_H$	BA
SCU_RTID	0000 0000$_H$	F000 0648$_H$	BA

5.1.4 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 15 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time (24000 h) is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDM})
  - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Table 15 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition except LVDS pins	I_{IN}	-5	–	+5	mA	
Input current on LVDS pins	I_{INLVDS}	-3	–	+3	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1)]	I_{ING}	-20	–	+20	mA	
Input current on analog pins	I_{INANA}	-3	–	+3	mA	
Absolute sum of all analog input currents for analog inputs of a single ADC during overload condition	I_{INSAS}	-15	–	+15	mA	
Absolute sum of all input circuit currents during overload condition	ΣI_{INS}	-100	–	100	mA	

1) The port groups are defined in **Table 19**.

Note: FADC input pins count as analog pin as they are overlayed with an ADC pins.

5.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC1782.

Digital supply voltages applied to the TC1782 must be static regulated voltages which allow a typical voltage swing of ± 5 %.

All parameters specified in the following tables refer to these operating conditions (**Table 18**), unless otherwise noticed in the Note / Test Condition column.

The **Voltage Operating Timing Profiles** did not increase area of validity of the parameters defined in table 8 and later.

Table 18 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for analog inputs, negative	K_{OVAN} CC	–	–	0.0001		$I_{OV} \leq$ 0 mA; $I_{OV} \geq$ -2 mA; analog pad= 5.0 V
Overload coupling factor for analog inputs, positive	K_{OVAP} CC	–	–	0.00001		$I_{OV} \leq$ 3 mA; $I_{OV} \geq$ 0 mA; analog pad= 5.0 V
CPU Frequency	f_{CPU} SR	–	–	133	MHz	SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL
		–	–	180	MHz	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL
		–	–	160	MHz	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL

Table 18 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PCP Frequency	f_{PCP} SR	–	–	133	MHz	SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL
		–	–	180	MHz	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL
		–	–	160	MHz	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL
Inactive device pin current	I_{ID} SR	-1	–	1	mA	All power supply voltages V_{DDx} = 0
Short circuit current of digital outputs[1)]	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} CC	–	–	100	mA	
Absolute sum of short circuit currents per pin group	ΣI_{SC_PG} CC	–	–	20	mA	
Ambient Temperature	T_A SR	-40	–	125	°C	
Junction temperature	T_J SR	-40	–	150	°C	

Table 23 Standard_Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A2 pads [1]	$HYSA2$ CC	0.1 x V_{DDP}	–	–	V	
Input Leakage current Class A2	I_{OZA2} CC	-6000	–	6000	nA	$V_i < V_{DDP}$ / 2 - 1 V; $V_i > V_{DDP}$ / 2 + 1 V; $V_i \geq 0$ V; $V_i \leq V_{DDP}$ V
		-3000	–	3000	nA	$V_i > V_{DDP}$ / 2 - 1 V; $V_i < V_{DDP}$ / 2 + 1 V
Ratio Vil/Vih, A2 pads	V_{ILA2} / V_{IHA2} CC	0.6	–	–		
On-Resistance of the class A2 pad, weak driver	R_{DSONW} CC	–	450	600	Ohm	I_{OH} < -0.5 mA; P_MOS
		–	210	340	Ohm	I_{OL} < 0.5 mA; N_MOS
On-Resistance of the class A2 pad, medium driver	R_{DSONM} CC	–	–	155	Ohm	I_{OH} < -2 mA; P_MOS
		–	–	110	Ohm	I_{OL} < 2 mA; N_MOS
On-Resistance of the class A2 pad, strong driver	R_{DSON2} CC	–	–	28	Ohm	I_{OH} < -2 mA; P_MOS
		–	–	22	Ohm	I_{OL} < 2 mA; N_MOS

5.2.2 Analog to Digital Converters (ADCx)

ADC parameter are valid for $V_{DD\,/\,DDAF}$ = 1.17 V to 1.43 V; V_{DDM} = 4.5 V to 5.5 V.

Table 27 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at the analog voltage inputs[1)]	C_{AINSW} CC	–	9	20	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	20	30	pF	
Switched capacitance at the positive reference voltage input[2)3)]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[2)]	$C_{AREFTOT}$ CC	–	20	40	pF	
Differential Non-Linearity Error[4)5)6)7)]	EA_{DNL} CC	-3	–	3	LSB	ADC resolution= 12-bit [8) 9)]
Gain Error[4)6)5)7)]	EA_{GAIN} CC	-3.5	–	3.5	LSB	ADC resolution= 12-bit [8) 9)]
Integral Non-Linearity[4)6)5)7)]	EA_{INL} CC	-3	–	3	LSB	ADC resolution= 12-bit [8) 9)]
Offset Error[4)6)5)7)]	EA_{OFF} CC	-4	–	4	LSB	ADC resolution= 12-bit [8) 9)]

Table 27 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Converter clock	f_{ADC} SC	4	–	90	MHz	f_{ADC}= f_{FPI}; SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL
		4	–	80	MHz	f_{ADC}= f_{FPI}; SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL
Internal ADC clock	f_{ADCI} CC	1	–	18	MHz	
Charge consumption per conversion	Q_{CONV} CC	70	85[10)]	100	pC	charge needs to be provided via V_{AREF0}

5.2.4 Oscillator Pins

Table 30 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-25	–	25	µA	$V_{IN}<V_{DDOSC3}$; $V_{IN}>0$ V
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		8	–	25	MHz	External Crystal Mode selected
Oscillator start-up time[1]	t_{OSCS} CC	–	–	10	ms	
Input high voltage at XTAL1[2]	V_{IHX} SR	0.7 x V_{DDOSC3}	–	V_{DDOSC3} + 0.5	V	
Input low voltage at XTAL1	V_{ILX} SR	-0.5	–	0.3 x V_{DDOSC3}	V	
Input Hysteresis for XTAL1 pad [3]	$HYSAX$ CC	–	–	200	mV	

1) t_{OSCS} is defined from the moment when V_{DDOSC3} = 3.13V until the oscillations reach an amplitude at XTAL1 of 0.3 * V_{DDOSC3}. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystral suppliers.

2) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of 0.4 * V_{DDOSC3} is necessary.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

5.3.3 Power, Pad and Reset Timing

Table 33 Reset Timings Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time[1)2)]	t_B CC	150	–	810	µs	SAK-TC1782N-256F133HR SAK-TC1782N-256F133HL
		150	–	665	µs	SAK-TC1782F320F180HR SAK-TC1782F320F180HL SAK-TC1782N-320F180HR SAK-TC1782N-320F180HL
		150	–	740	µs	SAK-TC1782F-320F160HR SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR SAK-TC1782N-320F160HL
Power on Reset Boot Time[3)4)]	t_{BP} CC	–	–	2.5	ms	
HWCFG pins hold time from ESR0 rising edge	t_{HDH} SR	16 / f_{FPI}	–	–	ns	
HWCFG pins setup time to ESR0 rising edge	t_{HDS} CC	0	–	–	ns	
Ports inactive after ESR0 reset active	t_{PI} CC	–	–	8 / f_{FPI}	ns	
Ports inactive after PORST reset active[5)]	t_{PIP} CC	–	–	150	ns	

Table 33 Reset Timings Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Minimum PORST active time after power supplies are stable at operating levels	t_{POA} CC	10	–	–	ms	
$\overline{\text{TESTMODE}}$ / $\overline{\text{TRST}}$ hold time from PORST rising edge	t_{POH} SR	100	–	–	ns	
PORST rise time	t_{POR} SR	–	–	50	ms	
$\overline{\text{TESTMODE}}$ / $\overline{\text{TRST}}$ setup time to PORST rising edge	t_{POS} SR	0	–	–	ns	

1) The duration of the boot time is defined between the rising edge of the internal application reset and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.
2) The given time includes the time of the internal reset extension for a configured value of SCU_RSTCNTCON.RELSA = 0x05BE.
3) The duration of the boot time is defined between the rising edge of the $\overline{\text{PORST}}$ and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.
4) The given time includes the internal reset extension time for the System and Application Reset which is visible through ESR0.
5) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.

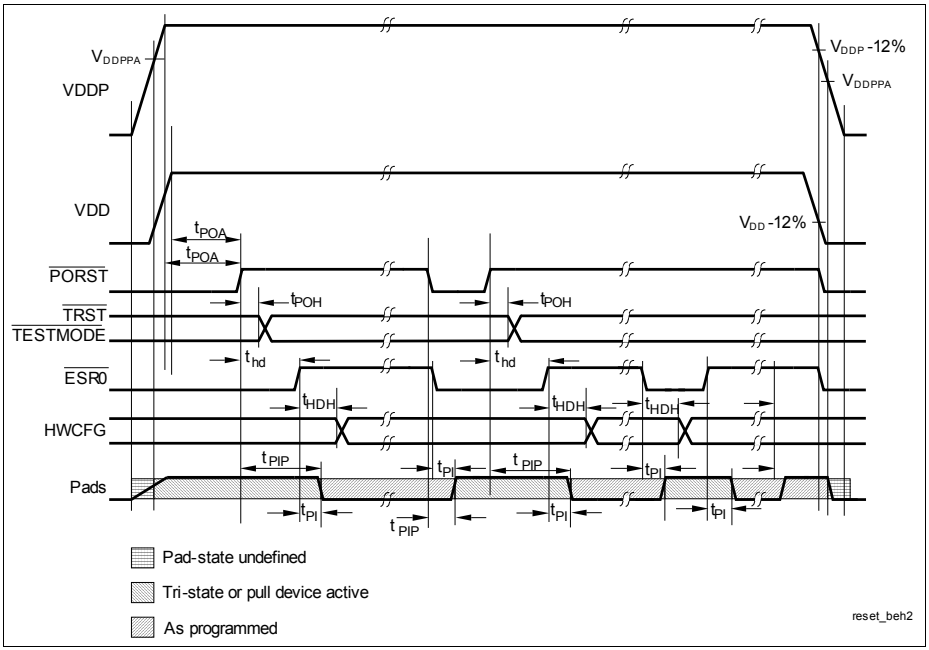

Figure 15 Power, Pad and Reset Timing

5.3.4 Phase Locked Loop (PLL)

Table 34 PLL_SysClk Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	-7	–	7	ns	
PLL base frequency	$f_{PLLBASE}$ CC	50	200	320	MHz	
VCO input frequency	f_{REF} CC	8	–	16	MHz	
VCO frequency range	f_{VCO} CC	400	–	720	MHz	
PLL lock-in time	t_L CC	14	–	200	µs	N > 32
		14	–	400	µs	N ≤ 32

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the LMB-Bus clock f_{LMB}) is constantly adjusted to the selected frequency. The PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or clock source), resulting in an accumulated jitter that is limited. This means that the relative deviation for periods of more than one clock cycle is lower than for a single clock cycle.

This is especially important for bus cycles using wait states and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

Two formulas are defined for the (absolute) approximate maximum value of jitter D_m in [ns] dependent on the K2 - factor, the LMB clock frequency f_{LMB} in [MHz], and the number m of consecutive f_{LMB} clock periods.

$$\text{for} \quad (K2 \le 100) \quad \text{and} \quad (m \le (f_{LMB}[MHz])/2)$$

$$|Dm[ns]| = \left(\frac{740}{K2 \times f_{LMB}[MHz]} + 5\right) \times \left(\frac{(1 - 0,01 \times K2) \times (m - 1)}{0,5 \times f_{LMB}[MHz] - 1} + 0,01 \times K2\right) \quad (6)$$

$$\text{else} \quad |Dm[ns]| = \frac{740}{K2 \times f_{LMB}[MHz]} + 5 \quad (7)$$

With rising number m of clock cycles the maximum jitter increases linearly up to a value of m that is defined by the K2-factor of the PLL. Beyond this value of m the maximum

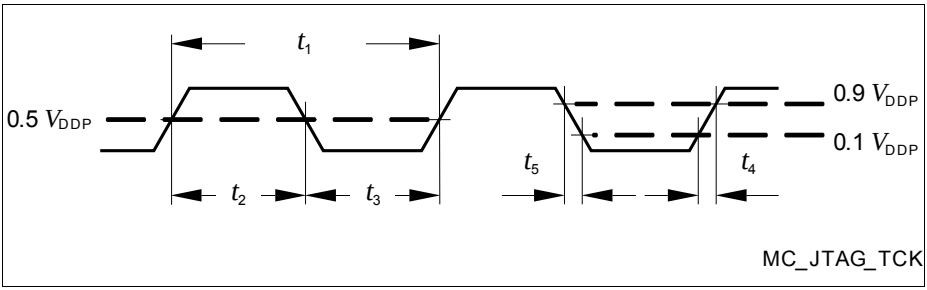

Figure 16 Test Clock Timing (TCK)

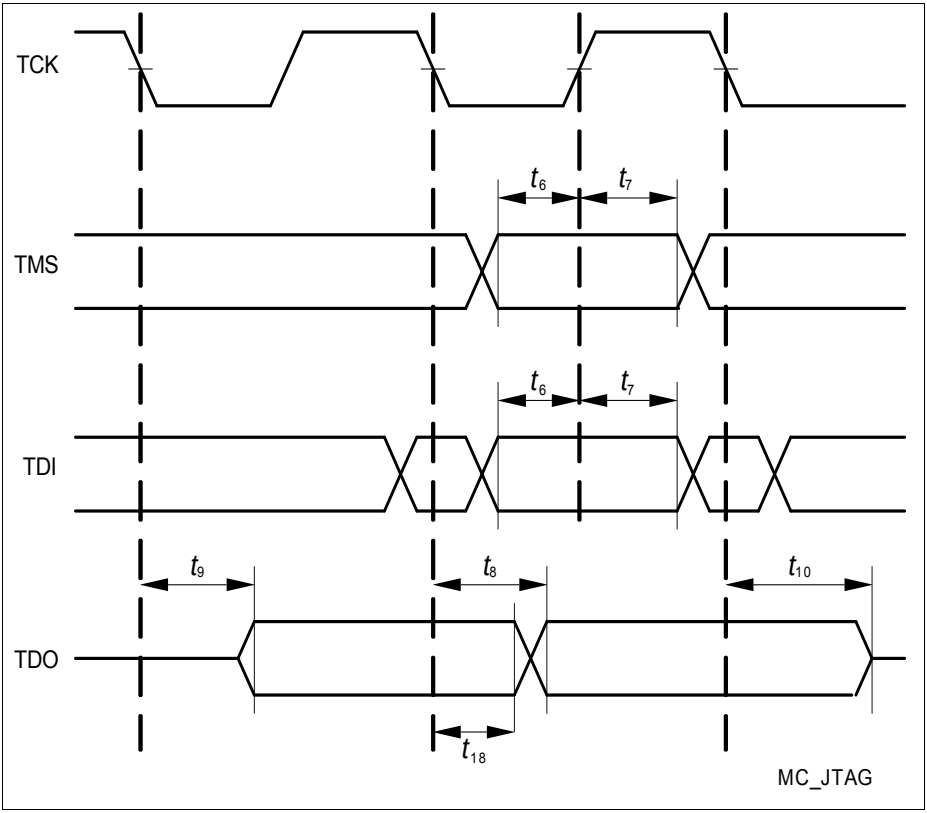

Figure 17 JTAG Timing

Table 39 MLI Transmitter (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCLK fall time	t_{14} CC	–	–	0.3 x t_{10} 3)	ns	
TDATA/TVALID output delay time	t_{15} CC	-3	–	4.4	ns	
TREADY setup time before TCLK rising edge	t_{16} SR	18	–	–	ns	
TREADY hold time after TCLK rising edge	t_{17} SR	-2	–	–	ns	

1) The following formula is valid: t11 + t12 = t10.

2) The min./max. TCLK low/high times t11/t12 include the PLL jitter of fSYS. Fractional divider settings must be regarded additionally to t11 / t12.

3) For high-speed MLI interface, strong driver sharp or medium edge selection (class A2 pad) is recommended for TCLK.

5.3.8.2 Micro Second Channel (MSC) Interface Timing

The MSC parameters are vaild for C_L = 50 pF.

Table 40 MSC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLP clock period[1)2)]	t_{40} CC	2 x T_{MSC} 3)	–	–	ns	
SOP[4)]/ENx outputs delay from FCLP[4)] rising edge	t_{45} CC	-2	–	5	ns	ENx with strong driver and sharp (minus) edge
		-2	–	10	ns	ENx with strong driver and medium (minus) edge
		0	–	21	ns	ENx with strong driver and soft edge

1) This lifetime refers only to the time when the device is powered on.
2) For worst-case temperature profile equivalent to:
   1200 hours at T_j = 125...150°C
   3600 hours at T_j = 110...125°C
   7200 hours at T_j = 100...110°C
   11000 hours at T_j = 25...100°C
   1000 hours at T_j = -40...25°C

- removed products SAK-TC1182N-320F180HR, SAK-TC1182N-320F180HL, SAK-TC1182N-256F133HR, and SAK-TC1182N-256F133HL
- improve parameters I_{DDFL3}
- change for parameter N_E note from Max. data retention to Min.
- removed the term (typical)
- change description of parameter t_{CAL} for the ADC
- correct typo for class D pads in tables 14 and 15
- adapt Absolute Maximun Rating
- add footnote to Flash parameter t_{ERD}
- add note at the end of Pin Reliability in Overload section
- clearify pad supply levels in Pin Reliability in Overload section
- add footnote for D-Flash currents in power section

The following changes where done between Version 1.2 and 1.3 of this document:

- add product option SAK-TC1782F-320F160HL, SAK-TC1782F-320F160HR, SAK-TC1782N-320F160HL and SAK-TC1782N-320F160HR
- update block diagrams to cover new option
- add identification registers for new product option
- rework first sentence for chapter 5.3
- reduce min value for t_L for both PLLs
- add for MLI and SSC parameter: valid strong driver medium edge only
- add footnote 5) for SSC parameters
- update FADC parameter EF_{DNL}
- change MLI parameter t_{17} min value
- rename section Extented Range Operating Conditions to Voltage Operating timing Profiles and remove limitions on GPIOs
- split R_{DSONM} for class F pads into two conditions

The following changes where done between Version 1.3 and 1.3.1 of this document:

- correct typos in table 1
  - SAK-TC1782N-320N160HR -> SAK-TC1782F-320F160HR
  - SAK-TC1782N-320N160HL -> SAK-TC1782F-320F160HL
- reduce current for I_{LVDS} from 24mA to 12mA (only 2 pairs are available)

The following changes where done between Version 1.3.1 and 1.4 of this document:

- remove the following product options:
  - SAK-TC1782F-256F133HR
  - SAK-TC1782F-256F133HL
- change t_{48} from 100ns to 200ns in table 42
- change t_{49} from 100ns to 200ns in table 42
- extend K_{OVAN} conditon from $I_{OV} \leq$ 0 mA; $I_{OV} \geq$ -1 mA to $I_{OV} \leq$ 0 mA; $I_{OV} \geq$ -2 mA
- change parameter EF_{OFF} from +-90mV to +-120 for condition Calibration = No

The following changes where done between Version 1.4 and 1.4.1 of this document:

- change parameter EF_{OFF} from +-120mV to +-90 for condition Calibration = No