Infineon Technologies - TC1782N320F180HRBAKXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	ASC, CANbus, FlexRay, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	86
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	128K x 8
RAM Size	176K x 8
Voltage - Supply (Vcc/Vdd)	1.17V ~ 3.63V
Data Converters	A/D 8x10b, 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1782n320f180hrbakxuma1

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1 Summary of Features

The **SAK-TC1782F-320F180HR** / **SAK-TC1782F-320F180HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 180 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 180 MHz operation at full temperature range
- Multiple on-chip memories
  - 2.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).

The **SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 160 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 160 MHz operation at full temperature range
- Multiple on-chip memories
  - 2.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
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  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1782 please refer to the **"Product Catalog Microcontrollers"**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

Table 1 TC1782 Derivative Synopsis

Derivative	Ambient Temperature Range	Package
SAK-TC1782F-320F180HR	T_A = -40°C to +125°C	PG-LQFP-176-20
SAK-TC1782F-320F180HL	T_A = -40°C to +125°C	PG-LQFP-176-10
SAK-TC1782N-320F180HR	T_A = -40°C to +125°C	PG-LQFP-176-20
SAK-TC1782N-320F180HL	T_A = -40°C to +125°C	PG-LQFP-176-10
SAK-TC1782N-256F133HR	T_A = -40°C to +125°C	PG-LQFP-176-20
SAK-TC1782N-256F133HL	T_A = -40°C to +125°C	PG-LQFP-176-10
SAK-TC1782F-320F160HR	T_A = -40°C to +125°C	PG-LQFP-176-20
SAK-TC1782F-320F160HL	T_A = -40°C to +125°C	PG-LQFP-176-10
SAK-TC1782N-320F160HR	T_A = -40°C to +125°C	PG-LQFP-176-20
SAK-TC1782N-320F160HL	T_A = -40°C to +125°C	PG-LQFP-176-10

Figure 2 shows the block diagram of the **SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL** / **SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL**.

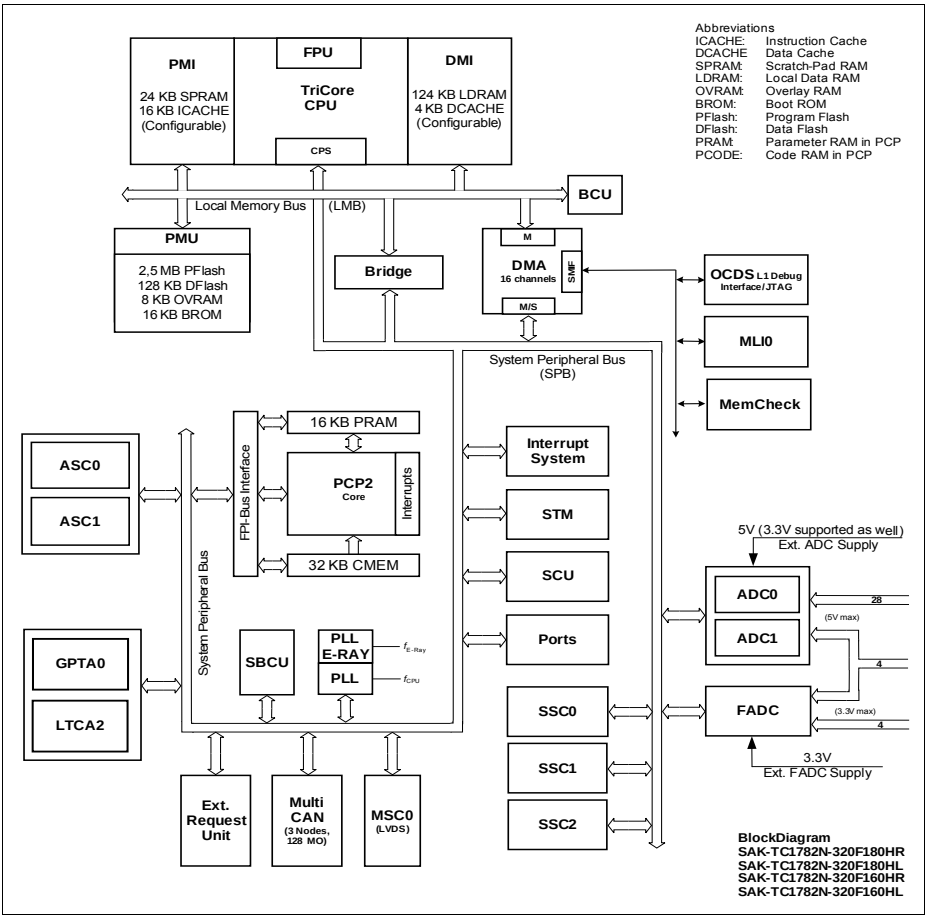

Figure 2 SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL / Block Diagram

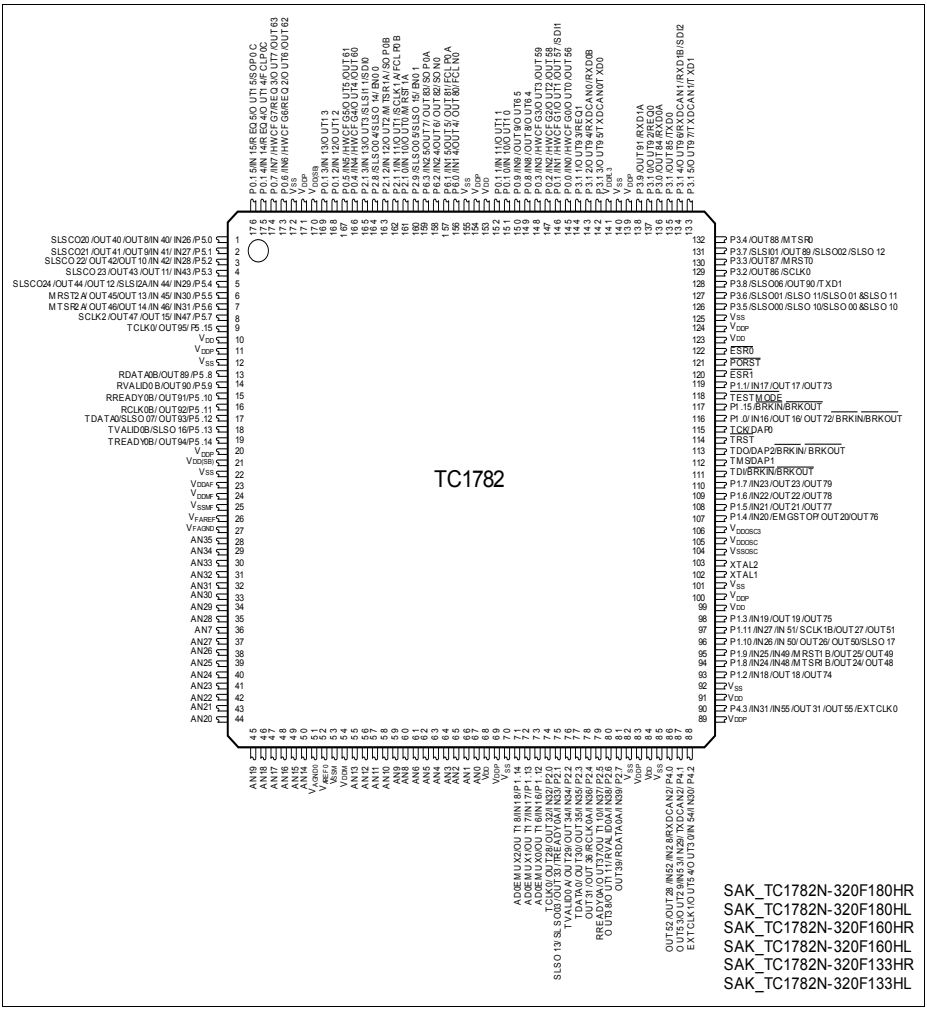

Figure 6 SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL / SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL / Pinning

Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
174	P0.7	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 7**
	IN7	I		**GPTA0 Input 7**
	IN7	I		**LTCA2 Input 7**
	HWCFG7	I		**Hardware Configuration Input 7**
	REQ3	I		**External Request Input 3**
	OUT7	O1		**GPTA0 Output 7**
	OUT63	O2		**GPTA0 Output 63**
	OUT7	O3		**LTCA2 Output 7**
149	P0.8	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 8**
	IN8	I		**GPTA0 Input 8**
	IN8	I		**LTCA2 Input 8**
	RXDA0	I		**E-Ray Channel A Receive Data Input 0** [1]
	OUT8	O1		**GPTA0 Output 8**
	OUT64	O2		**GPTA0 Output 64**
	OUT8	O3		**LTCA2 Output 8**
150	P0.9	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 9**
	IN9	I		**GPTA0 Input 9**
	IN9	I		**LTCA2 Input 9**
	RXDB0	I		**E-Ray Channel B Receive Data Input 0** [1]
	OUT9	O1		**GPTA0 Output 9**
	OUT65	O2		**GPTA0 Output 65**
	OUT9	O3		**LTCA2 Output 9**
151	P0.10	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 10**
	IN10	I		**GPTA0 Input 10**
	OUT10	O1		**GPTA0 Output 10**
	TXDA0	O2		**E-Ray Channel A transmit Data Output** [1]
	OUT10	O3		**LTCA2 Output 10**

Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
137	P3.10	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 10**
	REQ0	I		**External Request Input 0**
	Reserved	O1		**-**
	Reserved	O2		**-**
	OUT92	O3		**GPTA0 Output 92**
144	P3.11	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 11**
	REQ1	I		**External Request Input 1**
	Reserved	O1		**-**
	Reserved	O2		**-**
	OUT93	O3		**GPTA0 Output 93**
143	P3.12	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 12**
	RXDCAN0	I		**CAN Node 0 Receiver Input**
	RXD0B	I		**ASC0 Receiver Input B**
	RXD0B	O1		**ASC0 Receiver Output B (Synchronous Mode)**
	RXD0B	O2		**ASC0 Receiver Output B (Synchronous Mode)**
	OUT94	O3		**GPTA0 Output 94**
142	P3.13	I/O0	A2/ PU	**Port 3 General Purpose I/O Line 13**
	TXDCAN0	O1		**CAN Node 0 Transmitter Output**
	TXD0	O2		**ASC0 Transmit Output**
	OUT95	O3		**GPTA0 Output 95**
134	P3.14	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 14**
	RXDCAN1	I		**CAN Node 1 Receiver Input**
	RXD1B	I		**ASC1 Receiver Input B**
	SDI2	I		**MSC0 Serial Data Input 2**
	RXD1B	O1		**ASC1 Receiver Output B (Synchronous Mode)**
	RXD1B	O2		**ASC1 Receiver Output B (Synchronous Mode)**
	OUT96	O3		**GPTA0 Output 96**

Table 18 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FPI bus frequency	f_{FPI} SR	–	–	90	MHz	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782F-256F133HR / SAK-TC1782F-256F133HL / SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL
		–	–	80	MHz	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL

Table 19 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
1	P5.[7:2], P5.15
2	P5.[9:8]
3	P5.[11:10]
4	P5.[14:12]
5	P1.[14:12], P2.0
6	P2.[4:1]
7	P2.[7:5]
8	P4.[2:0]
9	P4.3
10	P1.2, P1.8
11	P1.[10:9]
12	P1.3, P1.11
13	P1.[7:4]
14	P1.[1:0], P1.15
15	P3.[8:5], P3.[3:2]
16	P3.[1:0], P3.4, P3.[10:9], P3.[15:14]
17	P0.[1:0], P3.[13:11]
18	P0.[3:2], P0.[9:8]
19	P0.[11:10]
20	P6.[3:0]
21	P2.[13:8]
22	P0.[5:4], P0.[13:12]
23	P0.[7:6], P0.[15:14], P5.[1:0]

5.2 DC Parameters

5.2.1 Input/Output Pins

Table 20 Standard_Pads Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	T_A= 25 °C; f= 1 MHz
Pull-down current	$\|I_{PDL}\|$ CC	–	–	150	µA	$V_i \geq$ 0.6 x V_{DDP} V
		10	–	–	µA	$V_i \geq$ 0.36 x V_{DDP} V
Pull-Up current	$\|I_{PUH}\|$ CC	10	–	–	µA	$V_i \leq$ 0.6 x V_{DDP} V
		–	–	100	µA	$V_i \leq$ 0.36 x V_{DDP} V
Spike filter always blocked pulse duration	t_{SF1} CC	–	–	10	ns	only PORST pin
Spike filter pass-through pulse duration	t_{SF2} CC	100	–	–	ns	only PORST pin

Table 21 Standard_Pads Class_A1

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A1 pads [1]	$HYSA1$ CC	0.1 x V_{DDP}	–	–	V	
Input Leakage Current Class A1	I_{OZA1} CC	-500	–	500	nA	$V_i \geq$ 0 V; $V_i \leq V_{DDP}$ V
Ratio Vil/Vih, A1 pads	V_{ILA1} / V_{IHA1} CC	0.6	–	–		
On-Resistance of the class A1 pad, weak driver	R_{DSONW} CC	–	450	600	Ohm	I_{OH}< -0.5 mA; P_MOS
		–	210	340	Ohm	I_{OL}< 0.5 mA; N_MOS

Table 22 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of the class A1+ pad, medium driver	R_{DSONM} CC	–	–	155	Ohm	I_{OH}< -2 mA; P_MOS
		–	–	110	Ohm	I_{OL}< 2 mA; N_MOS
On-Resistance of the class A1+ pad, strong driver	R_{DSON1+} CC	–	–	100	Ohm	I_{OH}< -2 mA; P_MOS
		–	–	80	Ohm	I_{OL}< 2 mA; N_MOS
Fall time, pad type A1+	t_{FA1+} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	28	ns	C_L= 50 pF; edge= slow ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak

Table 22 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A1+	t_{RA1+} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	28	ns	C_L= 50 pF; edge= slow ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak
Input high voltage, Class A1+ pads	V_{IHA1+} SR	0.6 x V_{DDP}	–	*min(VDDP*+ 0.3,3.6)	V	
Input low voltage Class A1+ pads	V_{ILA1+} SR	-0.3	–	0.36 x V_{DDP}	V	
Ratio Vil/Vih, A1+ pads	V_{ILA1+} / V_{IHA1+} CC	0.6	–	–		

5.2.2 Analog to Digital Converters (ADCx)

ADC parameter are valid for $V_{DD\,/\,DDAF}$ = 1.17 V to 1.43 V; V_{DDM} = 4.5 V to 5.5 V.

Table 27 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at the analog voltage inputs[1)]	C_{AINSW} CC	–	9	20	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	20	30	pF	
Switched capacitance at the positive reference voltage input[2)3)]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[2)]	$C_{AREFTOT}$ CC	–	20	40	pF	
Differential Non-Linearity Error[4)5)6)7)]	EA_{DNL} CC	-3	–	3	LSB	ADC resolution= 12-bit [8) 9)]
Gain Error[4)6)5)7)]	EA_{GAIN} CC	-3.5	–	3.5	LSB	ADC resolution= 12-bit [8) 9)]
Integral Non-Linearity[4)6)5)7)]	EA_{INL} CC	-3	–	3	LSB	ADC resolution= 12-bit [8) 9)]
Offset Error[4)6)5)7)]	EA_{OFF} CC	-4	–	4	LSB	ADC resolution= 12-bit [8) 9)]

5.3.4 Phase Locked Loop (PLL)

Table 34 PLL_SysClk Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	-7	–	7	ns	
PLL base frequency	$f_{PLLBASE}$ CC	50	200	320	MHz	
VCO input frequency	f_{REF} CC	8	–	16	MHz	
VCO frequency range	f_{VCO} CC	400	–	720	MHz	
PLL lock-in time	t_L CC	14	–	200	µs	N > 32
		14	–	400	µs	N ≤ 32

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the LMB-Bus clock f_{LMB}) is constantly adjusted to the selected frequency. The PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or clock source), resulting in an accumulated jitter that is limited. This means that the relative deviation for periods of more than one clock cycle is lower than for a single clock cycle.

This is especially important for bus cycles using wait states and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

Two formulas are defined for the (absolute) approximate maximum value of jitter D_m in [ns] dependent on the K2 - factor, the LMB clock frequency f_{LMB} in [MHz], and the number m of consecutive f_{LMB} clock periods.

$$\text{for} \quad (K2 \le 100) \quad \text{and} \quad (m \le (f_{LMB}[MHz])/2)$$

$$|Dm[ns]| = \left(\frac{740}{K2 \times f_{LMB}[MHz]} + 5\right) \times \left(\frac{(1 - 0,01 \times K2) \times (m - 1)}{0,5 \times f_{LMB}[MHz] - 1} + 0,01 \times K2\right) \quad (6)$$

$$\text{else} \quad |Dm[ns]| = \frac{740}{K2 \times f_{LMB}[MHz]} + 5 \quad (7)$$

With rising number m of clock cycles the maximum jitter increases linearly up to a value of m that is defined by the K2-factor of the PLL. Beyond this value of m the maximum

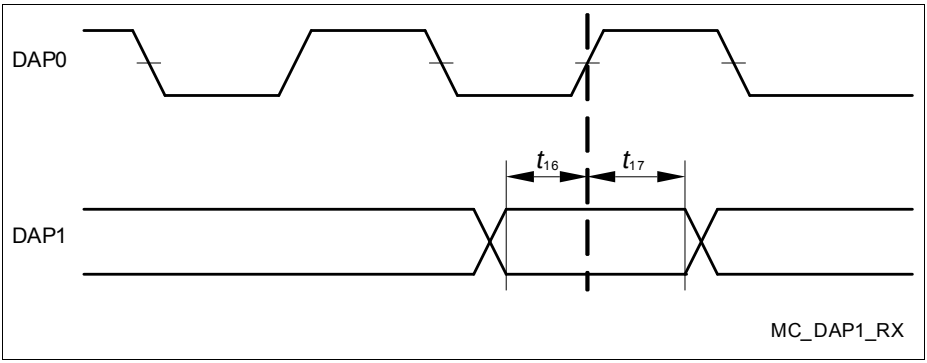

Figure 19 DAP Timing Host to Device

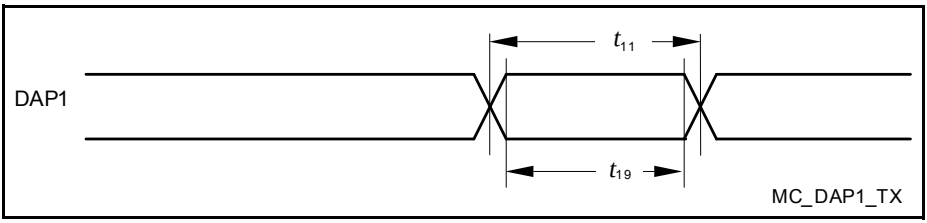

Figure 20 DAP Timing Device to Host

5.3.8.3 SSC Master/Slave Mode Timing

The SSC parameters are vaild for C_L = 50 pF and for strong driver medium edge.

Table 41 SSC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period[1)2)3)]	t_{50} CC	2 x 1 / f_{FPI}	–	–	ns	
MTSR/SLSOx delay form SCLK rising edge	t_{51} CC	0	–	8	ns	
MRST setup to SCLK falling edge[3)]	t_{52} SR	16.5	–	–	ns	
MRST hold from SCLK falling edge[3)]	t_{53} SR	0	–	–	ns	
SCLK input clock period[1)3)]	t_{54} SR	4 x 1 / f_{FPI}	–	–	ns	
SCLK input clock duty cycle	t_{55}_t_{54} SR	45	–	55	%	
MTSR setup to SCLK latching edge[3)4)]	t_{56} CC	1 / f_{FPI}	–	–	ns	
MTSR hold from SCLK latching edge	t_{57} CC	1 / f_{FPI} + 5	–	–	ns	
SLSI setup to first SCLK latching edge	t_{58} CC	1 / f_{FPI} + 5	–	–	ns	
SLSI hold from last SCLK latching edge[5)]	t_{59} CC	7	–	–	ns	
MRST delay from SCLK shift edge	t_{60} CC	0	–	16.5	ns	
SLSI to valid data on MRST	t_{61} CC	–	–	16.5	ns	

1) SCLK signal rise/fall times are the same as the rise/fall times of the pad.

2) SCLK signal high and low times can be minimum 1xTSSC.

3) TSSCmin = TSYS = 1/fSYS.

4) Fractional divider switched off, SSC internal baud rate generation used.

5) For CON.PH=1 slave select must not be removed before the following shifting edge. This mean, that what ever is configured (shifting / latching first), SLSI must not be de-actived before the last trailing edge from the pair of shifting / latching edges.

5) Valid for output slopes of the bus driver of dRxSlope ≤ 5ns, 20% * V_{DDP} to 80% * V_{DDP}, according to the FlexRay Electrical Physical Layer Specification V2.1B. For A2 pads, the rise and fall times of the incoming signal have to satisfy the following inequality: -1.6ns ≤ t_{FA2} - t_{RA2} ≤ 1.3ns.

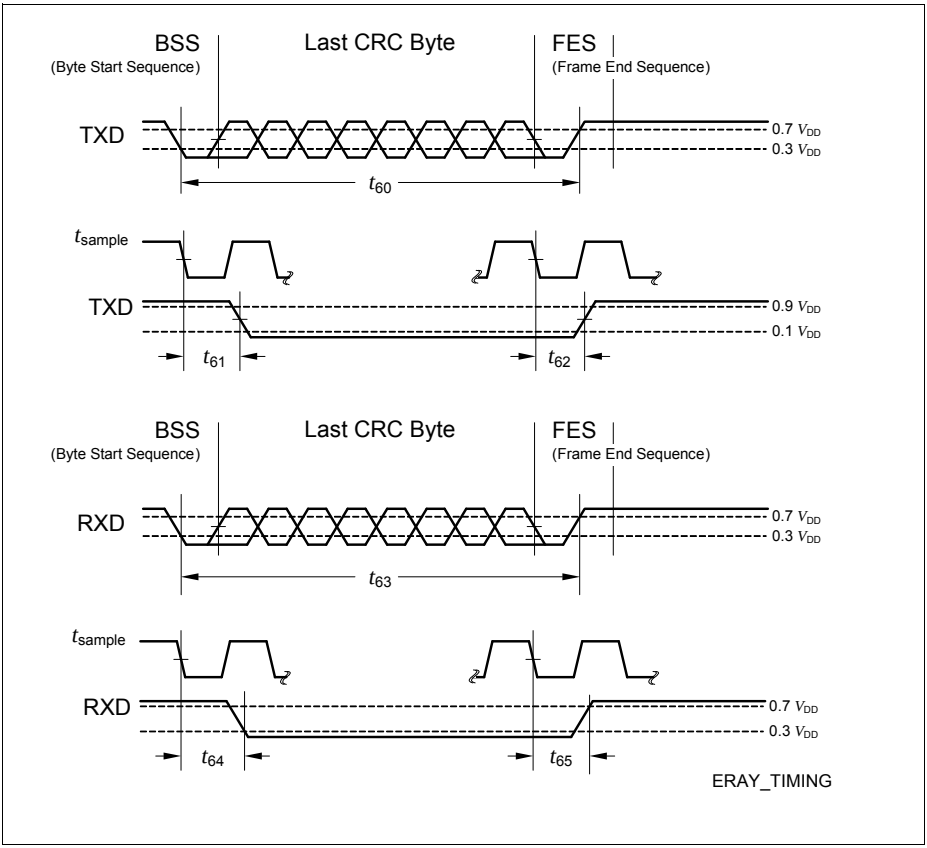

Figure 25 ERAY Timing