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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	87
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12352f13v

Figure 6-17 shows an example of wait state insertion timing.

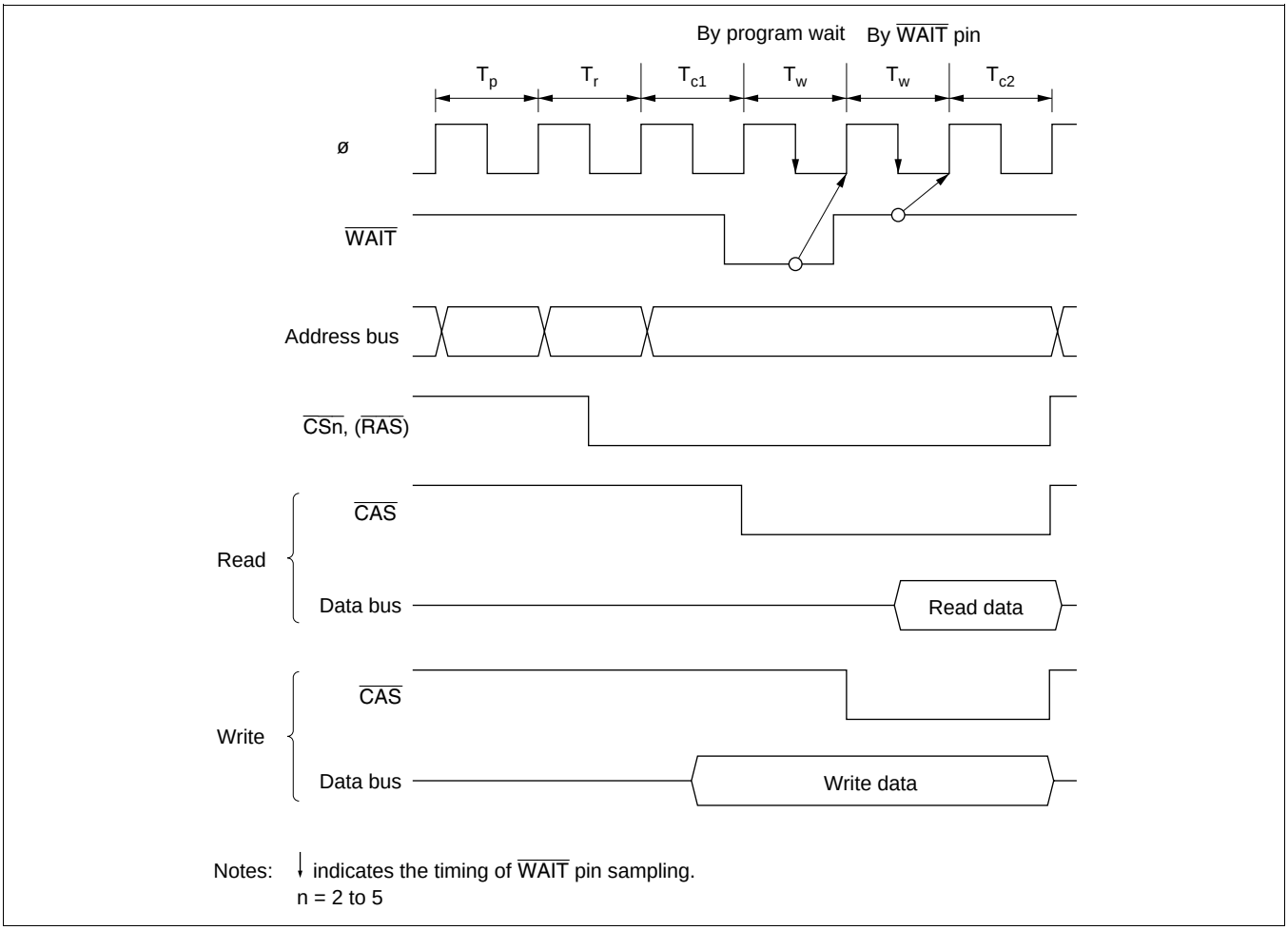


Figure 6-17 Example of Wait State Insertion Timing (CW2 = 1, 8-Bit Area Setting for Entire Space)

6.5.9 Byte Access Control

When DRAM with a ×16 configuration is connected, the 2-CAS system can be used for the control signals required for byte access.

When the CW2 bit is cleared to 0 in MCR, the 2-CAS system is selected. Figure 6-18 shows the control timing in the 2-CAS system, and figure 6-19 shows an example 2-CAS system DRAM connection.

When only DRAM with a ×8 configuration is connected, set the CW2 bit to 1 in MCR.

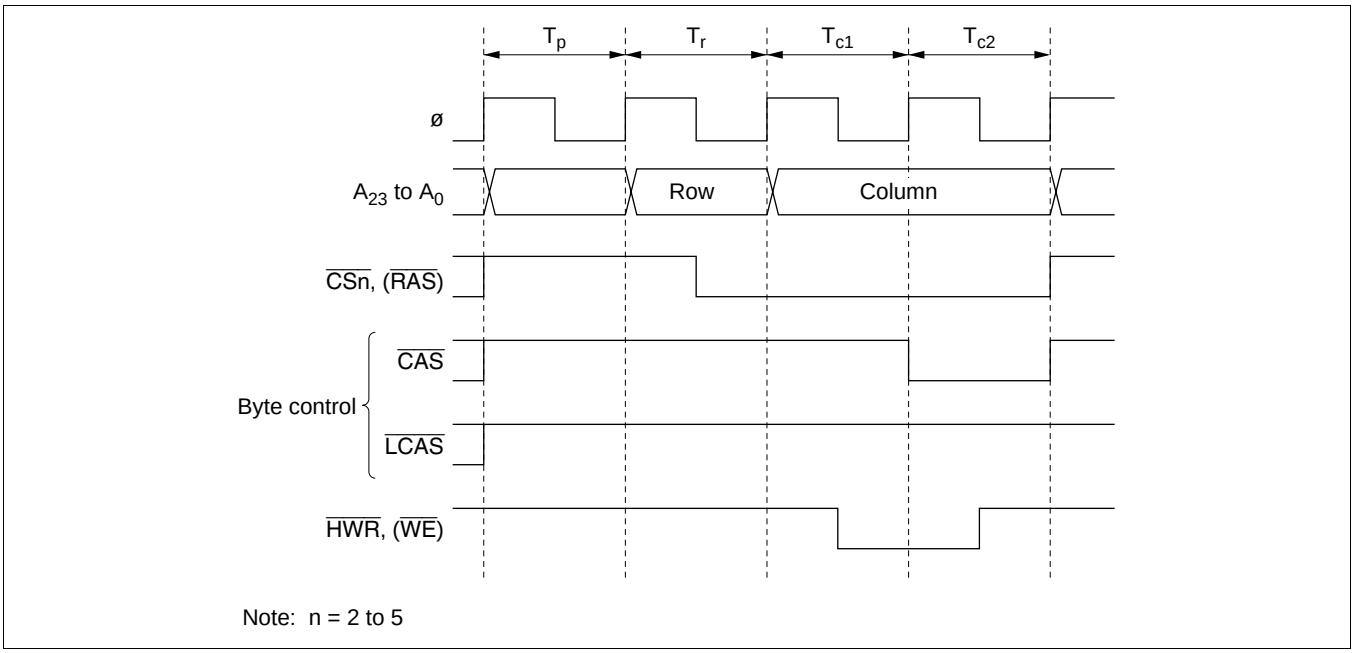


Figure 6-18 2-CAS System Control Timing (Upper Byte Write Access)

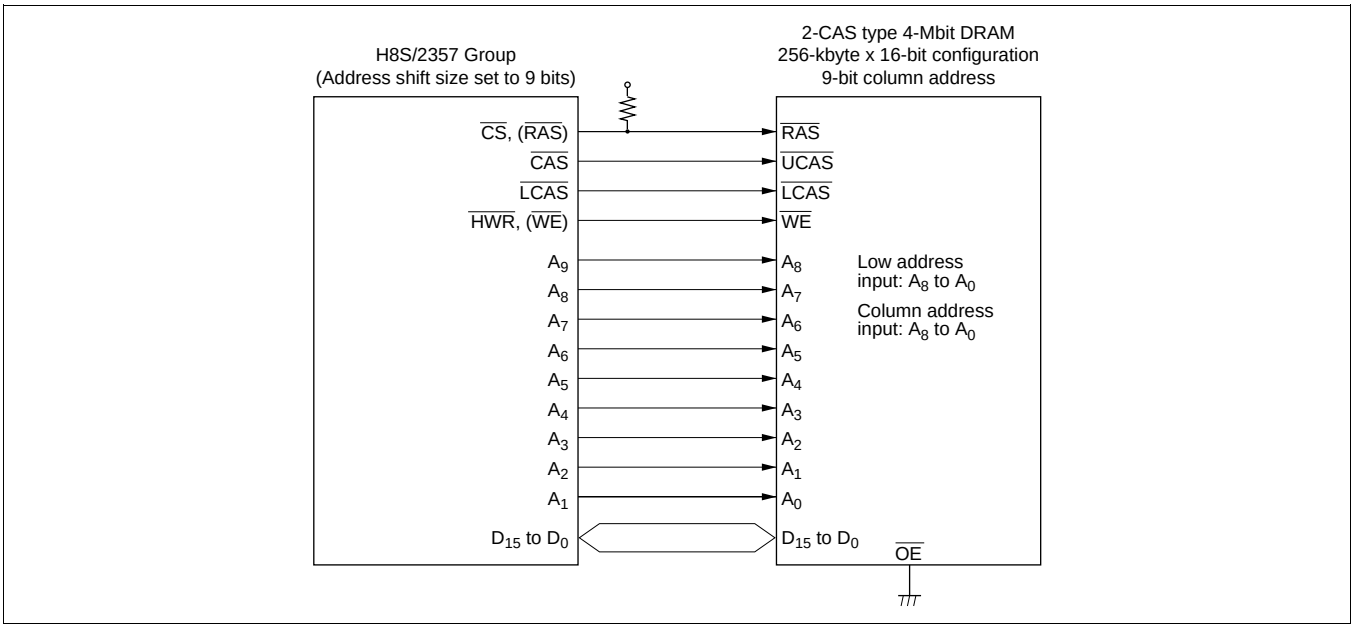


Figure 6-19 Example of 2-CAS System Connection

7.5.3 Idle Mode

Idle mode can be specified by setting the RPE bit and DTIE bit in DMACR to 1. In idle mode, one byte or word is transferred in response to a single transfer request, and this is executed the number of times specified in ETCR.

One address is specified by MAR, and the other by IOAR. The transfer direction can be specified by the DTDIR bit in DMACR.

Table 7-7 summarizes register functions in idle mode.

Table 7-7 Register Functions in Idle Mode

Register	Function		Initial Setting	Operation
	DTDIR = 0	DTDIR = 1		
23 MAR 0	Source address register	Destination address register	Start address of transfer destination or transfer source	Fixed
23 H'FF 15 IOAR 0	Destination address register	Source address register	Start address of transfer source or transfer destination	Fixed
15 ETCR 0	Transfer counter		Number of transfers	Decremented every transfer; transfer ends when count reaches H'0000

Legend:
MAR: Memory address register
IOAR: I/O address register
ETCR: Transfer count register
DTDIR: Data transfer direction bit

MAR specifies the start address of the transfer source or transfer destination as 24 bits. MAR is neither incremented nor decremented each time a byte or word is transferred.

IOAR specifies the lower 16 bits of the other address. The 8 bits above IOAR have a value of H'FF.

Figure 7-5 illustrates operation in idle mode.

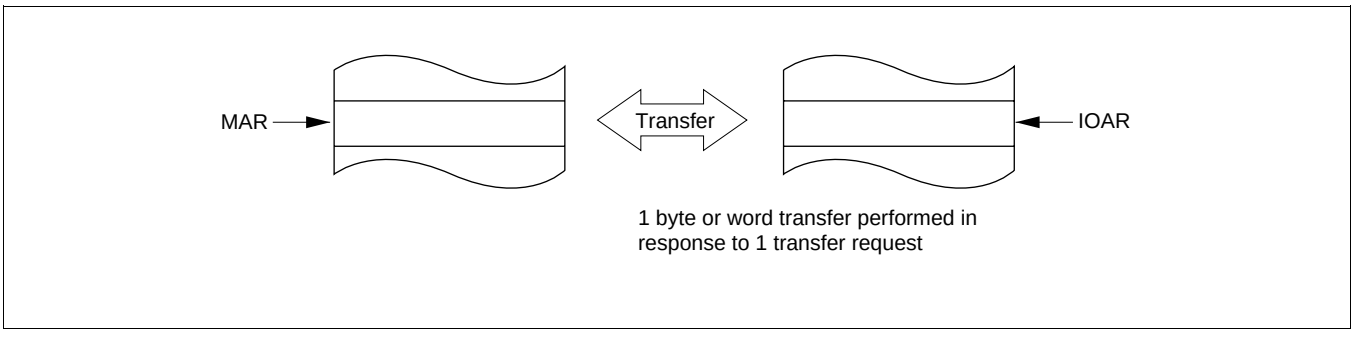


Figure 7-5 Operation in Idle Mode

Single Address Mode (Write): Figure 7-29 shows a transfer example in which $\overline{\text{TEND}}$ output is enabled and byte-size single address mode transfer (write) is performed from an external device to external 8-bit, 2-state access space.

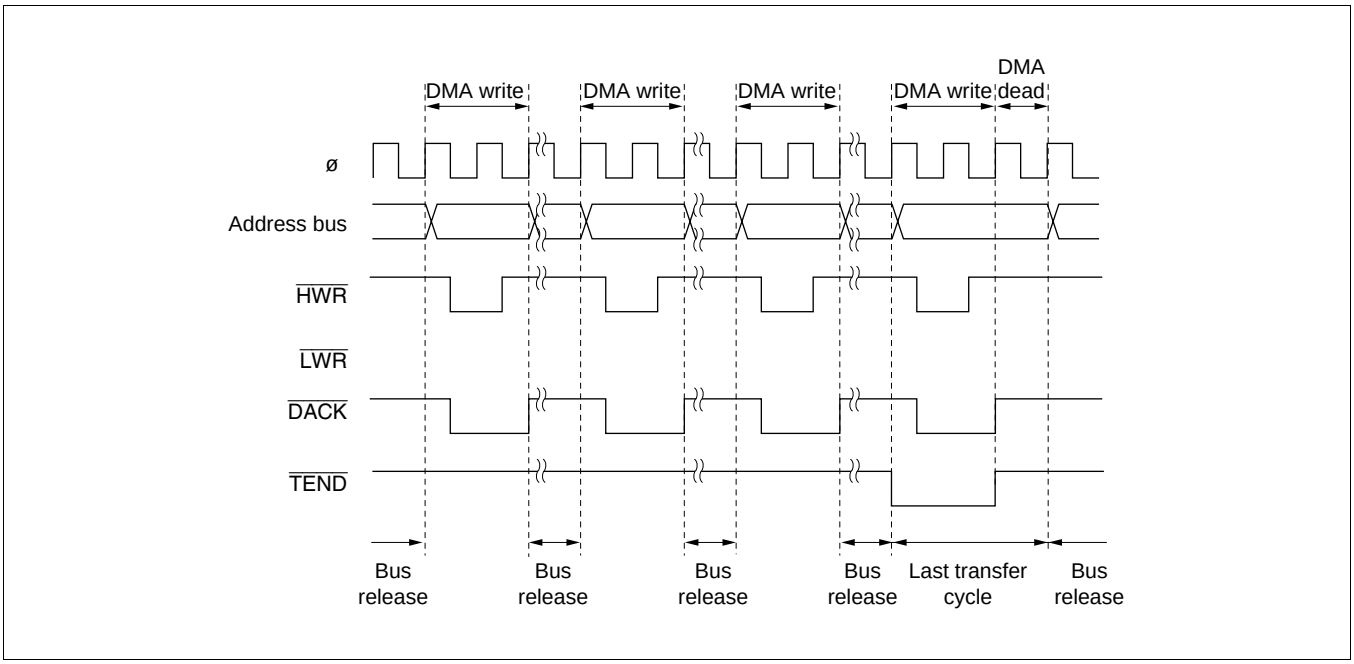


Figure 7-29 Example of Single Address Mode (Byte Write) Transfer

Figure 7-30 shows a transfer example in which $\overline{\text{TEND}}$ output is enabled and word-size single address mode transfer (write) is performed from an external device to external 8-bit, 2-state access space.

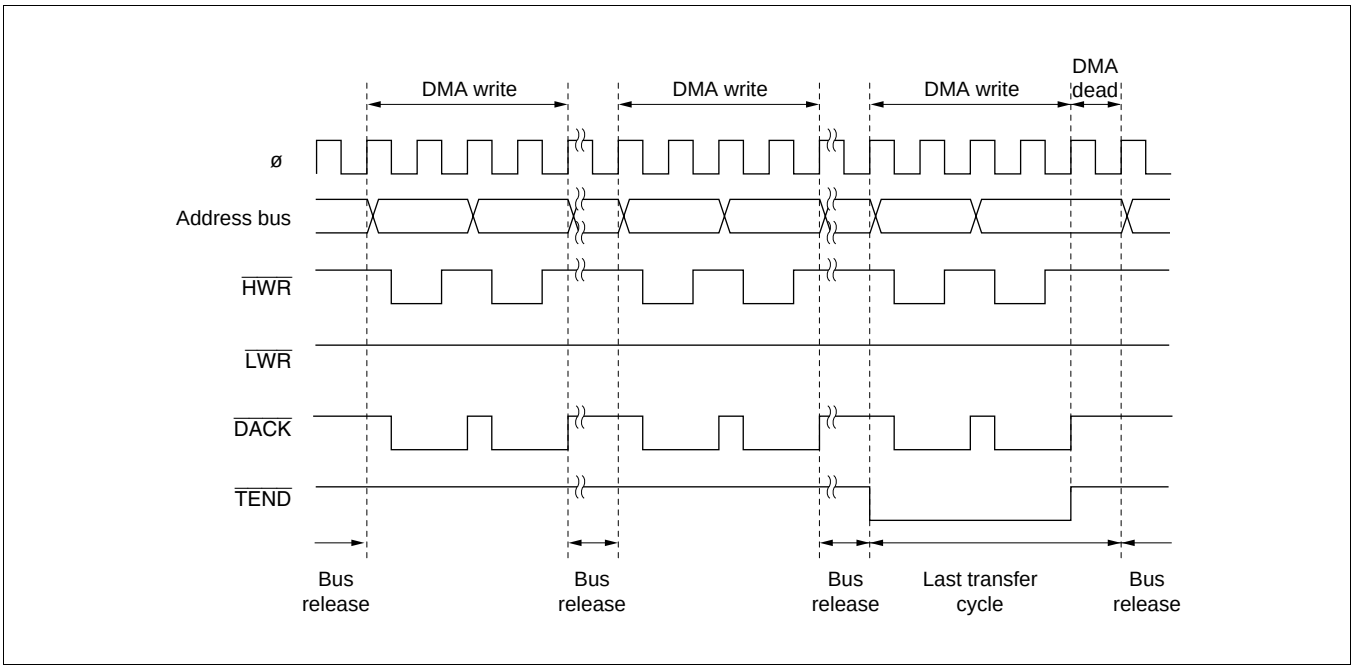


Figure 7-30 Example of Single Address Mode (Word Write) Transfer

A one-byte or one-word transfer is performed for one transfer request, and after the transfer the bus is released. While the bus is released one or more bus cycles are inserted by the CPU or DTC.

Section 9 I/O Ports

9.1 Overview

The H8S/2357 Group has 12 I/O ports (ports 1, 2, 3, 5, 6, and A to G), and one input-only port (port 4).

Table 9-1 summarizes the port functions. The pins of each port also have other functions.

Each port includes a data direction register (DDR) that controls input/output (not provided for the input-only port), a data register (DR) that stores output data, and a port register (PORT) used to read the pin states.

Ports A to E have a on-chip pull-up MOS function, and in addition to DR and DDR, have a MOS input pull-up control register (PCR) to control the on/off state of MOS input pull-up.

Port 3 and port A include an open-drain control register (ODR) that controls the on/off state of the output buffer PMOS.

Ports 1, and A to F can drive a single TTL load and 90 pF capacitive load, and ports 2, 3, 5, 6, and G can drive a single TTL load and 30 pF capacitive load. All the I/O ports can drive a Darlington transistor when in output mode. Ports 1, A, B, and C can drive an LED (10 mA sink current).

Port 2, and pins 6_4 to 6_7 and A_4 to A_7, are Schmitt-triggered inputs.

For block diagrams of the ports see Appendix C, I/O Port Block Diagrams.

9.7.3 Pin Functions

Port 6 pins also function as interrupt input pins ($\overline{IRQ0}$ to $\overline{IRQ3}$), DMAC I/O pins ($\overline{DREQ0}$, $\overline{TEND0}$, $\overline{DREQ1}$, and $\overline{TEND1}$), and bus control output pins ($\overline{CS4}$ to $\overline{CS7}$). Port 6 pin functions are shown in table 9-12.

Table 9-12 Port 6 Pin Functions

Pin	Selection Method and Pin Functions			
$P6_7/\overline{IRQ3}/\overline{CS7}$	The pin function is switched as shown below according to bit P67DDR.			
	Mode	Mode 7*		Modes 4 to 6*	
	P67DDR	0	1	0	1
	Pin function	$P6_7$ input pin	$P6_7$ output pin	$P6_7$ input pin	$\overline{CS7}$ output pin
		$\overline{IRQ3}$ interrupt input pin			
	Note: * Modes 6 and 7 are provided in the on-chip ROM version only.				
$P6_6/\overline{IRQ2}/\overline{CS6}$	The pin function is switched as shown below according to bit P66DDR.			
	Mode	Mode 7*		Modes 4 to 6*	
	P66DDR	0	1	0	1
	Pin function	$P6_6$ input pin	$P6_6$ output pin	$P6_6$ input pin	$\overline{CS6}$ output pin
		$\overline{IRQ2}$ interrupt input pin			
	Note: * Modes 6 and 7 are provided in the on-chip ROM version only.				
$P6_5/\overline{IRQ1}$	The pin function is switched as shown below according to bit P65DDR.			
	P65DDR	0		1	
	Pin function	$P6_5$ input pin		$P6_5$ output pin	
		$\overline{IRQ1}$ interrupt input pin			
$P6_4/\overline{IRQ0}$	The pin function is switched as shown below according to bit P64DDR.			
	P64DDR	0		1	
	Pin function	$P6_4$ input pin		$P6_4$ output pin	
		$\overline{IRQ0}$ interrupt input pin			

9.13.2 Register Configuration

Table 9-23 shows the port F register configuration.

Table 9-23 Port F Registers

Name	Abbreviation	R/W	Initial Value	Address *[1]
Port F data direction register	PFDDR	W	H'80/H'00*[2]	H'FEBE
Port F data register	PFDR	R/W	H'00	H'FF6E
Port F register	PORTF	R	Undefined	H'FF5E

Notes: 1. Lower 16 bits of the address.
2. Initial value depends on the mode.

Port F Data Direction Register (PFDDR)

Bit :	7	6	5	4	3	2	1	0
	PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR
Mode 7								
Initial value :	0	0	0	0	0	0	0	0
R/W :	W	W	W	W	W	W	W	W
Modes 4 to 6								
Initial value :	1	0	0	0	0	0	0	0
R/W :	W	W	W	W	W	W	W	W

PFDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port F. PFDDR cannot be read; if it is, an undefined value will be read.

PFDDR is initialized by a power-on reset, and in hardware standby mode, to H'80 in modes 4 to 6, and to H'00 in mode 7. It retains its prior state after a manual reset*, and in software standby mode. The OPE bit in SBYCR is used to select whether the bus control output pins retain their output state or become high-impedance when a transition is made to software standby mode.

Note: * Manual reset is only supported in the H8S/2357 ZTAT.

- Mode 7*

  Setting a PFDDR bit to 1 makes the corresponding port F pin PF_6 to PF_0 an output port, or in the case of pin PF_7, the ø output pin. Clearing the bit to 0 makes the pin an input port.

Note: * Modes 6 and 7 are provided in the on-chip ROM version only.

- Modes 4 to 6*

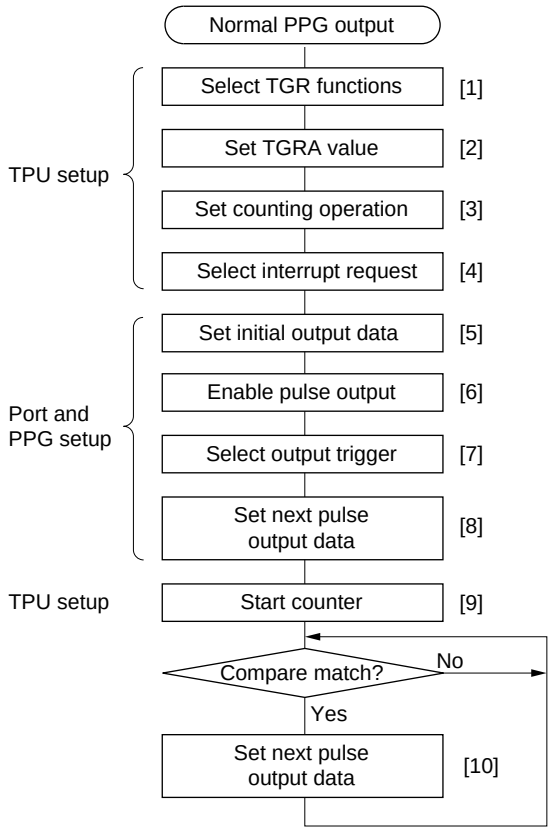
  Pin PF_7 functions as the ø output pin when the corresponding PFDDR bit is set to 1, and as an input port when the bit is cleared to 0.

  The input/output direction specified by PFDDR is ignored for pins PF_6 to PF_3, which are automatically designated as bus control outputs ($\overline{AS}$, $\overline{RD}$, $\overline{HWR}$, and $\overline{LWR}$).

  Pins PF_2 to PF_0 are designated as bus control input/output pins ($\overline{LCAS}$, $\overline{WAIT}$, $\overline{BREQO}$, $\overline{BACK}$, and $\overline{BREQ}$) by means of bus controller settings. At other times, setting a PFDDR bit to 1 makes the corresponding port F pin an output port, while clearing the bit to 0 makes the pin an input port.

11.3.3 Normal Pulse Output

Sample Setup Procedure for Normal Pulse Output: Figure 11-4 shows a sample procedure for setting up normal pulse output.



[1] Set TIOR to make TGRA an output compare register (with output disabled)

[2] Set the PPG output trigger period

[3] Select the counter clock source with bits TPSC2 to TPSC0 in TCR. Select the counter clear source with bits CCLR1 and CCLR0.

[4] Enable the TGIA interrupt in TIER. The DTC or DMAC can also be set up to transfer data to NDR.

[5] Set the initial output values in PODR.

[6] Set the DDR and NDER bits for the pins to be used for pulse output to 1.

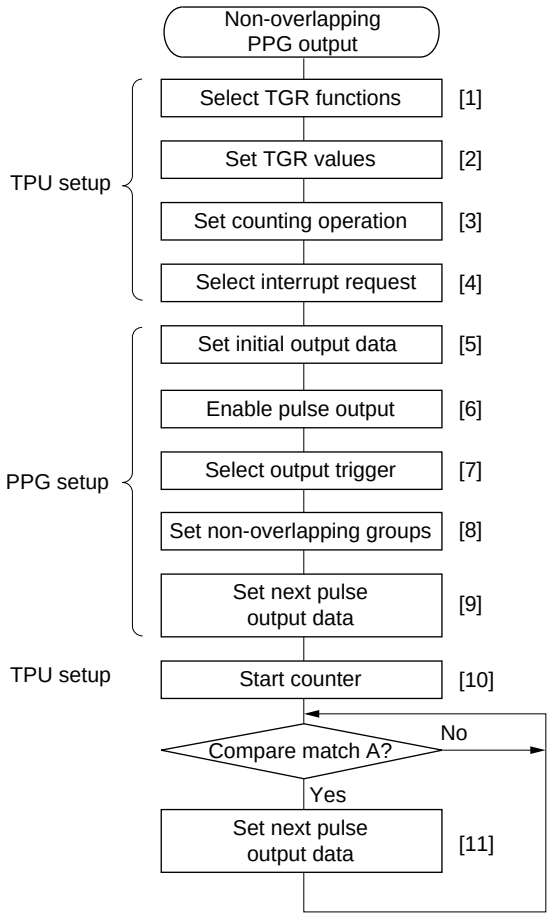
[7] Select the TPU compare match event to be used as the output trigger in PCR.

[8] Set the next pulse output values in NDR.

[9] Set the CST bit in TSTR to 1 to start the TCNT counter.

[10] At each TGIA interrupt, set the next output values in NDR.

Figure 11-4 Setup Procedure for Normal Pulse Output (Example)



[1] Set TIOR to make TGRA and TGRB an output compare registers (with output disabled)

[2] Set the pulse output trigger period in TGRB and the non-overlap margin in TGRA.

[3] Select the counter clock source with bits TPSC2 to TPSC0 in TCR. Select the counter clear source with bits CCLR1 and CCLR0.

[4] Enable the TGIA interrupt in TIER. The DTC or DMAC can also be set up to transfer data to NDR.

[5] Set the initial output values in PODR.

[6] Set the DDR and NDER bits for the pins to be used for pulse output to 1.

[7] Select the TPU compare match event to be used as the pulse output trigger in PCR.

[8] In PMR, select the groups that will operate in non-overlap mode.

[9] Set the next pulse output values in NDR.

[10] Set the CST bit in TSTR to 1 to start the TCNT counter.

[11] At each TGIA interrupt, set the next output values in NDR.

Figure 11-6 Setup Procedure for Non-Overlapping Pulse Output (Example)

Bit 0—Multiprocessor Bit Transfer (MPBT): When transmission is performed using multiprocessor format in asynchronous mode, MPBT stores the multiprocessor bit to be added to the transmit data.

The MPBT bit setting is invalid when multiprocessor format is not used, when not transmitting, and in clocked synchronous mode.

Bit 0 MPBT	Description	
0	Data with a 0 multiprocessor bit is transmitted	(Initial value)
1	Data with a 1 multiprocessor bit is transmitted	

14.2.8 Bit Rate Register (BRR)

Bit	:	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BRR is an 8-bit register that sets the serial transfer bit rate in accordance with the baud rate generator operating clock selected by bits CKS1 and CKS0 in SMR.

BRR can be read or written to by the CPU at all times.

BRR is initialized to H'FF by a reset, and by putting the device in standby mode or module stop mode. In the H8S/2398, H8S/2394, H8S/2392, and H8S/2390, however, the value in BRR is initialized to H'FF by a reset, or in hardware standby mode, but BRR retains its current state when the device enters software standby mode or module stop mode.

As baud rate generator control is performed independently for each channel, different values can be set for each channel.

Table 14-3 shows sample BRR settings in asynchronous mode, and table 14-4 shows sample BRR settings in clocked synchronous mode.

Table 14-3 BRR Settings for Various Bit Rates (Asynchronous Mode)

	ø = 2 MHz			ø = 2.097152 MHz			ø = 2.4576 MHz			ø = 3 MHz		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	1	141	0.03	1	148	–0.04	1	174	–0.26	1	212	0.03
150	1	103	0.16	1	108	0.21	1	127	0.00	1	155	0.16
300	0	207	0.16	0	217	0.21	0	255	0.00	1	77	0.16
600	0	103	0.16	0	108	0.21	0	127	0.00	0	155	0.16
1200	0	51	0.16	0	54	–0.70	0	63	0.00	0	77	0.16
2400	0	25	0.16	0	26	1.14	0	31	0.00	0	38	0.16
4800	0	12	0.16	0	13	–2.48	0	15	0.00	0	19	–2.34
9600	0	6	—	0	6	–2.48	0	7	0.00	0	9	–2.34
19200	0	2	—	0	2	—	0	3	0.00	0	4	–2.34
31250	0	1	0.00	0	1	—	0	1	—	0	2	0.00
38400	0	1	—	0	1	—	0	1	0.00	—	—	—

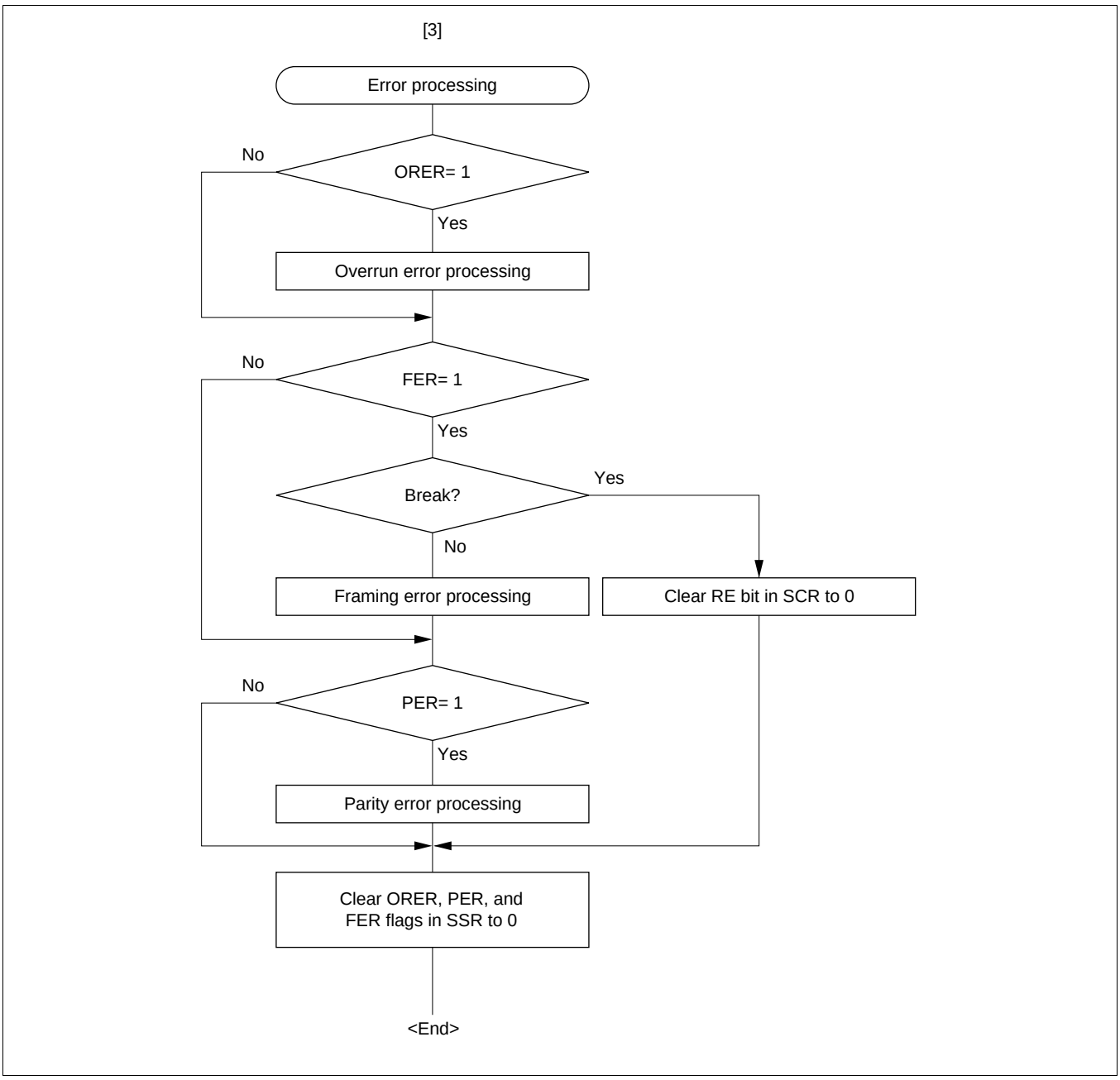
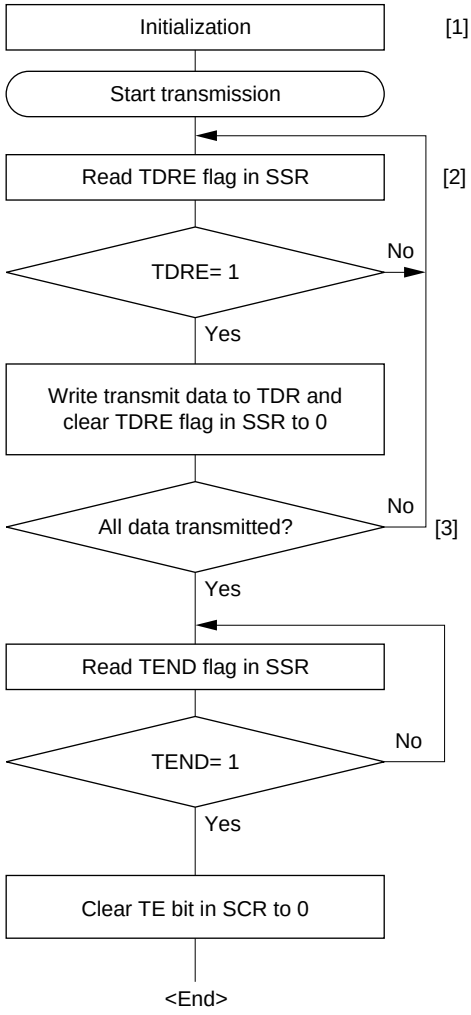


Figure 14-7 Sample Serial Reception Data Flowchart (cont)

- Serial data transmission (clocked synchronous mode)
  Figure 14-16 shows a sample flowchart for serial transmission.

  The following procedure should be used for serial data transmission.



[1] SCI initialization:
The TxD pin is automatically designated as the transmit data output pin.

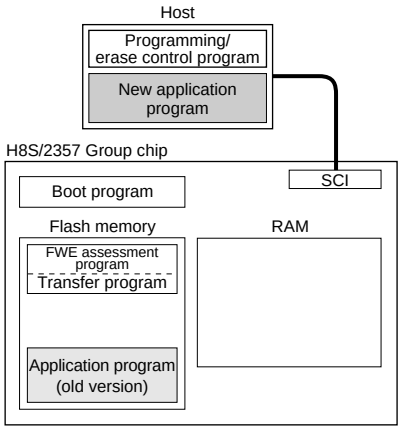
[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:
To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and then clear the TDRE flag to 0.
Checking and clearing of the TDRE flag is automatic when the DMAC or DTC is activated by a transmit data empty interrupt (TXI) request and data is written to TDR.

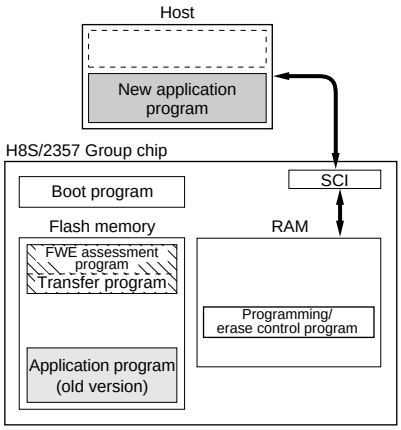
Figure 14-16 Sample Serial Transmission Flowchart

- User program mode

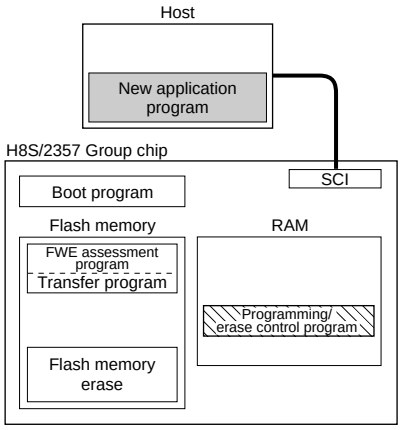
1. Initial state
   (1) The FWE assessment program that confirms that the FWE pin has been driven high, and (2) the program that will transfer the programming/ erase control program to on-chip RAM should be written into the flash memory by the user beforehand. (3) The programming/erase control program should be prepared in the host or in the flash memory.



2. Programming/erase control program transfer
   When the FWE pin is driven high, user software confirms this fact, executes the transfer program in the flash memory, and transfers the programming/erase control program to RAM.



3. Flash memory initialization
   The programming/erase program in RAM is executed, and the flash memory is initialized (to H'FF). Erasing can be performed in block units, but not in byte units.



4. Writing new application program
   Next, the new application program in the host is written into the erased flash memory blocks. Do not write to unerased blocks.

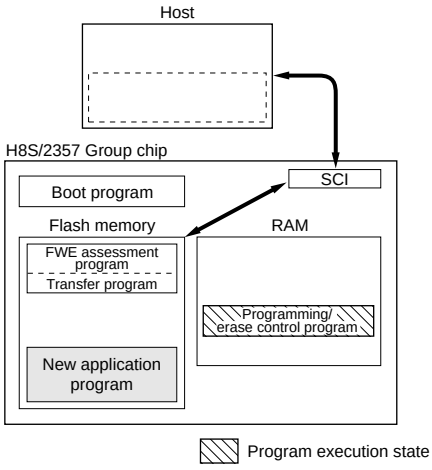


Figure 19-10 User Program Mode (Example)

19.6.4 Pin Configuration

The flash memory is controlled by means of the pins shown in table 19-10.

Table 19-10 Flash Memory Pins

Pin Name	Abbreviation	I/O	Function
Reset	$\overline{RES}$	Input	Reset
Flash write enable	FWE	Input	Flash program/erase protection by hardware
Mode 2	MD_2	Input	Sets MCU operating mode
Mode 1	MD_1	Input	Sets MCU operating mode
Mode 0	MD_0	Input	Sets MCU operating mode
Port 66	P66	Input	Sets MCU operating mode in programmer mode
Port 65	P65	Input	Sets MCU operating mode in programmer mode
Port 64	P64	Input	Sets MCU operating mode in programmer mode
Transmit data	TxD1	Output	Serial transmit data output
Receive data	RxD1	Input	Serial receive data input

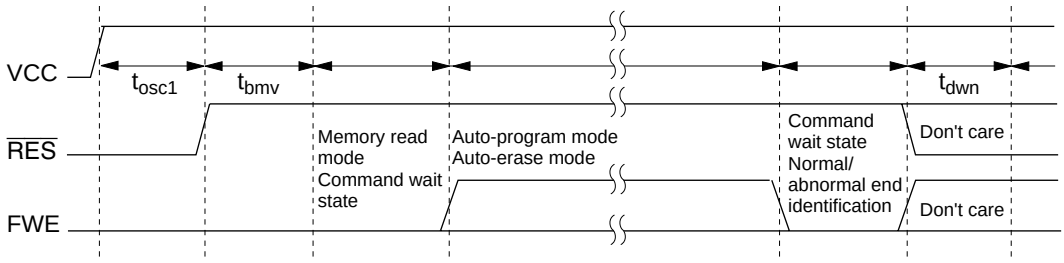
19.6.5 Register Configuration

The registers used to control the on-chip flash memory when enabled are shown in table 19-11.
In order for these registers to be accessed, the FLSHE bit must be set to 1 in SYSCR2 (except RAMER).

Table 19-11 Flash Memory Registers

Register Name	Abbreviation	R/W	Initial Value	Address*[1]
Flash memory control register 1	FLMCR1*[6]	R/W*[3]	H'00*[4]	H'FFC8*[2]
Flash memory control register 2	FLMCR2*[6]	R/W*[3]	H'00*[5]	H'FFC9*[2]
Erase block register 1	EBR1*[6]	R/W*[3]	H'00*[5]	H'FFCA*[2]
Erase block register 2	EBR2*[6]	R/W*[3]	H'00*[5]	H'FFCB*[2]
System control register 2	SYSCR2*[7]	R/W	H'00	H'FF42
RAM emulation register	RAMER	R/W	H'00	H'FEDB

Notes: 1. Lower 16 bits of the address.
2. Flash memory registers are selected by the FLSHE bit in system control register 2 (SYSCR2).
3. In modes in which the on-chip flash memory is disabled, a read will return H'00, and writes are invalid. Writes are also disabled when the FWE bit is cleared to 0 in FLMCR1.
4. When a high level is input to the FWE pin, the initial value is H'80.
5. When a low level is input to the FWE pin, or if a high level is input and the SWE bit in FLMCR1 is not set, these registers are initialized to H'00.
6. FLMCR1, FLMCR2, EBR1, and EBR2 are 8-bit registers. Only byte accesses are valid for these registers, the access requiring 2 states.
7. SYSCR2 is available only in the F-ZTAT version. In the masked ROM and ZTAT versions, this register cannot be written to and will return an undefined value if read.



Note: Except in auto-program mode and auto-erase mode, drive the FWE input pin low.

Figure 19-32 Oscillation Stabilization Time, Programmer Mode Setup Time, and Power Supply Fall Sequence

19.13.10 Notes on Memory Programming

- When programming addresses which have previously been programmed, carry out auto-erasing before auto-programming.
- When performing programming using PROM mode on a chip that has been programmed/erased in an on-board programming mode, auto-erasing is recommended before carrying out auto-programming.

Notes: 1. The flash memory is initially in the erased state when the device is shipped by Renesas Technology. For other chips for which the erasure history is unknown, it is recommended that auto-erasing be executed to check and supplement the initialization (erase) level.
2. Auto-programming should be performed once only on the same address block.

19.14 Flash Memory Programming and Erasing Precautions

Precautions concerning the use of on-board programming mode, the RAM emulation function, and PROM mode are summarized below.

Use the specified voltages and timing for programming and erasing: Applied voltages in excess of the rating can permanently damage the device. Use a PROM programmer that supports Renesas Technology microcomputer device types with 128-kbyte on-chip flash memory.

Do not select the HN28F101 setting for the PROM programmer, and only use the specified socket adapter. Incorrect use will result in damaging the device.

Powering on and off (see figures 19-33 to 19-35): Do not apply a high level to the FWE pin until V_{CC} has stabilized. Also, drive the FWE pin low before turning off V_{CC}.

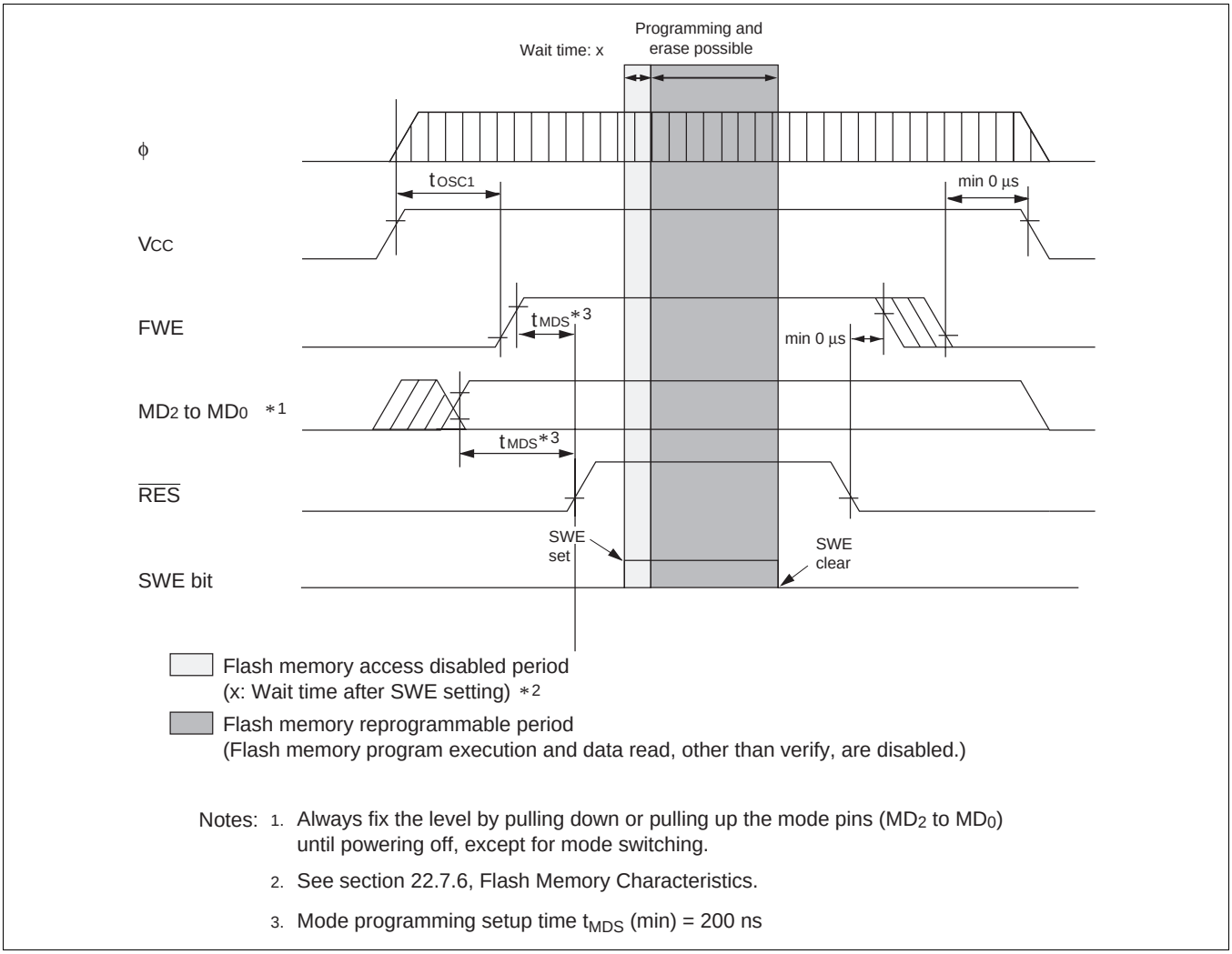
When applying or disconnecting V_{CC}, fix the FWE pin low and place the flash memory in the hardware protection state.

The power-on and power-off timing requirements should also be satisfied in the event of a power failure and subsequent recovery.

FWE application/disconnection (see figures 19-33 to 19-35): FWE application should be carried out when MCU operation is in a stable condition. If MCU operation is not stable, fix the FWE pin low and set the protection state.

The following points must be observed concerning FWE application and disconnection to prevent unintentional programming or erasing of flash memory:

- Apply FWE when the V_{CC} voltage has stabilized within its rated voltage range. Apply FWE when oscillation has stabilized (after the elapse of the oscillation settling time).
- In boot mode, apply and disconnect FWE during a reset.



Notes: 1. Always fix the level by pulling down or pulling up the mode pins (MD_2 to MD_0) until powering off, except for mode switching.

2. See section 22.7.6, Flash Memory Characteristics.

3. Mode programming setup time t_{MDS} (min) = 200 ns

Figure 19-33 Powering On/Off Timing (Boot Mode)

22.1.2 DC Characteristics

Table 22-2 lists the DC characteristics.
Table 22-3 lists the permissible output currents.

Table 22-2 DC Characteristics

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], Ta = -20 to +75°C (regular specifications), Ta = -40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Port 2, $P6_4$ to $P6_7$, PA_4 to PA_7	V_T^-	1.0	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Ports 1, 3, 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		2.0	—	V_{CC} + 0.3	V	
	Port 4		2.0	—	AV_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	0.5	V	
	NMI, EXTAL, Ports 1, 3 to 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		–0.3	—	0.8	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1, A to C		—	—	1.0	V	I_{OL} = 10 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD_2 to MD_0		—	—	1.0	µA	
	Port 4		—	—	1.0	µA	V_{in} = 0.5 V to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1 to 3, 5, 6, A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
MOS input pull-up current	Ports A to E	$-I_P$	50	—	300	µA	V_{in} = 0 V
Input capacitance	$\overline{RES}$	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	NMI		—	—	50	pF	
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)								Operation	Condition Code					No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa		I	H	N	Z	V	C	Advanced
BST	BST #xx:3,@aa:16	B						6			C→(#xx:3 of @aa:16)	—	—	—	—	—	—	5
	BST #xx:3,@aa:32	B						8			C→(#xx:3 of @aa:32)	—	—	—	—	—	—	6
BIST	BIST #xx:3,Rd	B	2								¬ C→(#xx:3 of Rd8)	—	—	—	—	—	—	1
	BIST #xx:3,@ERd	B			4						¬ C→(#xx:3 of @ERd)	—	—	—	—	—	—	4
	BIST #xx:3,@aa:8	B						4			¬ C→(#xx:3 of @aa:8)	—	—	—	—	—	—	4
	BIST #xx:3,@aa:16	B						6			¬ C→(#xx:3 of @aa:16)	—	—	—	—	—	—	5
	BIST #xx:3,@aa:32	B						8			¬ C→(#xx:3 of @aa:32)	—	—	—	—	—	—	6
BAND	BAND #xx:3,Rd	B	2								C∧(#xx:3 of Rd8)→C	—	—	—	—	—	↕	1
	BAND #xx:3,@ERd	B			4						C∧(#xx:3 of @ERd)→C	—	—	—	—	—	↕	3
	BAND #xx:3,@aa:8	B						4			C∧(#xx:3 of @aa:8)→C	—	—	—	—	—	↕	3
	BAND #xx:3,@aa:16	B						6			C∧(#xx:3 of @aa:16)→C	—	—	—	—	—	↕	4
	BAND #xx:3,@aa:32	B						8			C∧(#xx:3 of @aa:32)→C	—	—	—	—	—	↕	5
BIAND	BIAND #xx:3,Rd	B	2								C∧[¬ (#xx:3 of Rd8)]→C	—	—	—	—	—	↕	1
	BIAND #xx:3,@ERd	B			4						C∧[¬ (#xx:3 of @ERd)]→C	—	—	—	—	—	↕	3
	BIAND #xx:3,@aa:8	B						4			C∧[¬ (#xx:3 of @aa:8)]→C	—	—	—	—	—	↕	3
	BIAND #xx:3,@aa:16	B						6			C∧[¬ (#xx:3 of @aa:16)]→C	—	—	—	—	—	↕	4
	BIAND #xx:3,@aa:32	B						8			C∧[¬ (#xx:3 of @aa:32)]→C	—	—	—	—	—	↕	5
BOR	BOR #xx:3,Rd	B	2								C∨(#xx:3 of Rd8)→C	—	—	—	—	—	↕	1
	BOR #xx:3,@ERd	B			4						C∨(#xx:3 of @ERd)→C	—	—	—	—	—	↕	3

PDDDR—Port D Data Direction Register **H'FEBC** **Port D**
[On-chip ROM version Only]

Bit	:	7	6	5	4	3	2	1	0
		PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W

Specify input or output for individual port D pins

PEDDR—Port E Data Direction Register **H'FEBD** **Port E**

Bit	:	7	6	5	4	3	2	1	0
		PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W

Specify input or output for individual port E pins

PFDDR—Port F Data Direction Register **H'FEBE** **Port F**

Bit	:	7	6	5	4	3	2	1	0
		PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR
Modes 4 to 6									
Initial value	:	1	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W
Mode 7									
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W

Specify input or output for individual port F pins

PGDDR—Port G Data Direction Register **H'FEBF** **Port G**

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR
Modes 4, 5									
Initial value	:	Undefined	Undefined	Undefined	1	0	0	0	0
Read/Write	:	—	—	—	W	W	W	W	W
Modes 6, 7									
Initial value	:	Undefined	Undefined	Undefined	0	0	0	0	0
Read/Write	:	—	—	—	W	W	W	W	W

Specify input or output for individual port G pins

TCNT—Timer Counter **H'FFBC (W), H'FFBD (R)** **WDT**

Bit	:	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCNT is an 8-bit readable/writable* up-counter.

Note: * TCNT is write-protected by a password to prevent accidental overwriting. For details see section 13.2.4, Notes on Register Access.

RSTCSR—Reset Control/Status Register **H'FFBE (W) , H'FFBF (R)** **WDT**

Bit	:	7	6	5	4	3	2	1	0
		WOVF	RSTE	RSTS	—	—	—	—	—
Initial value	:	0	0	0	1	1	1	1	1
Read/Write	:	R/(W)*	R/W	R/W	—	—	—	—	—

Reset Select

0	Power-on reset
1	Manual reset*

Note: * Manual reset is not supported in the H8S/2357 (F-ZTAT and masked ROM versions) or the H8S/2352, H8S/2398, H8S/2394, H8S/2392 and H8S/2390. In these models, only 0 should be written to this bit.

Reset Enable

0	Reset signal is not generated if TCNT overflows*
1	Reset signal is generated if TCNT overflows

Note: * The modules H8S/2357 Group are not reset, but TCNT and TCSR in WDT are reset.

Watchdog Timer Overflow Flag

0	[Clearing condition] Cleared by reading RSTCSR when WOVF = 1, then writing 0 to WOVF
1	[Setting condition] Set when TCNT overflows (changed from H'FF to H'00) during watchdog timer operation

Note: * Can only be written with 0 for flag clearing.

The method for writing to RSTCSR is different from that for general registers to prevent accidental overwriting. For details see section 13.2.4, Notes on Register Access.