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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	87
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12352te20v

3.3.7 Mode 7 (Single-Chip Mode)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is enabled, but external addresses cannot be accessed.

All I/O ports are available for use as input-output ports.

3.3.8 Modes 8 and 9

Modes 8 and 9 are not supported in the H8S/2357 Group, and must not be set.

3.3.9 Mode 10 (H8S/2357 F-ZTAT Only)

This is a flash memory boot mode. For details, see section 19, ROM.

MCU operation is the same as in mode 6.

3.3.10 Mode 11 (H8S/2357 F-ZTAT Only)

This is a flash memory boot mode. For details, see section 19, ROM.

MCU operation is the same as in mode 7.

3.3.11 Modes 12 and 13 (H8S/2357 F-ZTAT Only)

Modes 12 and 13 are not supported in the H8S/2357 Group, and must not be set.

3.3.12 Mode 14 (H8S/2357 F-ZTAT Only)

This is a flash memory user program mode. For details, see section 19, ROM.

MCU operation is the same as in mode 6.

3.3.13 Mode 15 (H8S/2357 F-ZTAT Only)

This is a flash memory user program mode. For details, see section 19, ROM.

MCU operation is the same as in mode 7.

5.2.4 IRQ Sense Control Registers H and L (ISCRH, ISCRL)

ISCRH

Bit	:	15	14	13	12	11	10	9	8
		IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ISCRL

Bit	:	7	6	5	4	3	2	1	0
		IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ISCR registers are 16-bit readable/writable registers that select rising edge, falling edge, or both edge detection, or level sensing, for the input at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$.

ISCR registers are initialized to H'0000 by a reset and in hardware standby mode.

Bits 15 to 0: IRQ7 Sense Control A and B (IRQ7SCA, IRQ7SCB) to IRQ0 Sense Control A and B (IRQ0SCA, IRQ0SCB)

Bits 15 to 0

IRQ7SCB to IRQ0SCB	IRQ7SCA to IRQ0SCA	Description
0	0	Interrupt request generated at $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input low level (Initial value)
	1	Interrupt request generated at falling edge of $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input
1	0	Interrupt request generated at rising edge of $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input
	1	Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input

5.2.5 IRQ Status Register (ISR)

Bit	:	7	6	5	4	3	2	1	0
		IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only 0 can be written, to clear the flag.

ISR is an 8-bit readable/writable register that indicates the status of IRQ7 to IRQ0 interrupt requests.

ISR is initialized to H'00 by a reset and in hardware standby mode.

Bits 7 to 0—IRQ7 to IRQ0 flags (IRQ7F to IRQ0F): These bits indicate the status of IRQ7 to IRQ0 interrupt requests.

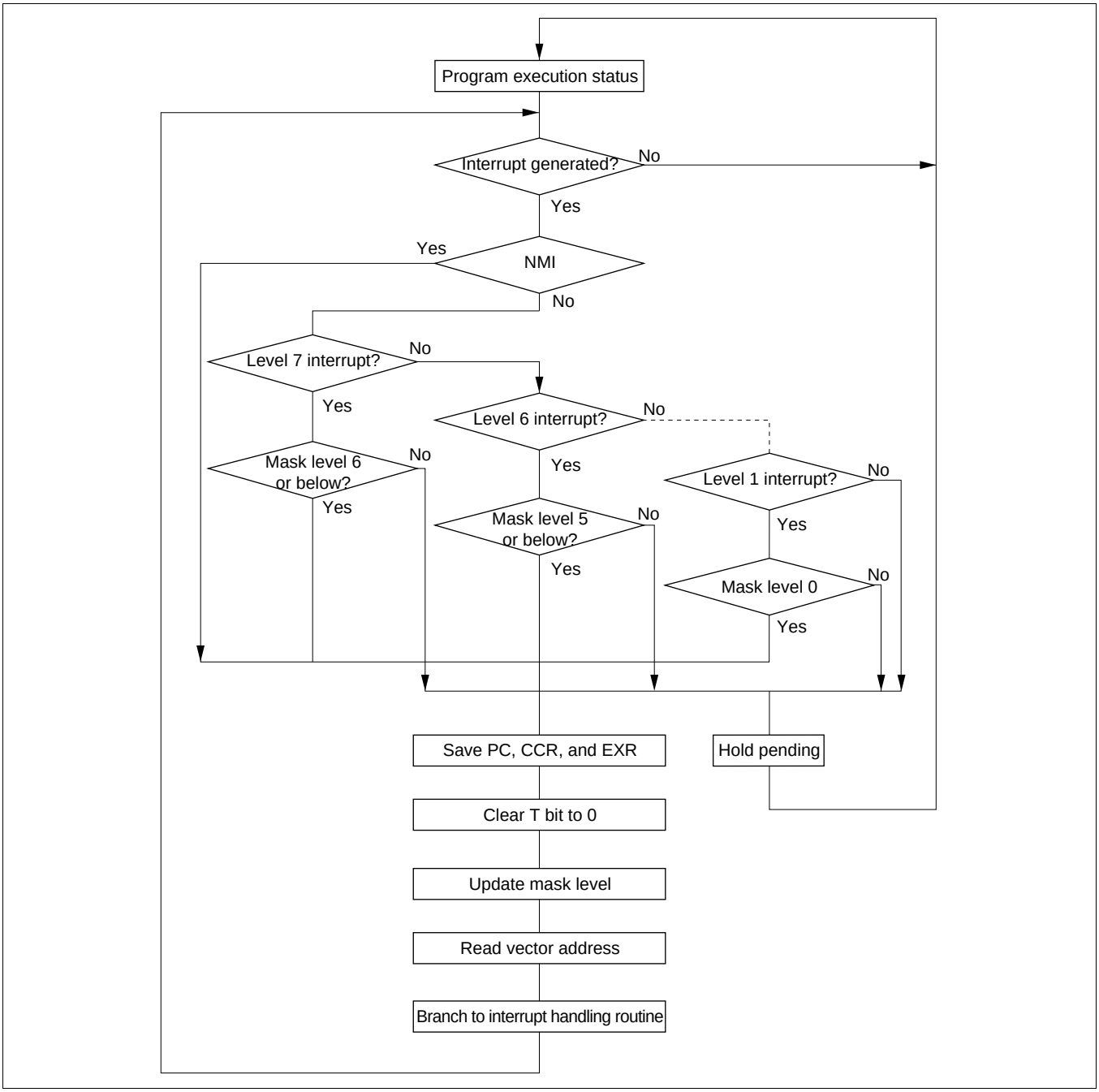


Figure 5-6 Flowchart of Procedure Up to Interrupt Acceptance in Interrupt Control Mode 2

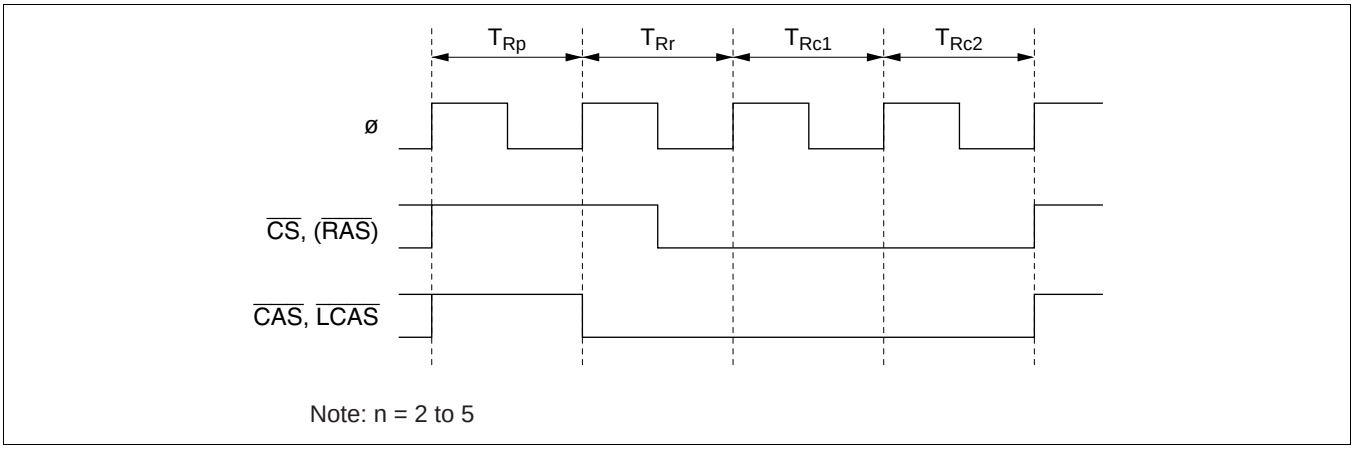


Figure 6-25 CBR Refresh Timing

When the RCW bit is set to 1, $\overline{RAS}$ signal output is delayed by one cycle. The width of the $\overline{RAS}$ signal should be adjusted with bits RLW1 and RLW0. These bits are only enabled in refresh operations.

Figure 6-26 shows the timing when the RCW bit is set to 1.

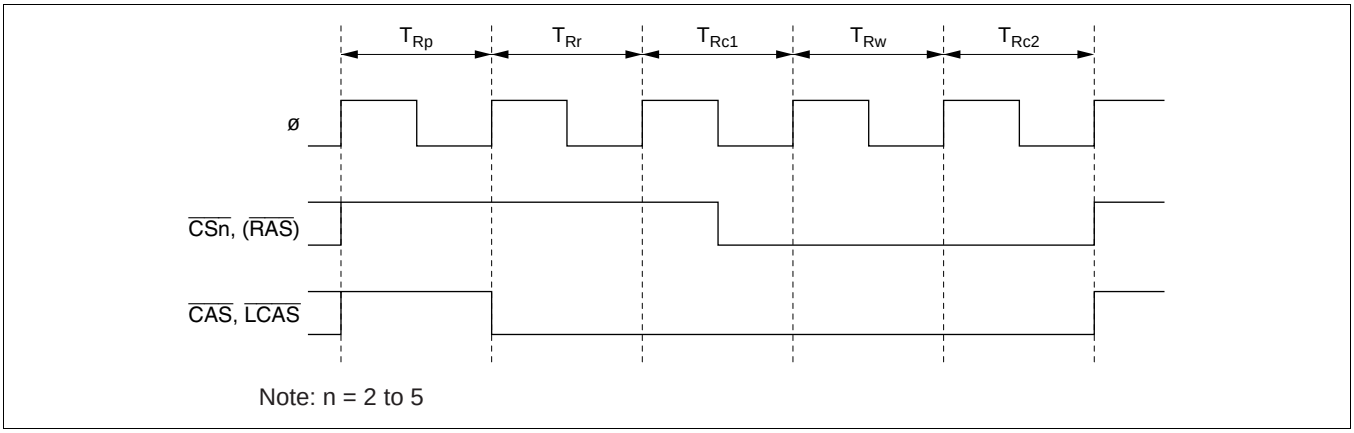


Figure 6-26 CBR Refresh Timing (When RCW = 1, RLW1 = 0, RLW0 = 1)

Self-Refreshing: A self-refresh mode (battery backup mode) is provided for DRAM as a kind of standby mode. In this mode, refresh timing and refresh addresses are generated within the DRAM.

To select self-refreshing, set the RFSHE bit and RMODE bit in DRAMCR to 1. Then, when a SLEEP instruction is executed to enter software standby mode, the $\overline{CAS}$ and $\overline{RAS}$ signals are output and DRAM enters self-refresh mode, as shown in figure 6-27.

When software standby mode is exited, the RMODE bit is cleared to 0 and self-refresh mode is cleared.

When switching to software standby mode, if there is a CBR refresh request, CBR refreshing is executed before self-refresh mode is entered.

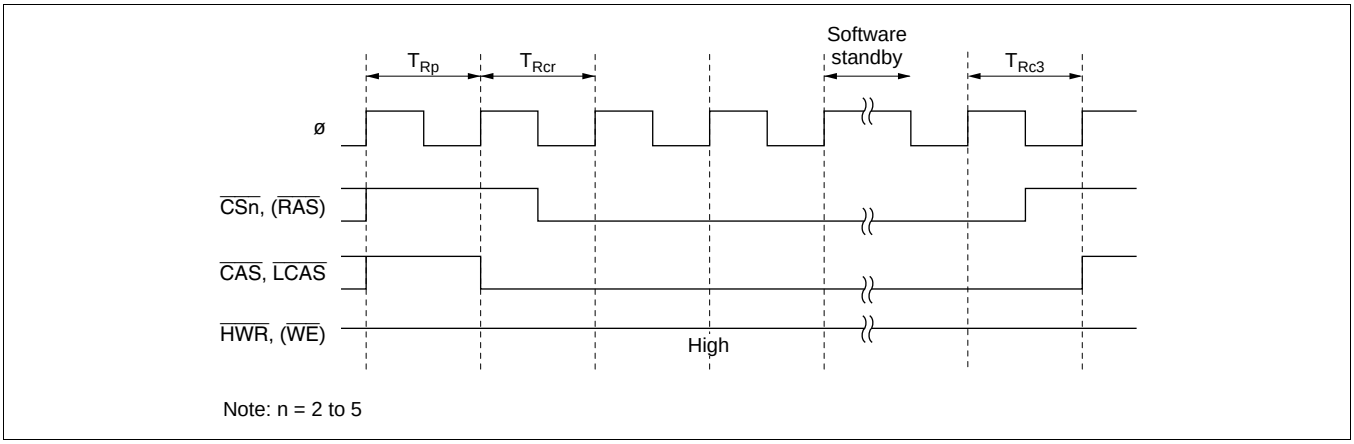


Figure 6-27 Self-Refresh Timing (When CW2 = 1, or CW2 = 0 and LCASS = 0)

6.6 DMAC Single Address Mode and DRAM Interface

When burst mode is selected with the DRAM interface, the $\overline{DACK}$ output timing can be selected with the DDS bit. When DRAM space is accessed in DMAC single address mode at the same time, whether or not burst access is to be performed is selected.

6.6.1 When DDS = 1

Burst access is performed by determining the address only, irrespective of the bus master. The $\overline{DACK}$ output goes low from the T_{C1} state in the case of the DRAM interface.

Figure 6-28 shows the $\overline{DACK}$ output timing for the DRAM interface when DDS = 1.

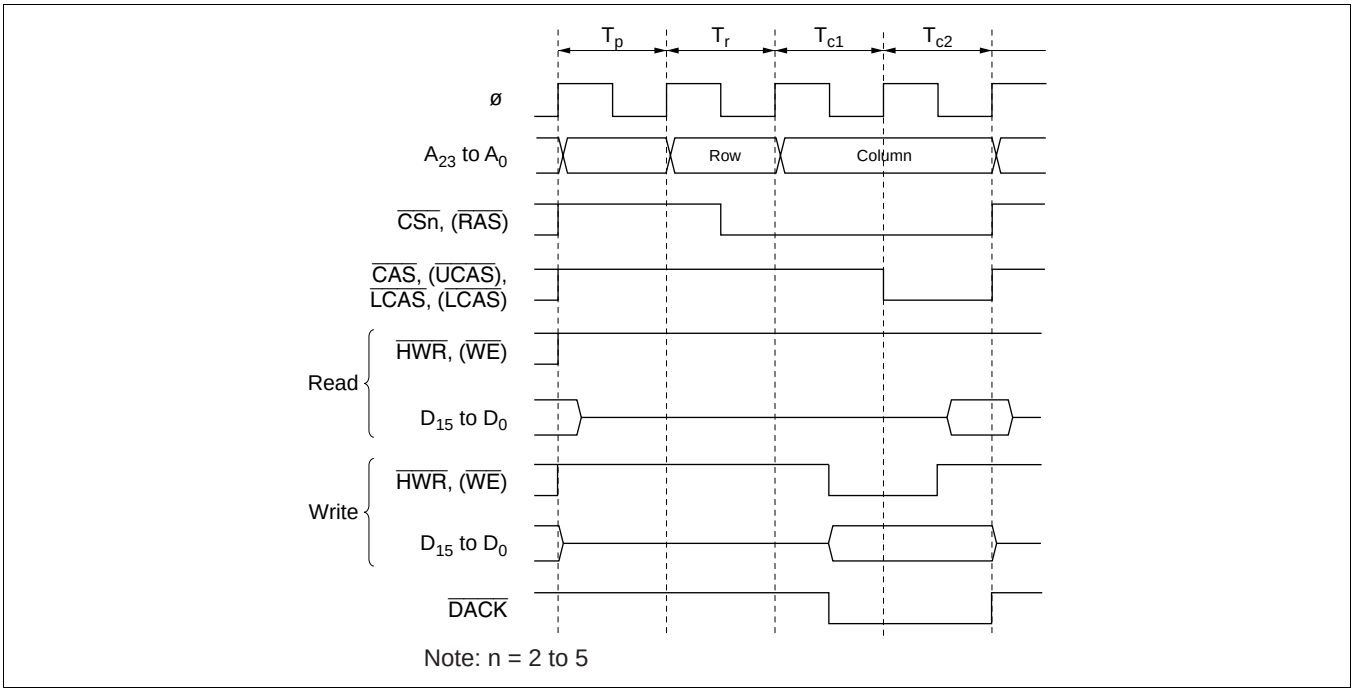


Figure 6-28 $\overline{DACK}$ Output Timing when DDS = 1 (Example of DRAM Access)

7.3 Register Descriptions (2) (Full Address Mode)

Full address mode transfer is performed with channels A and B together. For details of full address mode setting, see table 7-4.

7.3.1 Memory Address Register (MAR)

Bit	:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR	:	—	—	—	—	—	—	—	—								
Initial value	:	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
R/W	:	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR	:																
Initial value	:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

*: Undefined

MAR is a 32-bit readable/writable register; MARA functions as the transfer source address register, and MARB as the destination address register.

MAR is composed of two 16-bit registers, MARH and MARL. The upper 8 bits of MARH are reserved; they are always read as 0, and cannot be modified.

MAR is incremented or decremented each time a byte or word transfer is executed, so that the source or destination memory address can be updated automatically. For details, see section 7.3.4, DMA Control Register (DMACR).

MAR is not initialized by a reset or in standby mode.

7.3.2 I/O Address Register (IOAR)

IOAR is not used in full address transfer.

7.3.3 Execute Transfer Count Register (ETCR)

ETCR is a 16-bit readable/writable register that specifies the number of transfers. The function of this register is different in normal mode and in block transfer mode.

ETCR is not initialized by a reset or in standby mode.

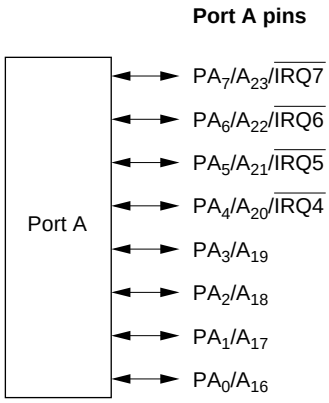
9.8 Port A

9.8.1 Overview

Port A is an 8-bit I/O port. Port A pins also function as address bus outputs and interrupt input pins ($\overline{IRQ4}$ to $\overline{IRQ7}$). The pin functions change according to the operating mode.

Port A has a on-chip MOS input pull-up function that can be controlled by software. Pins PA_7 to PA_4 are schmitt-triggered inputs.

Figure 9-7 shows the port A pin configuration.



Pin functions in mode 7*

PA_7 (I/O)/$\overline{IRQ7}$ (input)	
PA_6 (I/O)/$\overline{IRQ6}$ (input)	
PA_5 (I/O)/$\overline{IRQ5}$ (input)	
PA_4 (I/O)/$\overline{IRQ4}$ (input)	
PA_3 (I/O)	
PA_2 (I/O)	
PA_1 (I/O)	
PA_0 (I/O)	

Pin functions in mode 6*	**Pin functions in modes 4 and 5**
PA_7 (input)/A_{23} (output)/$\overline{IRQ7}$ (input)	PA_7 (input)/A_{23}(output)/$\overline{IRQ7}$ (input)
PA_6 (input)/A_{22} (output)/$\overline{IRQ6}$ (input)	PA_6 (input)/A_{22}(output)/$\overline{IRQ6}$ (input)
PA_5 (input)/A_{21} (output)/$\overline{IRQ5}$ (input)	PA_5 (input)/A_{21} (output)/$\overline{IRQ5}$ (input)
PA_4 (input)/A_{20} (output)/$\overline{IRQ4}$ (input)	A_{20} (output)
PA_3 (input)/A_{19} (output)	A_{19} (output)
PA_2 (input)/A_{18} (output)	A_{18} (output)
PA_1 (input)/A_{17} (output)	A_{17} (output)
PA_0 (input)/A_{16} (output)	A_{16} (output)

Note: * Modes 6 and 7 are provided in the on-chip ROM version only.

Figure 9-7 Port A Pin Functions

10.6.2 Interrupt Signal Timing

TGF Flag Setting Timing in Case of Compare Match: Figure 10-42 shows the timing for setting of the TGF flag in TSR by compare match occurrence, and TGI interrupt request signal timing.

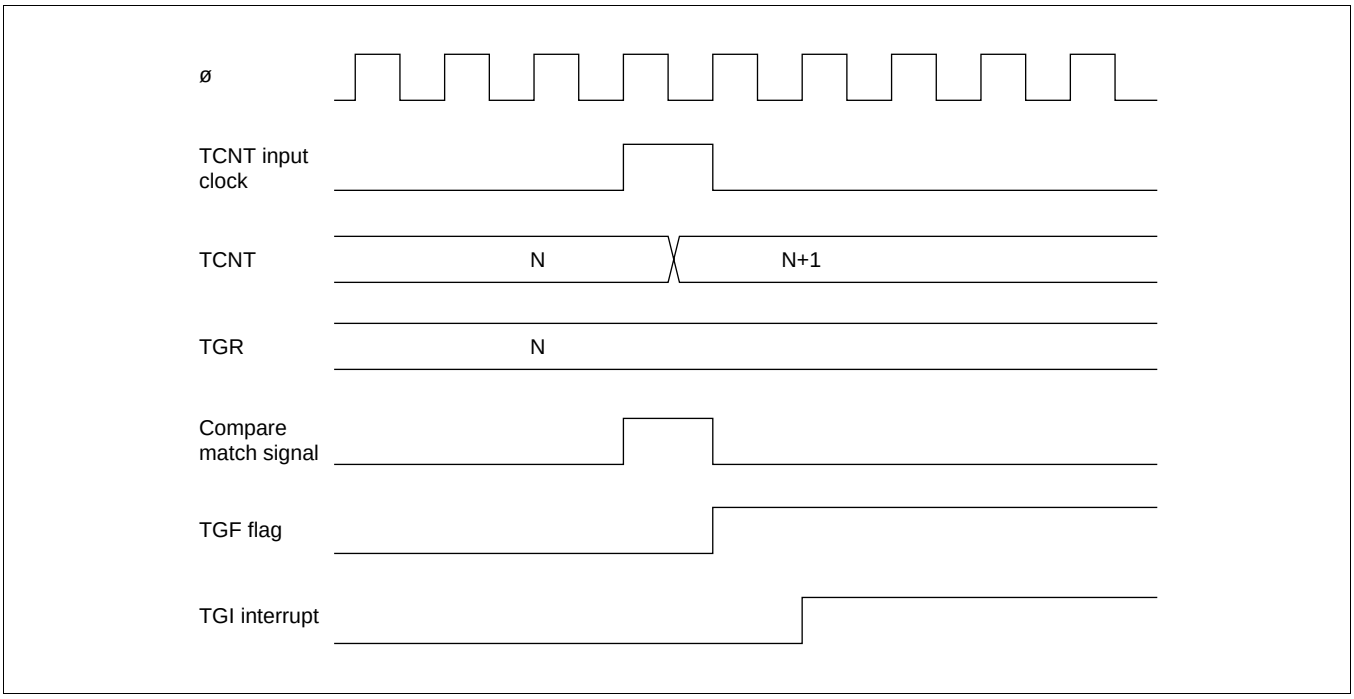


Figure 10-42 TGI Interrupt Timing (Compare Match)

TGF Flag Setting Timing in Case of Input Capture: Figure 10-43 shows the timing for setting of the TGF flag in TSR by input capture occurrence, and TGI interrupt request signal timing.

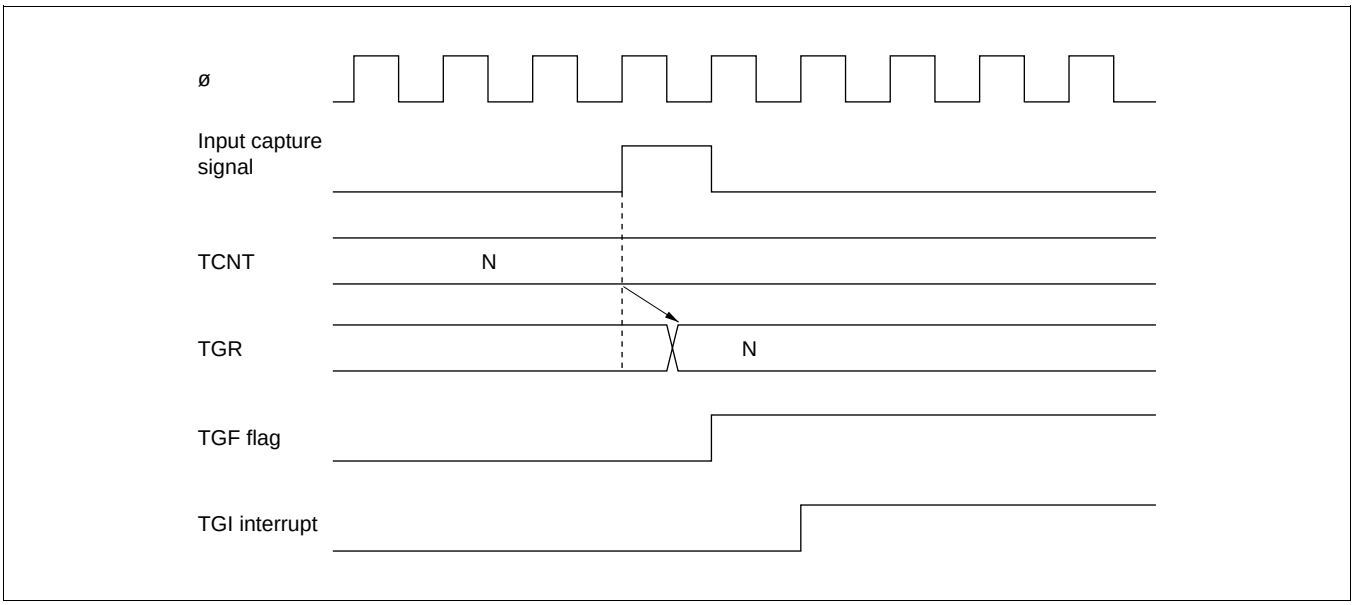


Figure 10-43 TGI Interrupt Timing (Input Capture)

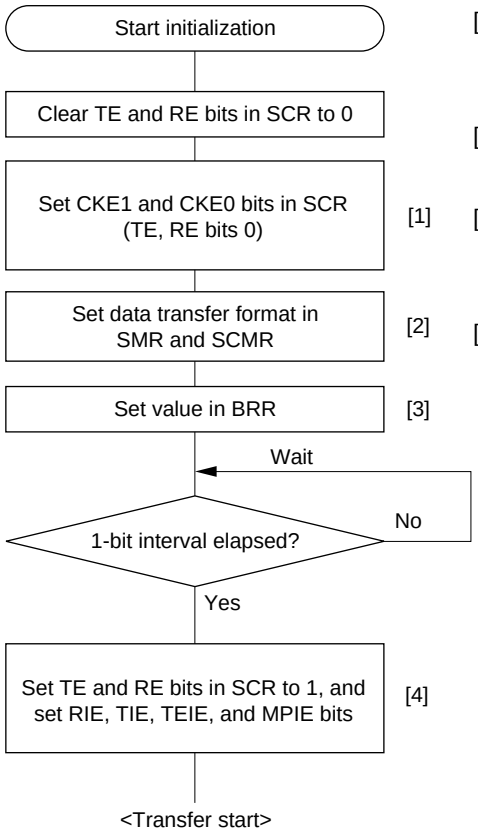
Data Transfer Operations:

- SCI initialization (clocked synchronous mode)

  Before transmitting and receiving data, you should first clear the TE and RE bits in SCR to 0, then initialize the SCI as described below.

  When the operating mode, transfer format, etc., is changed, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag is set to 1 and TSR is initialized. Note that clearing the RE bit to 0 does not change the contents of the RDRF, PER, FER, and ORER flags, or the contents of RDR.

  Figure 14-15 shows a sample SCI initialization flowchart.



[1] Set the clock selection in SCR. Be sure to clear bits RIE, TIE, TEIE, and MPIE, TE and RE, to 0.

[2] Set the data transfer format in SMR and SCMR.

[3] Write a value corresponding to the bit rate to BRR. Not necessary if an external clock is used.

[4] Wait at least one bit interval, then set the TE bit or RE bit in SCR to 1. Also set the RIE, TIE, TEIE, and MPIE bits.
Setting the TE and RE bits enables the TxD and RxD pins to be used.

Note: In simultaneous transmit and receive operations, the TE and RE bits should both be cleared to 0 or set to 1 simultaneously.

Figure 14-15 Sample SCI Initialization Flowchart

(1) Clock Timing

Table 22-14 lists the clock timing

Table 22-14 Clock Timing

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, ø = 10 to 20 MHz, T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Item	Symbol	Condition		Unit	Test Conditions
		Min	Max		
Clock cycle time	t_{cyc}	50	100	ns	Figure 22-36
Clock high pulse width	t_{CH}	20	—	ns	
Clock low pulse width	t_{CL}	20	—	ns	
Clock rise time	t_{Cr}	—	5	ns	
Clock fall time	t_{Cf}	—	5	ns	
Clock oscillator setting time at reset (crystal)	t_{OSC1}	10	—	ms	Figure 22-37
Clock oscillator setting time in software standby (crystal)	t_{OSC2}	10	—	ms	Figure 21-2
External clock output stabilization delay time	t_{DEXT}	500	—	µs	Figure 22-37

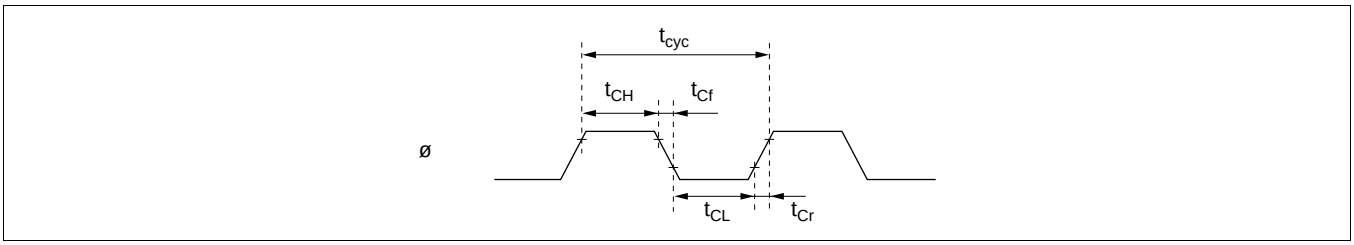


Figure 22-36 System Clock Timing

22.7.5 D/A Conversion Characteristics

Table 22-42 lists the D/A conversion characteristics

Table 22-42 D/A Conversion Characteristics

Condition B: $V_{CC} = AV_{CC} = 5.0\ V \pm 10\%$, $V_{ref} = 4.5\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$,
ø = 2 to 20 MHz, $T_a = –20$ to +75°C (regular specifications),
$T_a = –40$ to +85°C (wide-range specifications)

Condition C: $V_{CC} = AV_{CC} = 3.0\ V$ to $5.5\ V$, $V_{ref} = 3.0\ V$ to AV_{CC},
$V_{SS} = AV_{SS} = 0\ V$, ø = 2 to 13 MHz, $T_a = –20$ to +75°C (regular specifications),
$T_a = –40$ to +85°C (wide-range specifications)

	Condition B			Condition C				
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Resolution	8	8	8	8	8	8	bit	
Conversion time	—	—	10	—	—	10	µs	20-pF capacitive load
Absolute accuracy	—	±1.0	±1.5	—	±2.0	±3.0	LSB	2-MΩ resistive load
	—	—	±1.0	—	—	±2.0	LSB	4-MΩ resistive load

22.7.6 Flash Memory Characteristics

Table 22-43 shows the flash memory characteristics.

Table 22-43 Flash Memory Characteristics (1)

Conditions: $V_{CC} = 5.0\ V \pm 10\%$, $AV_{CC} = 5.0\ V \pm 10\%$, $V_{ref} = 4.5\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0V$
$T_a = 0$ to +75°C (Programming/erasing operating temperature, regular specifications), $T_a = 0$ to + 85°C (Programming/erasing operating temperature, wide-range specifications)

Item		**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**
Programming time*1*2*4		t_P	—	10	200	ms/32 bytes	
Erase time*1*3*5		t_E	—	100	1200	ms/block	
Reprogramming count		N_{WEC}	—	—	100	Times	
Programming	Wait time after SWE bit setting*1	x	10	—	—	µs	
	Wait time after PSU bit setting*1	y	50	—	—	µs	
	Wait time after P bit setting*1*4	z	150	—	200	µs	
	Wait time after P bit clear*1	α	10	—	—	µs	
	Wait time after PSU bit clear*1	β	10	—	—	µs	
	Wait time after PV bit setting*1	γ	4	—	—	µs	
	Wait time after H'FF dummy write*1	ε	2	—	—	µs	

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Programming	Wait time after SWE bit setting*[1]	x	10	—	—	µs	
	Wait time after PSU bit setting*[1]	y	50	—	—	µs	
	Wait time after P bit setting*[1]*[4]	z	150	—	200	µs	
	Wait time after P bit clear*[1]	α	10	—	—	µs	
	Wait time after PSU bit clear*[1]	β	10	—	—	µs	
	Wait time after PV bit setting*[1]	γ	4	—	—	µs	
	Wait time after H'FF dummy write*[1]	ε	2	—	—	µs	
	Wait time after PV bit clear*[1]	η	4	—	—	µs	
	Maximum programming count*[1]*[4]	N	—	—	1000 *[5]	Times	Z = 200 µs
Erase	Wait time after SWE bit setting*[1]	x	10	—	—	µs	
	Wait time after ESU bit setting*[1]	y	200	—	—	µs	
	Wait time after E bit setting*[1]*[6]	z	5	—	10	ms	
	Wait time after E bit clear*[1]	α	10	—	—	µs	
	Wait time after ESU bit clear*[1]	β	10	—	—	µs	
	Wait time after EV bit setting*[1]	γ	20	—	—	µs	
	Wait time after H'FF dummy write*[1]	ε	2	—	—	µs	
	Wait time after EV bit clear*[1]	η	5	—	—	µs	
	Maximum erase count*[1]*[6]	N	120	—	240	Times	

Notes: 1. Set the times according to the program/erase algorithms.

2. Programming time per 32 bytes (Shows the total time the flash memory control register (FLMCR) is set. It does not include the programming verification time.)
3. Block erase time (Shows the period the E bit in FLMCR is set. It does not include the erase verification time.)
4. Maximum programming time
   (t_p (max)=wait time after P-bit setting (Z) × maximum programming count (N))
5. Number of times when the wait time after P bit setting (z) = 200 µs.
   The maximum number of writes (N) should be set according to the actual set value of z so as not to exceed the maximum programming time (t_P(max)).
6. For the maximum erase time (t_E(max)), the following relationship applies between the wait time after E bit setting (z) and the maximum number of erases (N):
   t_E(max) = Wait time after E bit setting (z) × maximum number of erases (N)
   The values of z and N should be set so as to satisfy the above formula.
   Examples: When z = 5 [ms], N = 240 times
   When z = 10 [ms], N = 120 times

Instruction	Mnemonic	Size	Instruction Format																	
			1st byte		2nd byte		3rd byte		4th byte		5th byte		6th byte		7th byte		8th byte		9th byte	10th byte
BCLR	BCLR #xx:3,Rd	B	7	2	0 IMM	rd														
	BCLR #xx:3,@ERd	B	7	D	0 erd	0	7	2	0 IMM	0										
	BCLR #xx:3,@aa:8	B	7	F	abs		7	2	0 IMM	0										
	BCLR #xx:3,@aa:16	B	6	A	1	8	abs				7	2	0 IMM	0						
	BCLR #xx:3,@aa:32	B	6	A	3	8	abs								7	2	0 IMM	0		
	BCLR Rn,Rd	B	6	2	rn	rd														
	BCLR Rn,@ERd	B	7	D	0 erd	0	6	2	rn	0										
	BCLR Rn,@aa:8	B	7	F	abs		6	2	rn	0										
	BCLR Rn,@aa:16	B	6	A	1	8	abs				6	2	rn	0						
	BCLR Rn,@aa:32	B	6	A	3	8	abs								6	2	rn	0		
BIAND	BIAND #xx:3,Rd	B	7	6	1 IMM	rd														
	BIAND #xx:3,@ERd	B	7	C	0 erd	0	7	6	1 IMM	0										
	BIAND #xx:3,@aa:8	B	7	E	abs		7	6	1 IMM	0										
	BIAND #xx:3,@aa:16	B	6	A	1	0	abs				7	6	1 IMM	0						
	BIAND #xx:3,@aa:32	B	6	A	3	0	abs								7	6	1 IMM	0		
BILD	BILD #xx:3,Rd	B	7	7	1 IMM	rd														
	BILD #xx:3,@ERd	B	7	C	0 erd	0	7	7	1 IMM	0										
	BILD #xx:3,@aa:8	B	7	E	abs		7	7	1 IMM	0										
	BILD #xx:3,@aa:16	B	6	A	1	0	abs				7	7	1 IMM	0						
	BILD #xx:3,@aa:32	B	6	A	3	0	abs								7	7	1 IMM	0		
BIOR	BIOR #xx:3,Rd	B	7	4	1 IMM	rd														
	BIOR #xx:3,@ERd	B	7	C	0 erd	0	7	4	1 IMM	0										
	BIOR #xx:3,@aa:8	B	7	E	abs		7	4	1 IMM	0										
	BIOR #xx:3,@aa:16	B	6	A	1	0	abs				7	4	1 IMM	0						
	BIOR #xx:3,@aa:32	B	6	A	3	0	abs								7	4	1 IMM	0		

Instruction	Mnemonic	Instruction Fetch	Branch Address Read	Stack Operation	Byte Data Access	Word Data Access	Internal Operation
		I	J	K	L	M	N
MOV	MOV.B Rs,@-ERd	1			1		1
	MOV.B Rs,@aa:8	1			1		
	MOV.B Rs,@aa:16	2			1		
	MOV.B Rs,@aa:32	3			1		
	MOV.W #xx:16,Rd	2					
	MOV.W Rs,Rd	1					
	MOV.W @ERs,Rd	1				1	
	MOV.W @(d:16,ERs),Rd	2				1	
	MOV.W @(d:32,ERs),Rd	4				1	
	MOV.W @ERs+,Rd	1				1	1
	MOV.W @aa:16,Rd	2				1	
	MOV.W @aa:32,Rd	3				1	
	MOV.W Rs,@ERd	1				1	
	MOV.W Rs,@(d:16,ERd)	2				1	
	MOV.W Rs,@(d:32,ERd)	4				1	
	MOV.W Rs,@-ERd	1				1	1
	MOV.W Rs,@aa:16	2				1	
	MOV.W Rs,@aa:32	3				1	
	MOV.L #xx:32,ERd	3					
	MOV.L ERs,ERd	1					
	MOV.L @ERs,ERd	2				2	
	MOV.L @(d:16,ERs),ERd	3				2	
	MOV.L @(d:32,ERs),ERd	5				2	
	MOV.L @ERs+,ERd	2				2	1
	MOV.L @aa:16,ERd	3				2	
	MOV.L @aa:32,ERd	4				2	
	MOV.L ERs,@ERd	2				2	
	MOV.L ERs,@(d:16,ERd)	3				2	
	MOV.L ERs,@(d:32,ERd)	5				2	
	MOV.L ERs,@-ERd	2				2	1
	MOV.L ERs,@aa:16	3				2	
	MOV.L ERs,@aa:32	4				2	
MOVFPE	MOVFPE @:aa:16,Rd	Can not be used in the H8S/2357 Group					
MOVTPE	MOVTPE Rs,@:aa:16						
MULXS	MULXS.B Rs,Rd	2					11
	MULXS.W Rs,ERd	2					19
MULXU	MULXU.B Rs,Rd	1					11
	MULXU.W Rs,ERd	1					19
NEG	NEG.B Rd	1					
	NEG.W Rd	1					
	NEG.L ERd	1					
NOP	NOP	1					

Instruction		1	2	3	4	5	6	7	8	9
XOR.L ERs,ERd		R:W 2nd	R:W NEXT							
XORC #xx:8,CCR		R:W NEXT								
XORC #xx:8,EXR		R:W 2nd	R:W NEXT							
Reset exception handling	Advanced	R:W VEC	R:W VEC+2	Internal operation, 1 state	R:W*5					
Interrupt exception handling	Advanced	R:W*6	Internal operation, 1 state	W:W stack (L)	W:W stack (H)	W:W stack (EXR)	R:W:M VEC	R:W VEC+2	Internal operation, 1 state	R:W*7

Notes:
1. EAs is the contents of ER5. EAd is the contents of ER6.
2. EAs is the contents of ER5. EAd is the contents of ER6. Both registers are incremented by 1 after execution of the instruction. n is the initial value of R4L or R4. If n = 0, these bus cycles are not executed.
3. Repeated two times to save or restore two registers, three times for three registers, or four times for four registers.
4. Start address after return.
5. Start address of the program.
6. Prefetch address, equal to two plus the PC value pushed onto the stack. In recovery from sleep mode or software standby mode the read operation is replaced by an internal operation.
7. Start address of the interrupt-handling routine.
8. Only register ER0, ER1, ER4, or ER5 should be used when using the TAS instruction.

B.2 Functions

MRA—DTC Mode Register A **H'F800—H'FBFF** **DTC**

Bit :	7	6	5	4	3	2	1	0
	SM1	SM0	DM1	DM0	MD1	MD0	DTS	Sz
Initial value :	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write :	—	—	—	—	—	—	—	—

DTC Data Transfer Size

0	Byte-size transfer
1	Word-size transfer

DTC Transfer Mode Select

0	Destination side is repeat area or block area
1	Source side is repeat area or block area

DTC Mode

0	0	Normal mode
	1	Repeat mode
1	0	Block transfer mode
	1	—

Destination Address Mode

0	—	DAR is fixed
1	0	DAR is incremented after a transfer (by +1 when Sz = 0; by +2 when Sz = 1)
	1	DAR is decremented after a transfer (by -1 when Sz = 0; by -2 when Sz = 1)

Source Address Mode

0	—	SAR is fixed
1	0	SAR is incremented after a transfer (by +1 when Sz = 0; by +2 when Sz = 1)
	1	SAR is decremented after a transfer (by -1 when Sz = 0; by -2 when Sz = 1)

SYSCR2—System Control Register 2 **H'FF42** **MCU**

[F-ZTAT version Only]

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	FLSHE	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	—	—	—

Flash memory control register enable

0	Flash memory control register is not selected
1	Flash memory control register is selected

Note: SYSCR2 can only be accessed in the F-ZTAT version. In other versions, this register cannot be written to and will return an undefined value if read.

Reserved Register **H'FF44**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	—	—	—	—	—

Reserved
Only 0 should be written to these bits

Reserved Register **H'FF45**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reserved
Only 0 should be written to these bits

Reserved
Only 1 should be written to these bits

PMR—PPG Output Mode Register **H'FF47** **PPG**

Bit	7	6	5	4	3	2	1	0
	G3INV	G2INV	G1INV	G0INV	G3NOV	G2NOV	G1NOV	G0NOV
Initial value	1	1	1	1	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Pulse Output Group n Normal/Non-Overlap Operation Select

0	Normal operation in pulse output group n (output values updated at compare match A in the selected TPU channel)
1	Non-overlapping operation in pulse output group n (independent 1 and 0 output at compare match A or B in the selected TPU channel)

n=3 to 0

Pulse Output Group n Direct/Inverted Output

0	Inverted output for pulse output group n (low-level output at pin for a 1 in PODRH)
1	Direct output for pulse output group n (high-level output at pin for a 1 in PODRH)

n=3 to 0

EBR1—Erase Block Specification Register 1 **H'FFCA** **FLASH (For the H8S/2357 F-ZTAT)**

EBR2— Erase Block Specification Register 2 **H'FFCB** **FLASH (For the H8S/2357 F-ZTAT)**

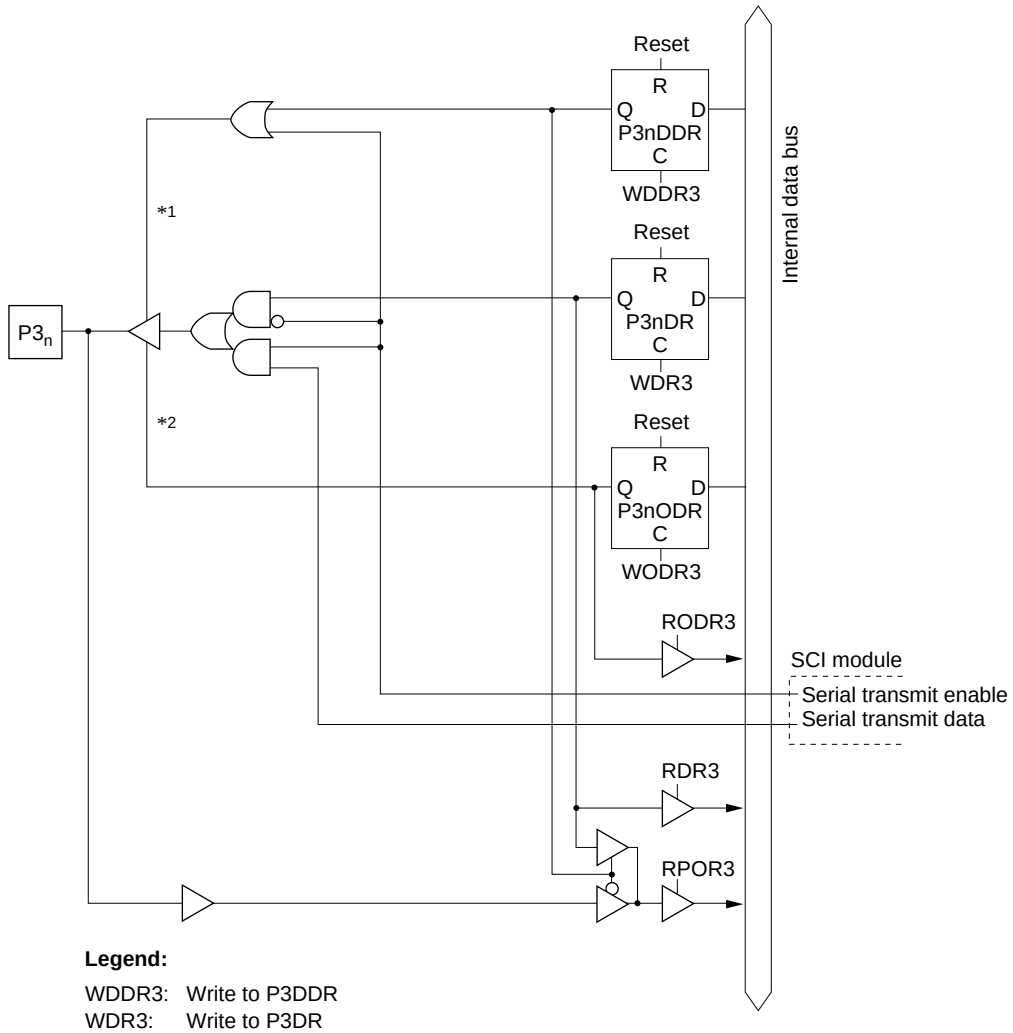
Bit	:	7	6	5	4	3	2	1	0
EBR1		—	—	—	—	—	—	EB9	EB8
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	—	—	—	—	—	—	R/W	R/W

Bit	:	7	6	5	4	3	2	1	0
EBR2		EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Deviding Erase Blocks

Block (size)	Address
EB0 (1 kbyte)	H'000000 to H'0003FF
EB1 (1 kbyte)	H'000400 to H'0007FF
EB2 (1 kbyte)	H'000800 to H'000BFF
EB3 (1 kbyte)	H'000C00 to H'000FFF
EB4 (28 kbytes)	H'001000 to H'007FFF
EB5 (16 kbytes)	H'008000 to H'00BFFF
EB6 (8 kbytes)	H'00C000 to H'00DFFF
EB7 (8 kbytes)	H'00E000 to H'00FFFF
EB8 (32 kbytes)	H'010000 to H'017FFF
EB9 (32 kbytes)	H'018000 to H'01FFFF

C.3 Port 3 Block Diagram



Legend:

WDDR3: Write to P3DDR
WDR3: Write to P3DR
WODR3: Write to P3ODR
RDR3: Read P3DR
RPOR3: Read port 3
RODR3: Read P3ODR
n = 0 or 1

Notes: 1. Output enable signal
2. Open drain control signal

Figure C-3 (a) Port 3 Block Diagram (Pins $P3_0$ and $P3_1$)