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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	87
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12392f20v

User's manuals for development tools:

Manual Title	Document No.
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimized Linkage Editor User's Manual	REJ10B0058
H8S, H8/300 Series Simulator/Debugger (for Windows) User's Manual	ADE-702-037
H8S, H8/300 Series High-performance Embedded Workshop User's Manual	ADE-702-201

Application Note:

Manual Title	Document No.
H8S Family Technical Q & A	REJ05B0397

Table 4-2 Exception Vector Table

Exception Source		Vector Number	Vector Address*[1] Advanced Mode
Power-on reset		0	H'0000 to H'0003
Manual reset*[3]		1	H'0004 to H'0007
Reserved for system use		2	H'0008 to H'000B
		3	H'000C to H'000F
		4	H'0010 to H'0013
Trace		5	H'0014 to H'0017
Reserved for system use		6	H'0018 to H'001B
External interrupt	NMI	7	H'001C to H'001F
Trap instruction (4 sources)		8	H'0020 to H'0023
		9	H'0024 to H'0027
		10	H'0028 to H'002B
		11	H'002C to H'002F
Reserved for system use		12	H'0030 to H'0033
		13	H'0034 to H'0037
		14	H'0038 to H'003B
		15	H'003C to H'003F
External interrupt	IRQ0	16	H'0040 to H'0043
	IRQ1	17	H'0044 to H'0047
	IRQ2	18	H'0048 to H'004B
	IRQ3	19	H'004C to H'004F
	IRQ4	20	H'0050 to H'0053
	IRQ5	21	H'0054 to H'0057
	IRQ6	22	H'0058 to H'005B
	IRQ7	23	H'005C to H'005F
Internal interrupt*[2]		24 ⎮ 91	H'0060 to H'0063 ⎮ H'016C to H'016F

Notes: 1. Lower 16 bits of the address.
2. For details of internal interrupt vectors, see section 5.3.3, Interrupt Exception Handling Vector Table.
3. Manual reset is only supported in the H8S/2357 ZTAT.

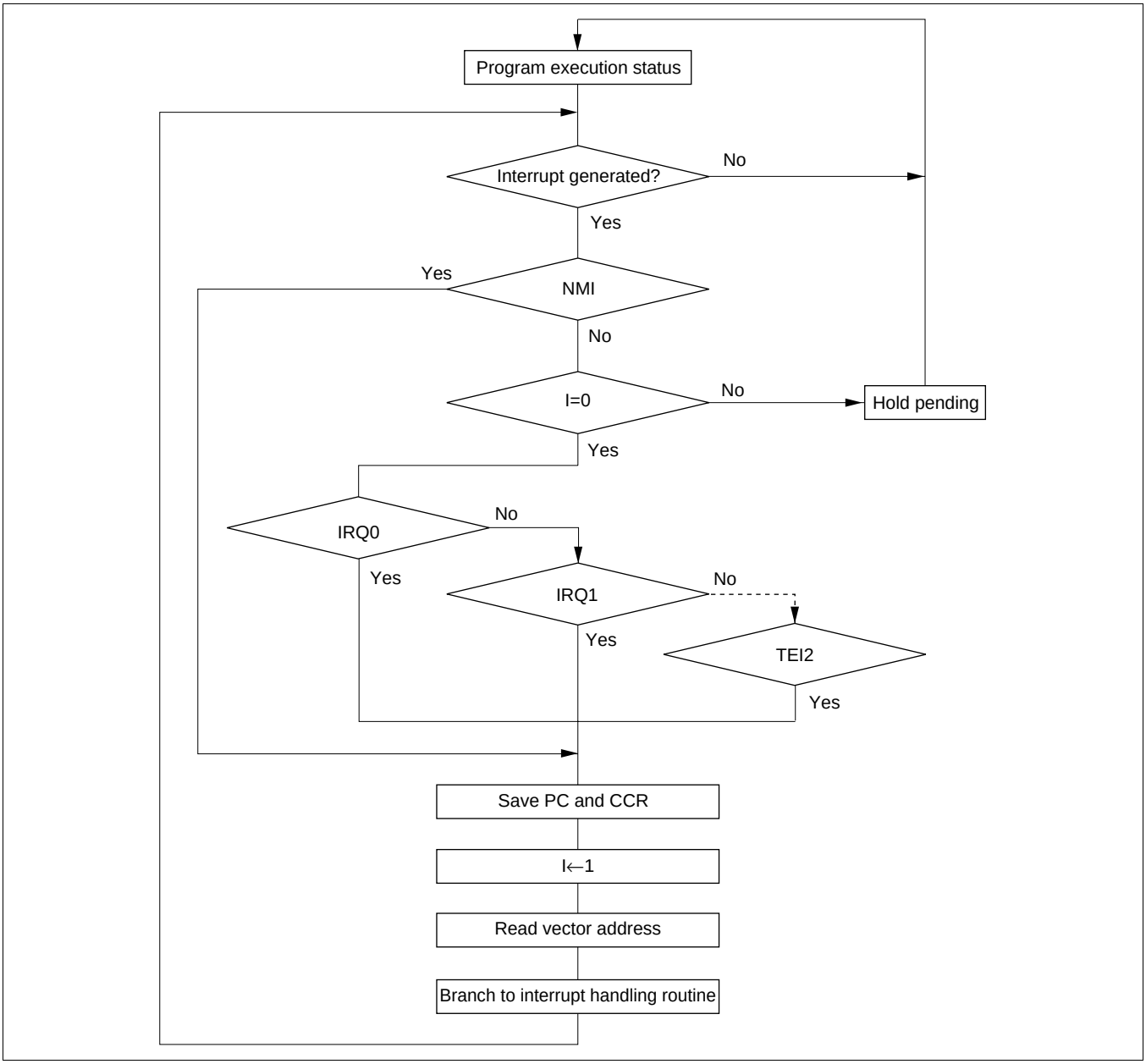

Figure 5-5 Flowchart of Procedure Up to Interrupt Acceptance in Interrupt Control Mode 0

5.5.3 Times when Interrupts are Disabled

There are times when interrupt acceptance is disabled by the interrupt controller.

The interrupt controller disables interrupt acceptance for a 3-state period after the CPU has updated the mask level with an LDC, ANDC, ORC, or XORC instruction.

5.5.4 Interrupts during Execution of EEPMOV Instruction

Interrupt operation differs between the EEPMOV.B instruction and the EEPMOV.W instruction.

With the EEPMOV.B instruction, an interrupt request (including NMI) issued during the transfer is not accepted until the move is completed.

With the EEPMOV.W instruction, if an interrupt request is issued during the transfer, interrupt exception handling starts at a break in the transfer cycle. The PC value saved on the stack in this case is the address of the next instruction.

Therefore, if an interrupt is generated during execution of an EEPMOV.W instruction, the following coding should be used.

```
L1:   EEPMOV.W
      MOV.W     R4,R4
      BNE       L1
```

5.6 DTC and DMAC Activation by Interrupt

5.6.1 Overview

The DTC and DMAC can be activated by an interrupt. In this case, the following options are available:

- Interrupt request to CPU
- Activation request to DTC
- Activation request to DMAC
- Selection of a number of the above

For details of interrupt requests that can be used with to activate the DTC or DMAC, see section 8, Data Transfer Controller, and section 7, DMA Controller.

6.4.4 Basic Timing

8-Bit 2-State Access Space: Figure 6-6 shows the bus timing for an 8-bit 2-state access space. When an 8-bit access space is accessed, the upper half (D_{15} to D_8) of the data bus is used.

The $\overline{\text{LWR}}$ pin is fixed high. Wait states cannot be inserted.

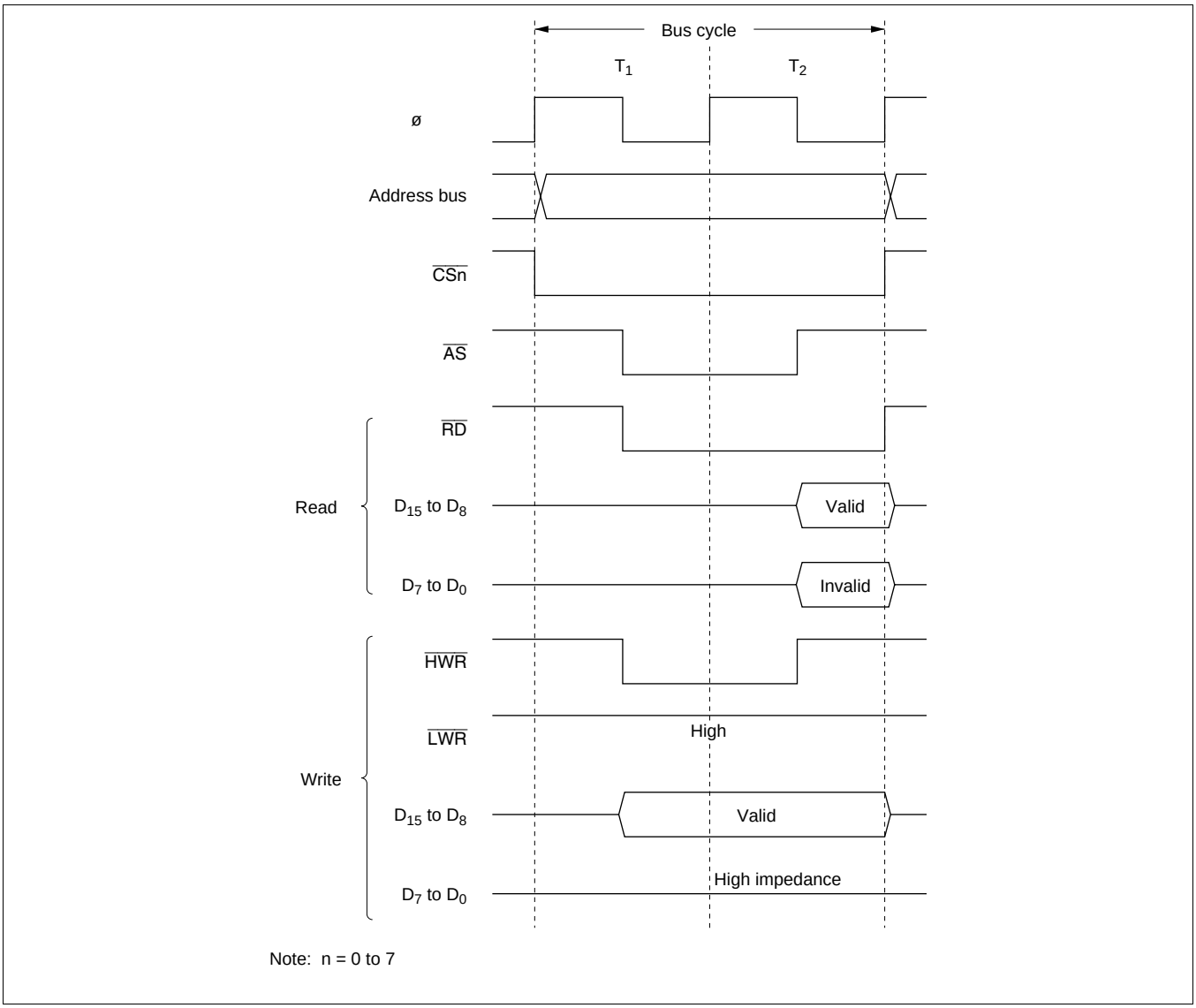

Figure 6-6 Bus Timing for 8-Bit 2-State Access Space

Figure 6-17 shows an example of wait state insertion timing.

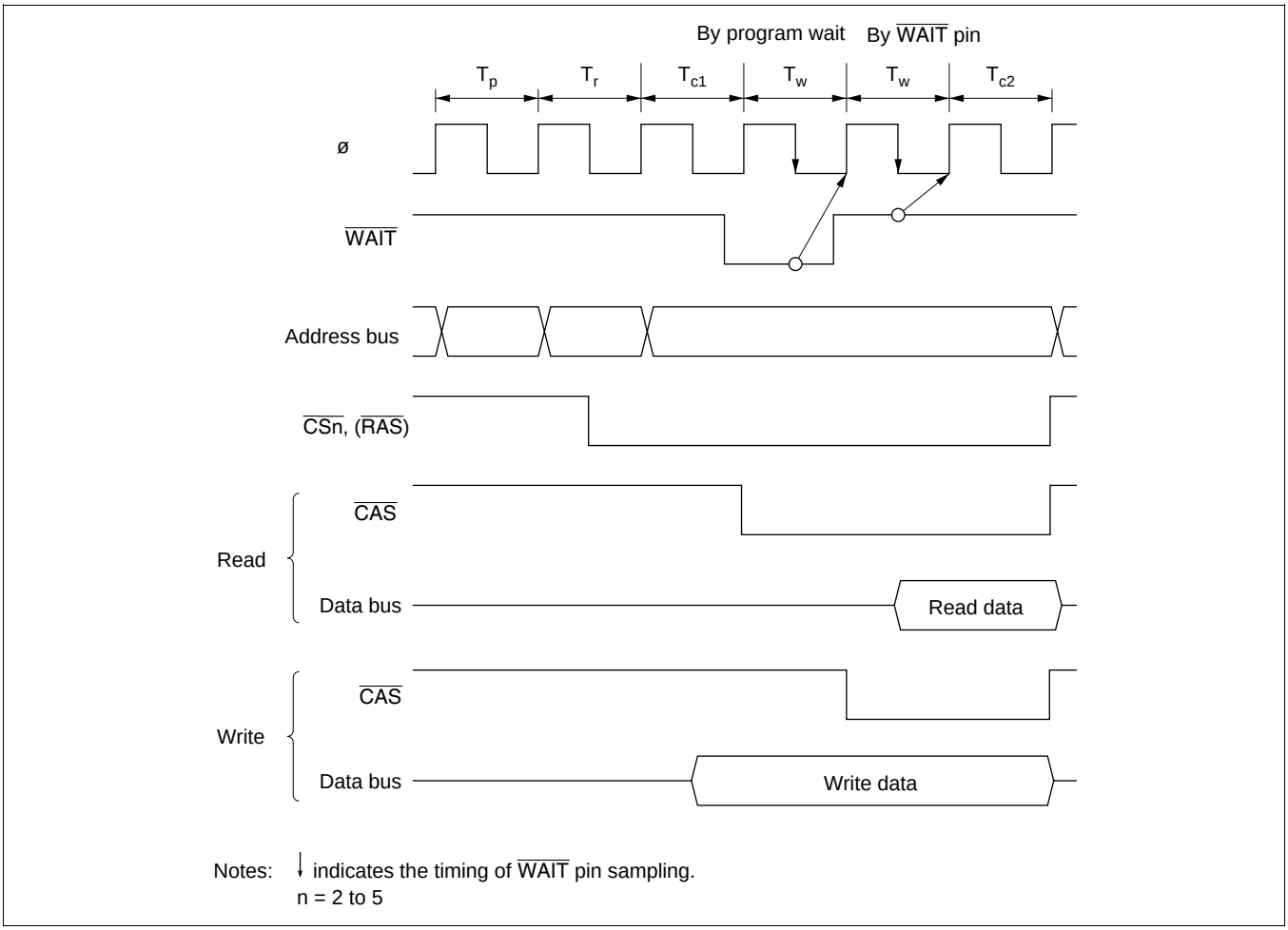

Figure 6-17 Example of Wait State Insertion Timing (CW2 = 1, 8-Bit Area Setting for Entire Space)

Bits 3 and 1—Data Transfer Interrupt Enable B (DTIEB): These bits enable or disable an interrupt to the CPU or DTC when transfer is interrupted. If the DTIEB bit is set to 1 when DTME = 0, the DMAC regards this as indicating a break in the transfer, and issues a transfer break interrupt request to the CPU or DTC.

A transfer break interrupt can be canceled either by clearing the DTIEB bit to 0 in the interrupt handling routine, or by performing processing to continue transfer by setting the DTME bit to 1.

Bit 3—Data Transfer Interrupt Enable 1B (DTIE1B): Enables or disables the channel 1 transfer break interrupt.

Bit 3 DTIE1B	Description	
0	Transfer break interrupt disabled	(Initial value)
1	Transfer break interrupt enabled	

Bit 1—Data Transfer Interrupt Enable 0B (DTIE0B): Enables or disables the channel 0 transfer break interrupt.

Bit 1 DTIE0B	Description	
0	Transfer break interrupt disabled	(Initial value)
1	Transfer break interrupt enabled	

Bits 2 and 0—Data Transfer End Interrupt Enable A (DTIEA): These bits enable or disable an interrupt to the CPU or DTC when transfer ends. If DTIEA bit is set to 1 when DTE = 0, the DMAC regards this as indicating the end of a transfer, and issues a transfer end interrupt request to the CPU or DTC.

A transfer end interrupt can be canceled either by clearing the DTIEA bit to 0 in the interrupt handling routine, or by performing processing to continue transfer by setting the transfer counter and address register again, and then setting the DTE bit to 1.

Bit 2—Data Transfer Interrupt Enable 1A (DTIE1A): Enables or disables the channel 1 transfer end interrupt.

Bit 2 DTIE1A	Description	
0	Transfer end interrupt disabled	(Initial value)
1	Transfer end interrupt enabled	

Bit 0—Data Transfer Interrupt Enable 0A (DTIE0A): Enables or disables the channel 0 transfer end interrupt.

Bit 0 DTIE0A	Description	
0	Transfer end interrupt disabled	(Initial value)
1	Transfer end interrupt enabled	

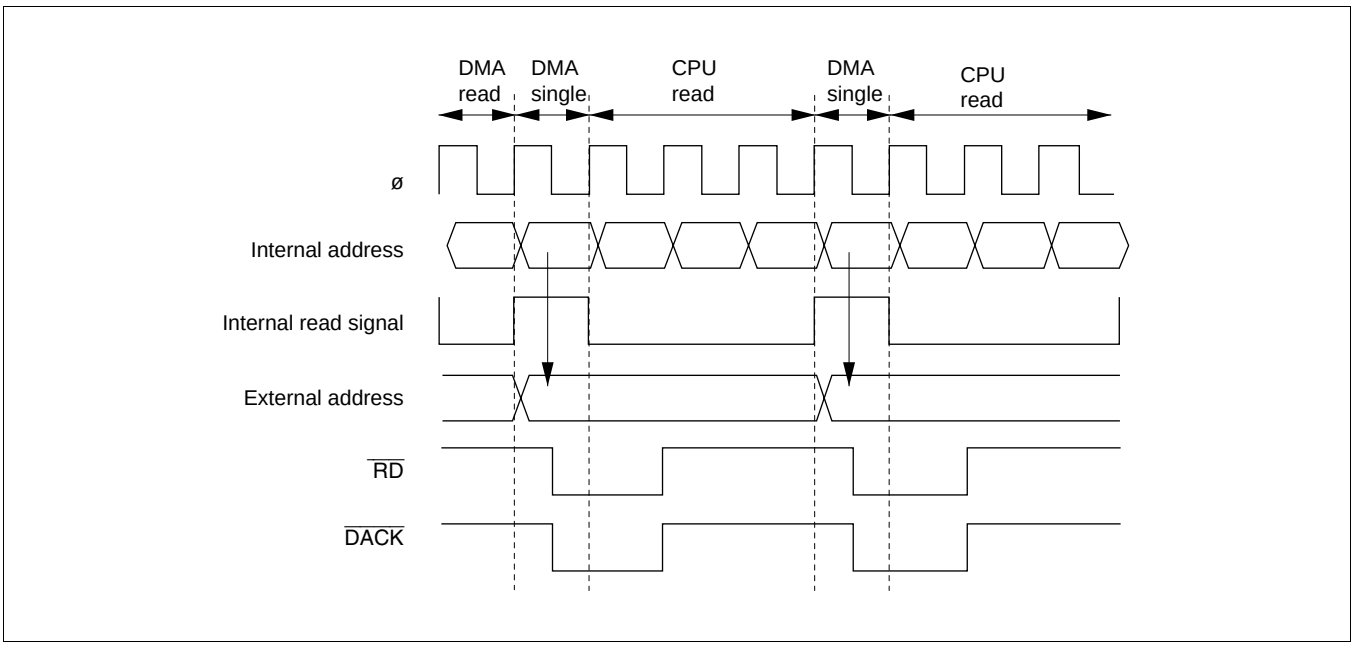

Figure 7-34 Example of Single Address Transfer Using Write Data Buffer Function

When the write data buffer function is activated, the DMAC recognizes that the bus cycle concerned has ended, and starts the next operation. Therefore, $\overline{\text{DREQ}}$ pin sampling is started one state after the start of the DMA write cycle or single address transfer.

7.5.13 DMAC Multi-Channel Operation

The DMAC channel priority order is: channel 0 > channel 1, and channel A > channel B. Table 7-13 summarizes the priority order for DMAC channels.

Table 7-13 DMAC Channel Priority Order

Short Address Mode	Full Address Mode	Priority
Channel 0A	Channel 0	High
Channel 0B		↑
Channel 1A	Channel 1	
Channel 1B		Low

Pin	Selection Method and Pin Functions
$P2_6$/PO6/TIOCA5/ TMO0	The pin function is switched as shown below according to the combination of the TPU channel 5 setting by bits MD3 to MD0 in TMDR5, bits IOA3 to IOA0 in TIOR5, bits CCLR1 and CCLR0 in TCR5, bit NDER6 in NDERL, bits OS3 to OS0 in TCSR0, and bit P26DDR.

OS3 to OS0	All 0				Any 1
TPU Channel 5 Setting	Table Below (1)	Table Below (2)			—
P26DDR	—	0	1	1	—
NDER6	—	—	0	1	—
Pin function	TIOCA5 output	$P2_6$ input	$P2_6$ output	PO6 output	TMO0 output
		TIOCA5 input *1			

Note: 1. TIOCA5 input when MD3 to MD0 = B'0000, B'01××, and IOA3 = 1.

TPU Channel 5 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01××		B'001×	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1×××	B'0001 to B'0011 B'0101 to B'0111	B'××00	Other than B'××00		
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

×: Don't care

Note: 2. TIOCB5 output is disabled.

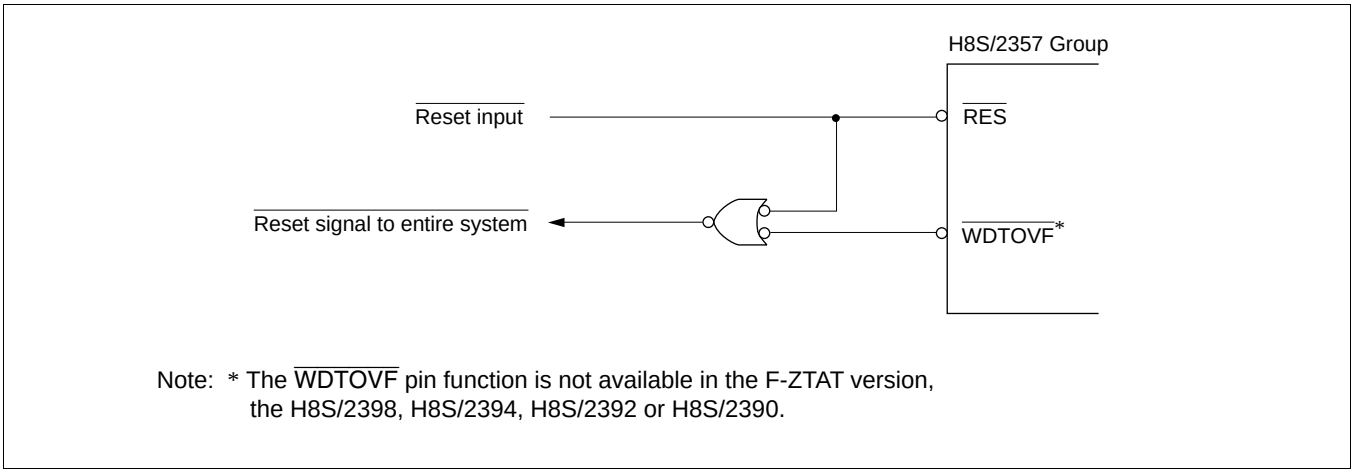

Figure 13-9 Circuit for System Reset by WDTOVF Signal (Example)

13.5.5 Internal Reset in Watchdog Timer Mode

The H8S/2357 Group is not reset internally if TCNT overflows while the RSTE bit is cleared to 0 during watchdog timer operation, but TCNT and TSCR of the WDT are reset.

TCNT, TCSR, and RSTCR cannot be written to while the WDTOVF signal* is low. Also note that a read of the WOVF flag is not recognized during this period. To clear the WOVF falg, therefore, read RSTCSR after the WDTOVF signal* goes high, then write 0 to the WOVF flag.

Note: * The WDTOVF pin function is not available in the F-ZTAT version, the H8S/2398, H8S/2394, H8S/2392 or H8S/2390.

19.11 Flash Memory Emulation in RAM

19.11.1 Emulation in RAM

Making a setting in the RAM emulation register (RAMER) enables part of RAM to be overlapped onto the flash memory area so that data to be written to flash memory can be emulated in RAM in real time. After the RAMER setting has been made, accesses can be made from the flash memory area or the RAM area overlapping flash memory. Emulation can be performed in user mode and user program mode. Figure 19-22 shows an example of emulation of real-time flash memory programming.

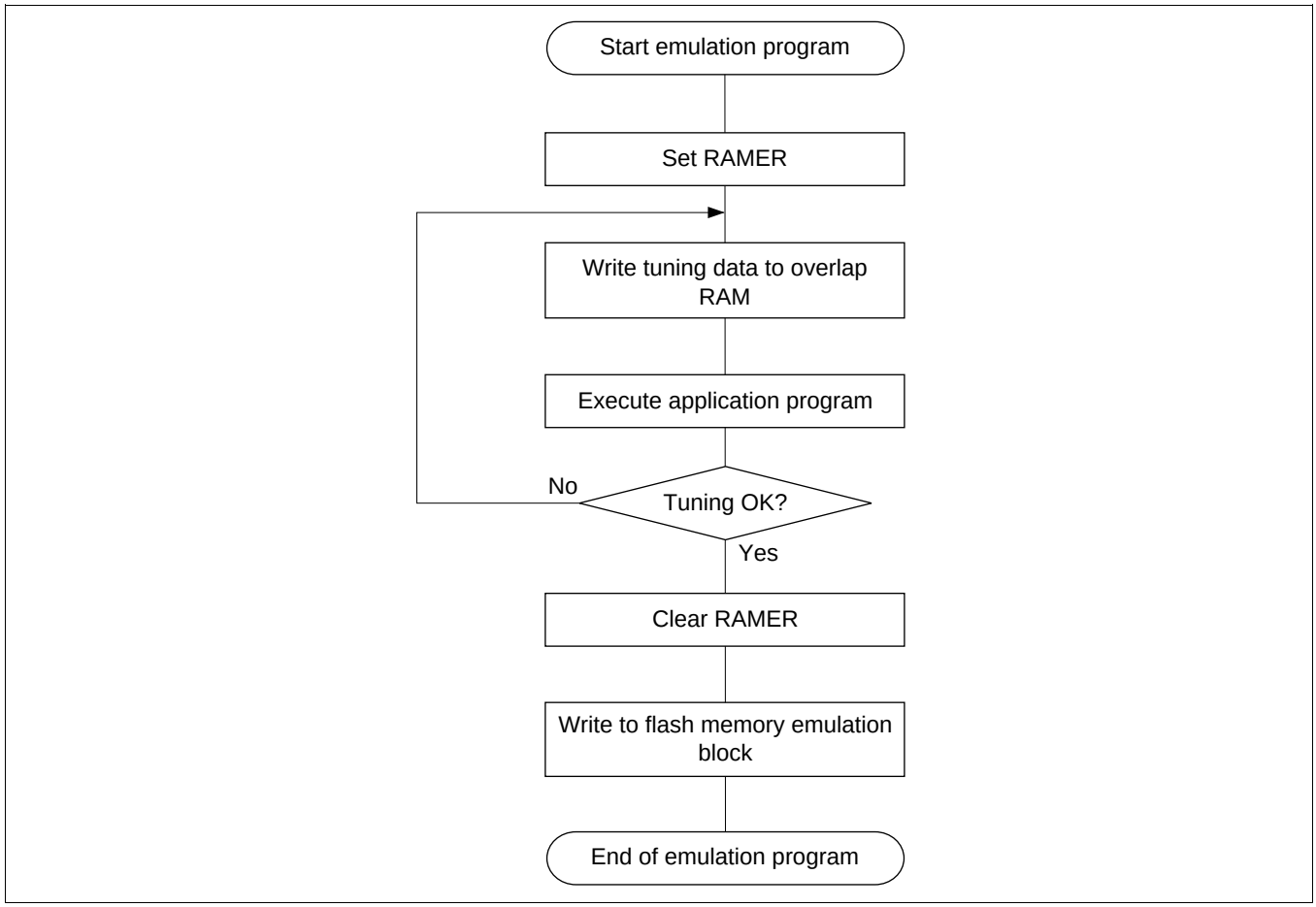

Figure 19-22 Flowchart for Flash Memory Emulation in RAM

19.16 Register Descriptions

19.16.1 Flash Memory Control Register 1 (FLMCR1)

Bit	:	7	6	5	4	3	2	1	0
		FWE	SWE	ESU	PSU	EV	PV	E	P
Initial value	:	1	0	0	0	0	0	0	0
R/W	:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FLMCR1 is an 8-bit register used for flash memory operating mode control. Program-verify mode or erase-verify mode is entered by setting SWE to 1, then setting the EV or PV bit. Program mode is entered by setting SWE to 1, then setting the PSU bit, and finally setting the P bit. Erase mode is entered by setting SWE to 1, then setting the ESU bit, and finally setting the E bit. FLMCR1 is initialized to H'80 by a reset, and in hardware standby mode and software standby mode. When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

Writing to bits ESU, PSU, EV, and PV in FLMCR1 is enabled only when SWE = 1; writing to the E bit is enabled only when SWE = 1, and ESU = 1; and writing to the P bit is enabled only when SWE = 1, and PSU = 1.

Bit 7—Flash Write Enable Bit (FWE): Sets hardware protection against flash memory programming/erasing. These bits cannot be modified and are always read as 1 in this model.

Bit 6—Software Write Enable Bit (SWE): Enables or disables flash memory programming and erasing. This bit should be set when setting bits 5 to 0, EBR1 bits 7 to 0, and EBR2 bits 3 to 0.

When SWE = 1, the flash memory can only be read in program-verify or erase-verify mode.

Bit 6 SWE	Description	
0	Writes disabled	(Initial value)
1	Writes enabled	

Bit 5—Erase Setup Bit (ESU): Prepares for a transition to erase mode. Do not set the SWE, PSU, EV, PV, E, or P bit at the same time.

Bit 5 ESU	Description	
0	Erase setup cleared	(Initial value)
1	Erase setup [Setting condition] When SWE = 1	

Bit 4—Program Setup Bit (PSU): Prepares for a transition to program mode. Do not set the SWE, ESU, EV, PV, E, or P bit at the same time.

Bit 4 PSU	Description	
0	Program setup cleared	(Initial value)
1	Program setup [Setting condition] When SWE = 1	

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current dissipation*2	Normal operation	I_{CC}*4	—	46 (5.0 V)	69	mA	f = 20 MHz
	Sleep mode		—	37 (5.0 V)	56	mA	f = 20 MHz
	Standby mode*3		—	0.01	10	µA	$T_a \leq 50°C$
			—	—	80		$50°C < T_a$
Analog power supply current	During A/D and D/A conversion	AI_{CC}	—	0.8 (5.0 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference current	During A/D and D/A conversion	AI_{CC}	—	2.2 (5.0 V)	3.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{ref} to V_{CC} pin, and connect AV_{SS} to V_{SS} pin.

2. Current dissipation values are for V_{IH} min = V_{CC} -0.2 V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up MOS in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 4.5$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:
   I_{CC} max = 3.0 (mA) + 0.60 (mA/(MHz × V)) × V_{CC} × f [normal mode]
   I_{CC} max = 3.0 (mA) + 0.48 (mA/(MHz × V)) × V_{CC} × f [sleep mode]

Table 22-3 Permissible Output Currents

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 1, A to C	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 32 pins including ports 1 and A to C	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 22-3.

2. When driving a darlington pair or LED directly, always insert a current-limiting resistor in the output line, as show in figures 22-1 and 22-2.

Item	Symbol	Condition			Test Conditions
		Min	Max	Unit	
$\overline{WR}$ hold time	t_{WCH}	0.5 × t_{cyc} – 10	—	ns	Figure 22-8 to Figure 22-15
$\overline{CAS}$ setup time	t_{CSR}	0.5 × t_{cyc} – 10	—	ns	Figure 22-12
$\overline{WAIT}$ setup time	t_{WTS}	30	—	ns	Figure 22-10
$\overline{WAIT}$ hold time	t_{WTH}	5	—	ns	
$\overline{BREQ}$ setup time	t_{BRQS}	30	—	ns	Figure 22-16
$\overline{BACK}$ delay time	t_{BACD}	—	15	ns	
Bus-floating time	t_{BZD}	—	50	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	30	ns	Figure 22-17

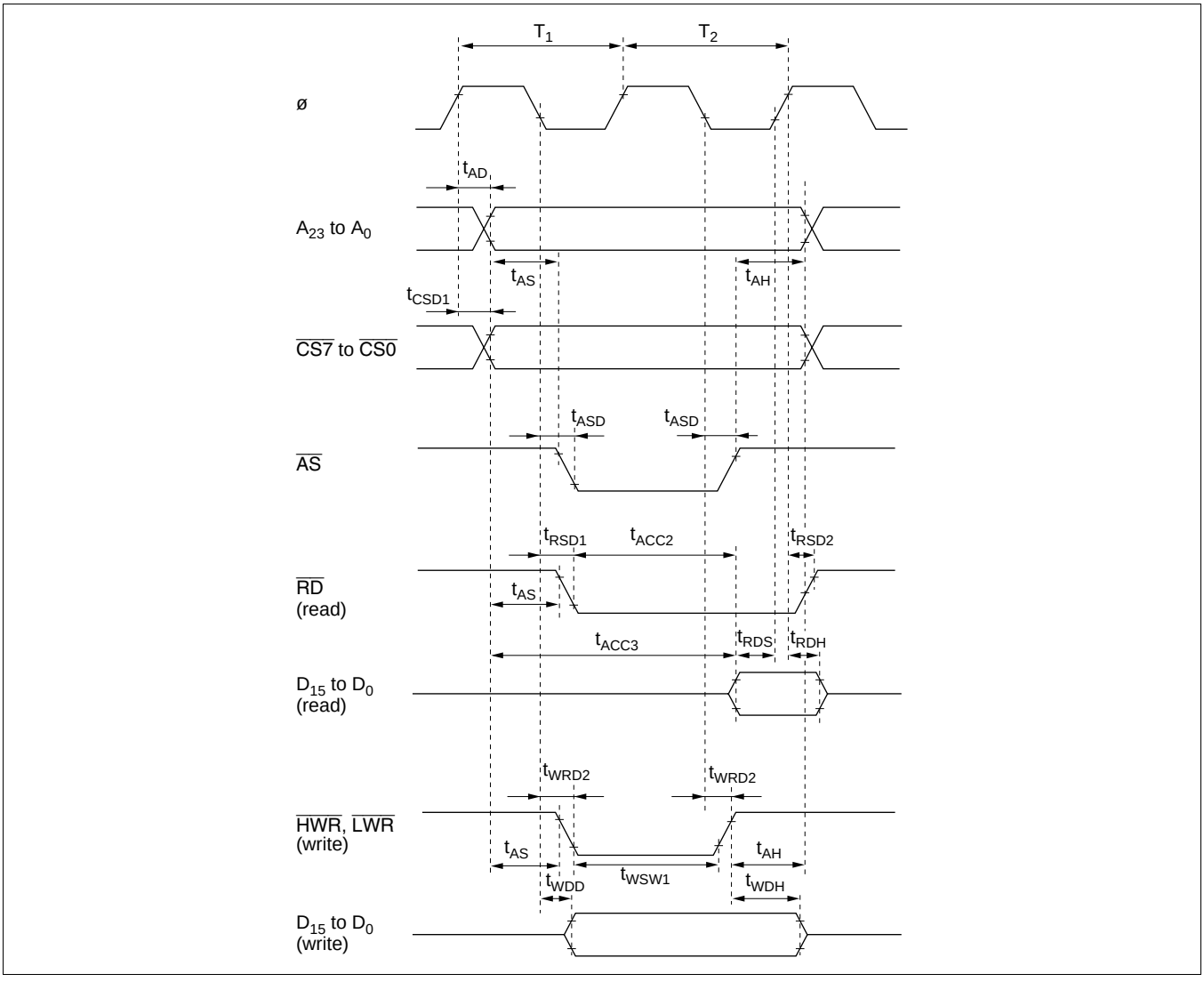

Figure 22-8 Basic Bus Timing (Two-State Access)

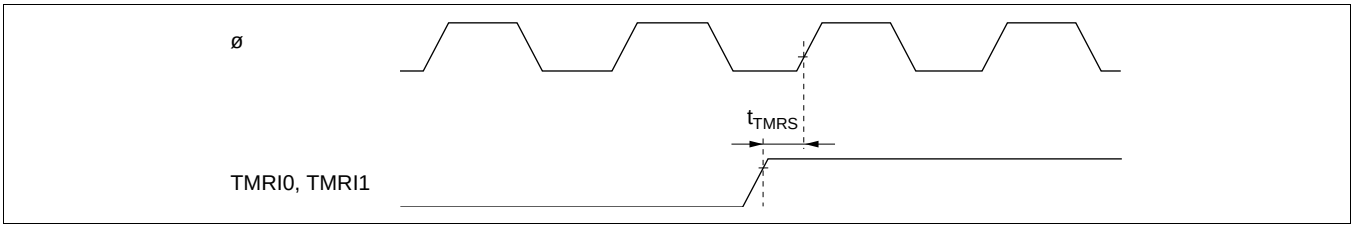

Figure 22-92 8-Bit Timer Reset Input Timing

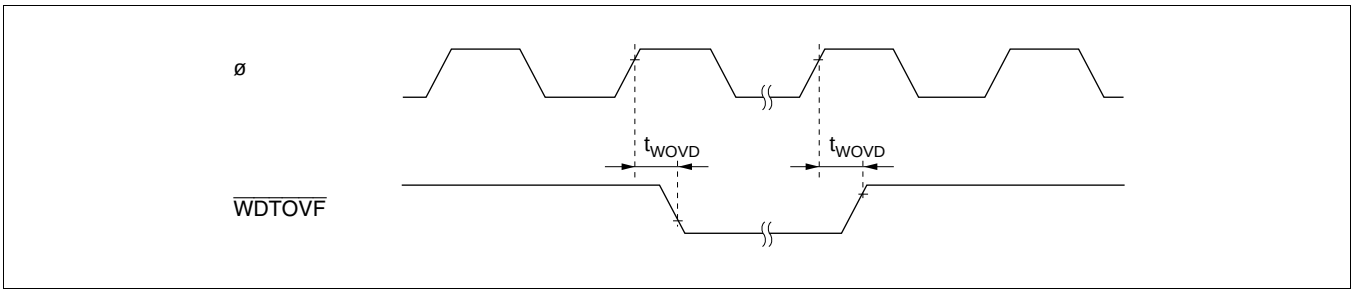

Figure 22-93 WDT Output Timing

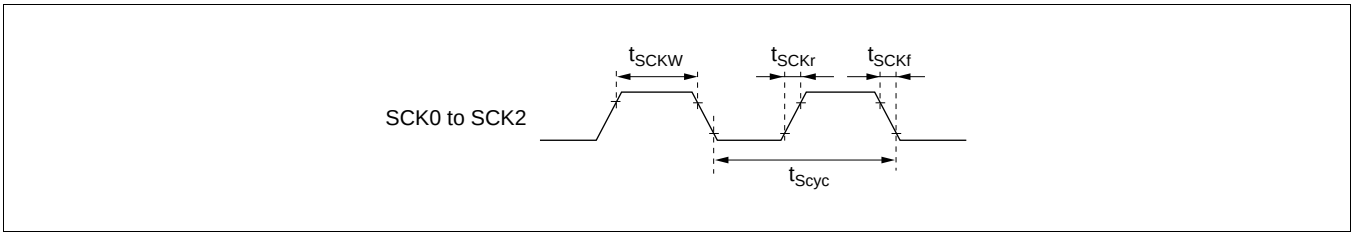

Figure 22-94 SCK Clock Input Timing

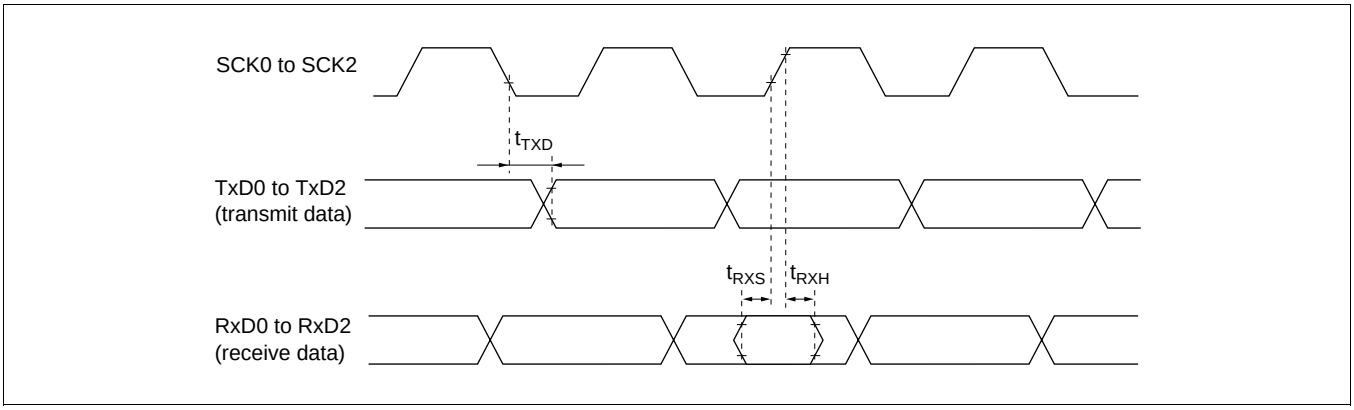

Figure 22-95 SCI Input/Output Timing (Clock Synchronous Mode)

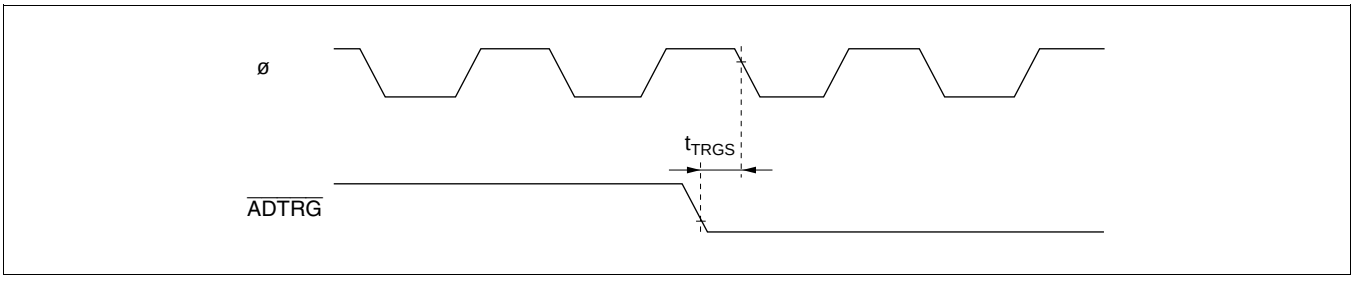

Figure 22-96 A/D Converter External Trigger Input Timing

Instruction	1	2	3	4	5	6	7	8	9
BLE d:8	R:W NEXT	R:W EA							
BRA d:16 (BT d:16)	R:W 2nd	Internal operation, 1 state	R:W EA						
BRN d:16 (BF d:16)	R:W 2nd	Internal operation, 1 state	R:W EA						
BHI d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BLS d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BCC d:16 (BHS d:16)	R:W 2nd	Internal operation, 1 state	R:W EA						
BCS d:16 (BLO d:16)	R:W 2nd	Internal operation, 1 state	R:W EA						
BNE d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BEQ d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BVC d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BVS d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BPL d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BMI d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BGE d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BLT d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BGT d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BLE d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BCLR #xx:3,Rd	R:W NEXT								
BCLR #xx:3,@ERd	R:W 2nd	R:B:M EA	R:W:M NEXT	W:B EA					
BCLR #xx:3,@aa:8	R:W 2nd	R:B:M EA	R:W:M NEXT	W:B EA					
BCLR #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B:M EA	R:W:M NEXT	W:B EA				

FLMCR1—Flash Memory Control Register 1 H'FFC8 FLASH
(For the H8S/2357 F-ZTAT)

Bit :	7	6	5	4	3	2	1	0
	FWE	SWE	—	—	EV	PV	E	P
Initial value :	—*	0	0	0	0	0	0	0
Read/Write :	R	R/W	—	—	R/W	R/W	R/W	R/W

Program

0	Clears program mode
1	Program mode is entered [Setting condition] FWE=1, SWE=1, and PSU=1

Erase

0	Clears erase mode
1	Erase mode is entered [Setting condition] FWE=1, SWE=1, and ESU=1

Program Verify

0	Clears program verify mode
1	Program verify mode is entered [Setting condition] FWE=1 and SWE=1

Erase Verify

0	Clears erase verify mode
1	Erase verify mode is entered [Setting condition] FWE=1 and SWE=1

Software Write Enable

0	Writing disabled
1	Writing enabled [Setting condition] FWE=1

Flash Write Enable

0	When a low level is input to the FWE pin (hardware protect state)
1	When a high level is input to the FWE pin

Note: * Determined by the state of the FWE pin.

TMDR0—Timer Mode Register 0 **H'FFD1** **TPU0**

Bit	7	6	5	4	3	2	1	0
	—	—	BFB	BFA	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	×	×	×	—

×: Don't care

Notes: 1. MD3 is a reserved bit. In a write, it should always be written with 0.
2. Phase counting mode cannot be set for channels 0 and 3. In this case, 0 should always be written to MD2.

TGRA Buffer Operation

0	TGRA operates normally
1	TGRA and TGRC used together for buffer operation

TGRB Buffer Operation

0	TGRB operates normally
1	TGRB and TGRD used together for buffer operation

TIOR2—Timer I/O Control Register 2 H'FFF2 TPU2

Bit	:	7	6	5	4	3	2	1	0
		IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR2A I/O Control

0	0	0	0	TGR2A is output compare register	Output disabled
			1		Initial output is 0 output: 0 output at compare match
		1	0		1 output at compare match
			1		Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output: 0 output at compare match
		1	0		1 output at compare match
			1		Toggle output at compare match
1	×	0	0	TGR2A is input capture register	Capture input source is TIOCA2 pin: Input capture at rising edge
			1		Input capture at falling edge
		1	×		Input capture at both edges

×: Don't care

TGR2B I/O Control

0	0	0	0	TGR2B is output compare register	Output disabled
			1		Initial output is 0 output: 0 output at compare match
		1	0		1 output at compare match
			1		Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output: 0 output at compare match
		1	0		1 output at compare match
			1		Toggle output at compare match
1	×	0	0	TGR2B is input capture register	Capture input source is TIOCB2 pin: Input capture at rising edge
			1		Input capture at falling edge
		1	×		Input capture at both edges

×: Don't care

C.11 Port E Block Diagram

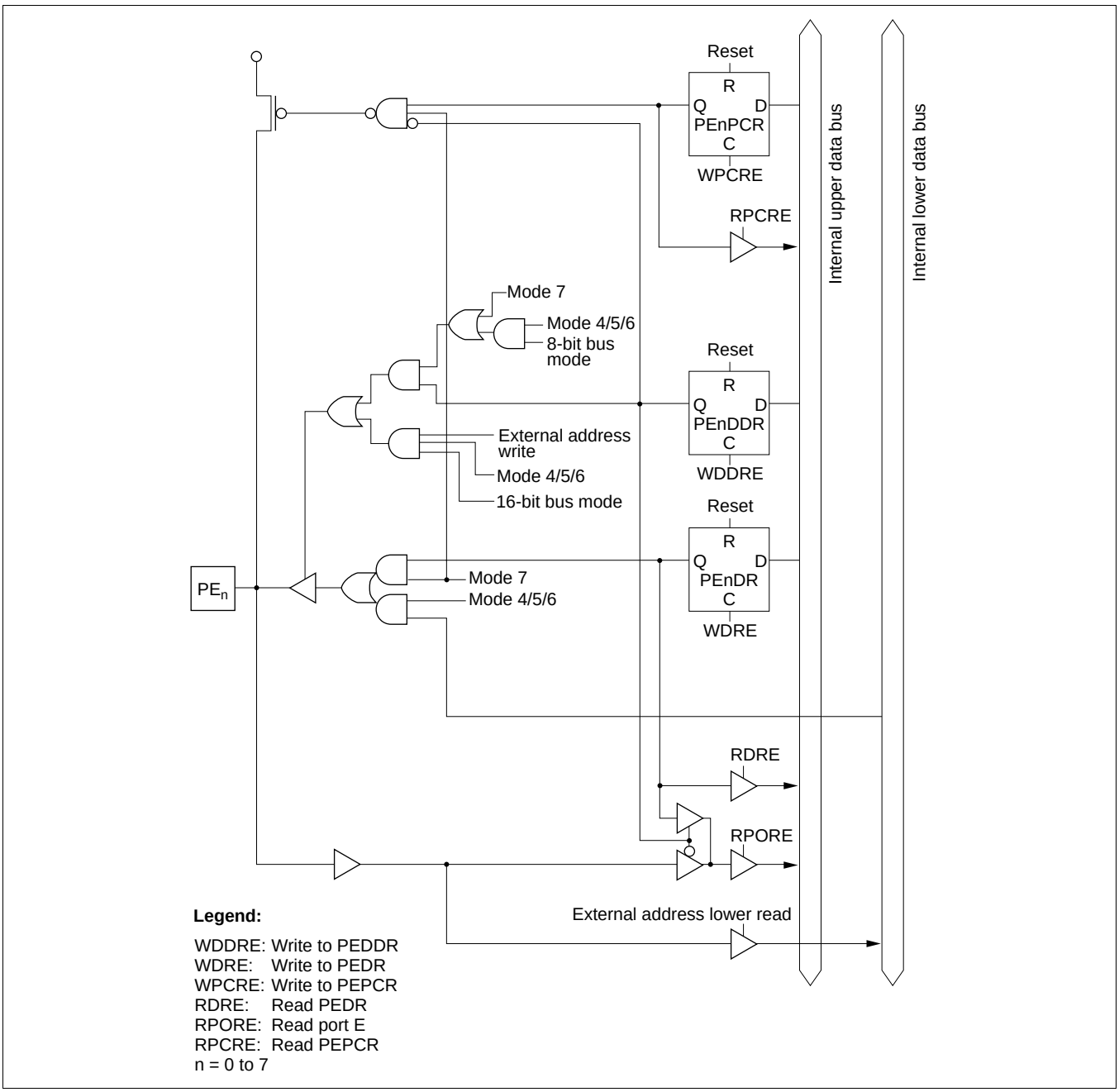

Figure C-11 Port E Block Diagram (Pin PE_0 to PE_7)