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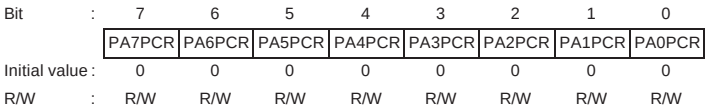
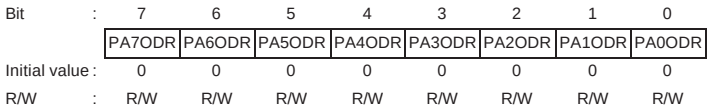
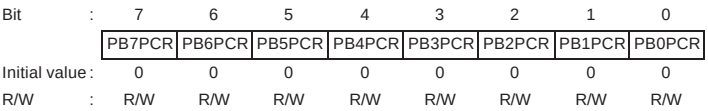
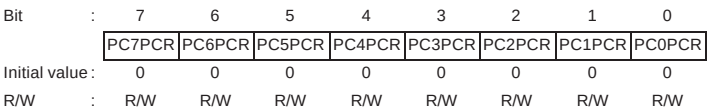
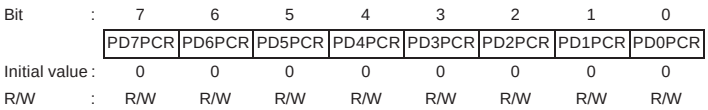
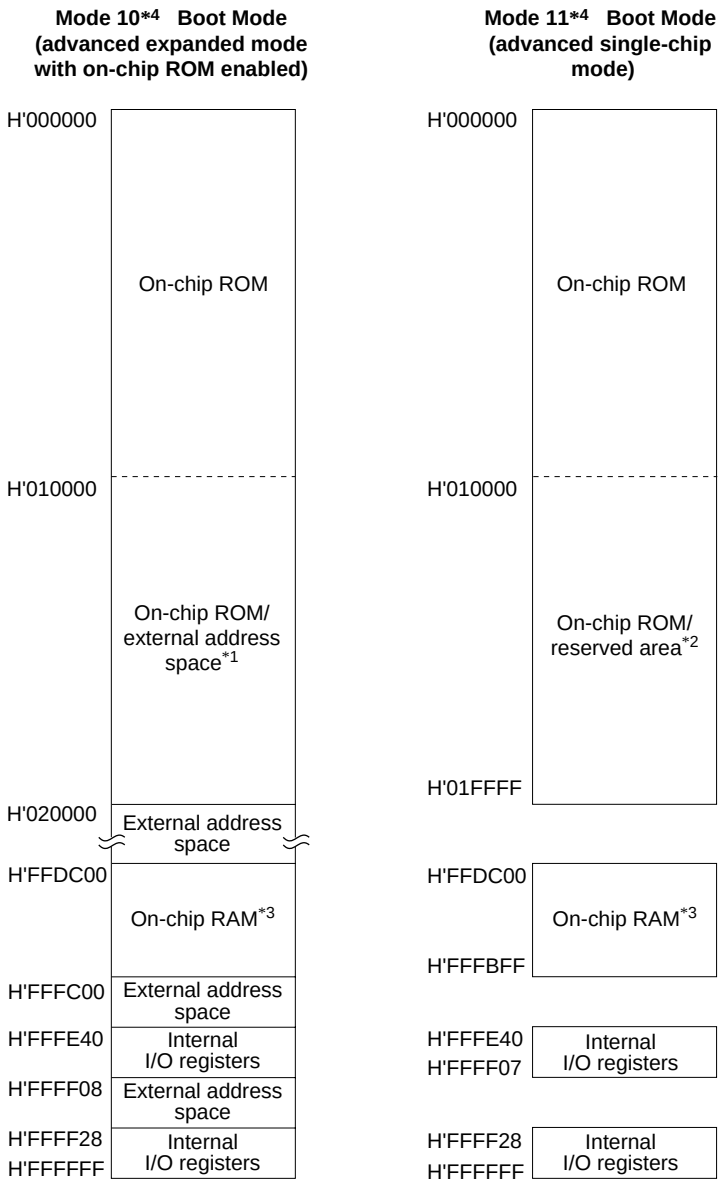
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	87
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12392te20v

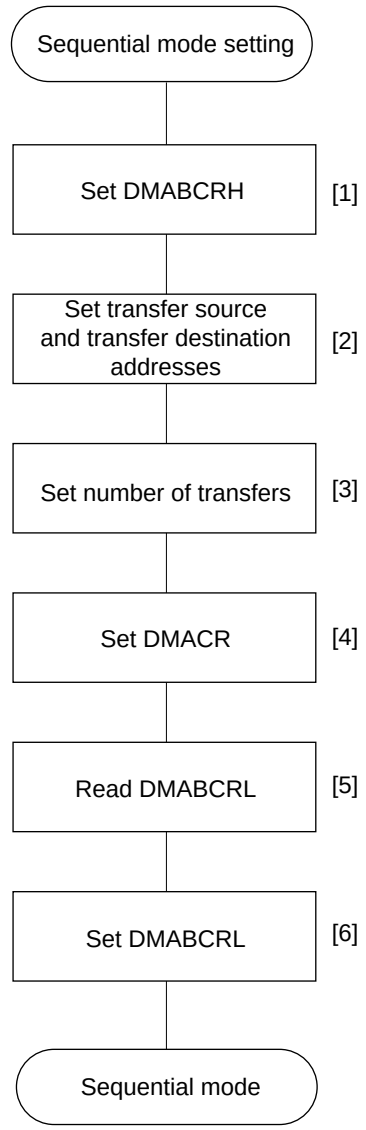
Item	Page	Revision (See Manual for Details)
9.8.2 Register Configuration	303	Note added Port A MOS Pull-Up Control Register (PAPCR) (ON-Chip ROM Version Only)  Note: Setting is prohibited in the H8S/2352, H8S/2394, H8S/2392, and H8S/2390.
	304	Port A Open Drain Control Register (PAODR) (ON-Chip ROM Version Only)  Note: Setting is prohibited in the H8S/2352, H8S/2394, H8S/2392, and H8S/2390.
9.9.2 Register Configuration (On-Chip ROM Version Only)	309	Note added Port B MOS Pull-Up Control Register (PBPCR) (ON-Chip ROM Version Only)  Note: Setting is prohibited in the H8S/2352, H8S/2394, H8S/2392, and H8S/2390.
9.10.2 Register Configuration (On-Chip ROM Version Only)	314	Note added Port C MOS Pull-Up Control Register (PCPCR) (ON-Chip ROM Version Only)  Note: Setting is prohibited in the H8S/2352, H8S/2394, H8S/2392, and H8S/2390.
9.11.2 Register Configuration (On-Chip ROM Version Only)	319	Note added Port D MOS Pull-Up Control Register (PDPCR) (ON-Chip ROM Version Only)  Note: Setting is prohibited in the H8S/2352, H8S/2394, H8S/2392, and H8S/2390.



Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. On-chip RAM is used for flash memory programming. Do not clear the RAME bit to 0 in SYSCR.
4. Modes 10 and 11 are provided in the F-ZTAT version only.

Figure 3-1 Memory Map in Each Operating Mode (H8S/2357, H8S/2352) (2)

Figure 7-4 shows an example of the setting procedure for sequential mode.



[1] Set each bit in DMABCRH.
- Clear the FAE bit to 0 to select short address mode.
- Specify enabling or disabling of internal interrupt clearing with the DTA bit.

[2] Set the transfer source address and transfer destination address in MAR and IOAR.

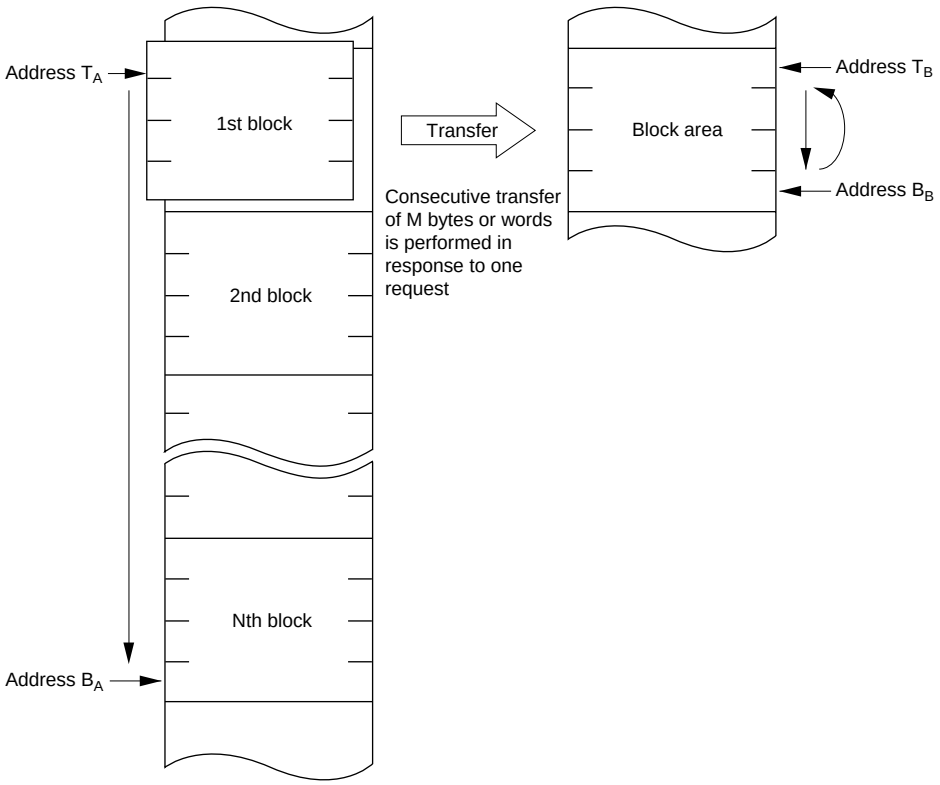
[3] Set the number of transfers in ETCR.

[4] Set each bit in DMACR.
- Set the transfer data size with the DTSZ bit.
- Specify whether MAR is to be incremented or decremented with the DTID bit.
- Clear the RPE bit to 0 to select sequential mode.
- Specify the transfer direction with the DTDIR bit.
- Select the activation source with bits DTF3 to DTF0.

[5] Read the DTE bit in DMABCRL as 0.

[6] Set each bit in DMABCRL.
- Specify enabling or disabling of transfer end interrupts with the DTIE bit.
- Set the DTE bit to 1 to enable transfer.

Figure 7-4 Example of Sequential Mode Setting Procedure

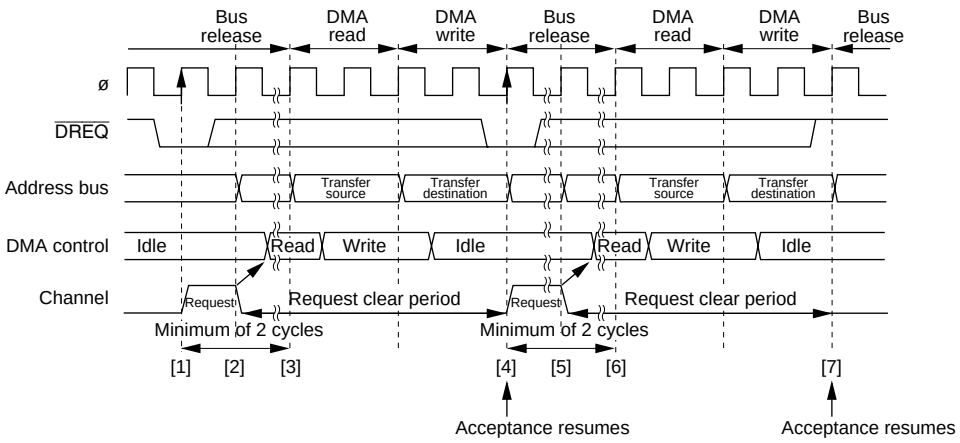


Legend:
Address $T_A = L_A$
Address $T_B = L_B$
Address $B_A = L_A + SAIDE \bullet (-1)^{SAID} \bullet (2^{DTSZ} \bullet (M \bullet N-1))$
Address $B_B = L_B + DAIDE \bullet (-1)^{DAID} \bullet (2^{DTSZ} \bullet (N-1))$
Where : L_A = Value set in MARA
L_B = Value set in MARB
N = Value set in ETCRB
M = Value set in ETCRAH and ETCRAL

Figure 7-13 Operation in Block Transfer Mode (BLKDIR = 0)

$\overline{\text{DREQ}}$ Level Activation Timing (Normal Mode): Set the DTA bit for the channel for which the $\overline{\text{DREQ}}$ pin is selected to 1.

Figure 7-25 shows an example of $\overline{\text{DREQ}}$ level activated normal mode transfer.



[1] Acceptance after transfer enabling; the $\overline{\text{DREQ}}$ pin low level is sampled on the rising edge of ø, and the request is held.
[2] [5] The request is cleared at the next bus break, and activation is started in the DMAC.
[3] [6] The DMA cycle is started.
[4] [7] Acceptance is resumed after the write cycle is completed.
(As in [1], the $\overline{\text{DREQ}}$ pin low level is sampled on the rising edge of ø, and the request is held.)

Note: In write data buffer mode, bus breaks from [2] to [7] may be hidden, and not visible.

Figure 7-25 Example of $\overline{\text{DREQ}}$ Level Activated Normal Mode Transfer

$\overline{\text{DREQ}}$ pin sampling is performed every cycle, with the rising edge of the next ø cycle after the end of the DMABCR write cycle for setting the transfer enabled state as the starting point.

When the $\overline{\text{DREQ}}$ pin low level is sampled while acceptance by means of the $\overline{\text{DREQ}}$ pin is possible, the request is held in the DMAC. Then, when activation is initiated in the DMAC, the request is cleared. After the end of the write cycle, acceptance resumes, $\overline{\text{DREQ}}$ pin low level sampling is performed again, and this operation is repeated until the transfer ends.

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address	DTCE*	Priority
TGI5B (GR5B compare match/ input capture)	TPU channel 5	61	H'047A	DTCED4	High
CMIA0	8-bit timer channel 0	64	H'0480	DTCED3	
CMIB0		65	H'0482	DTCED2	
CMIA1	8-bit timer channel 1	68	H'0488	DTCED1	
CMIB1		69	H'048A	DTCED0	
DMTEND0A (DMAC transfer end 0)	DMAC	72	H'0490	DTCEE7	
DMTEND0B (DMAC transfer end 1)		73	H'0492	DTCEE6	
DMTEND1A (DMAC transfer end 2)		74	H'0494	DTCEE5	
DMTEND1B (DMAC transfer end 3)		75	H'0496	DTCEE4	
RXI0 (reception data full 0)	SCI channel 0	81	H'04A2	DTCEE3	
TXI0 (transmit data empty 0)		82	H'04A4	DTCEE2	
RXI1 (reception data full 1)	SCI channel 1	85	H'04AA	DTCEE1	
TXI1 (transmit data empty 1)		86	H'04AC	DTCEE0	
RXI2 (reception data full 2)	SCI channel 2	89	H'04B2	DTCEF7	
TXI2 (transmit data empty 2)		90	H'04B4	DTCEF6	Low

Note: * DTCE bits with no corresponding interrupt are reserved, and should be written with 0.

9.3.3 Pin Functions

Port 2 pins also function as PPG output pins (PO7 to PO0) and TPU I/O pins (TIOCA3, TIOCB3, TIOCC3, TIOCD3, TIOCA4, TIOCB4, TIOCA5, and TIOCB5), and 8-bit timer I/O pins (TMRI0, TMCI0, TMO0, TMRI1, TMCI1, and TMO1). Port 2 pin functions are shown in table 9-5.

Table 9-5 Port 2 Pin Functions

<table>
<tr><th>Pin</th><th>Selection Method and Pin Functions</th></tr>
<tr><td>$P2_7$/PO7/TIOCB5/
TMO1</td><td>The pin function is switched as shown below according to the combination of the TPU channel 5 setting by bits MD3 to MD0 in TMDR5, bits IOB3 to IOB0 in TIOR5, bits CCLR1 and CCLR0 in TCR5, bit NDER7 in NDERL, bits OS3 to OS0 in TCSR1, and bit P27DDR.
<table>
<tr><td>OS3 to OS0</td><td colspan="4">All 0</td><td>Any 1</td></tr>
<tr><td>TPU Channel 5 Setting</td><td>Table Below (1)</td><td colspan="3">Table Below (2)</td><td>—</td></tr>
<tr><td>P27DDR</td><td>—</td><td>0</td><td>1</td><td>1</td><td>—</td></tr>
<tr><td>NDER7</td><td>—</td><td>—</td><td>0</td><td>1</td><td>—</td></tr>
<tr><td rowspan="2">Pin function</td><td rowspan="2">TIOCB5 output</td><td>$P2_7$ input</td><td>$P2_7$ output</td><td>PO7 output</td><td>TMO1 output</td></tr>
<tr><td colspan="4">TIOCB5 input *</td></tr>
</table>
Note: * TIOCB5 input when MD3 to MD0 = B'0000, B'01××, and IOB3 = 1.
<table>
<tr><td>TPU Channel 5 Setting</td><td>(2)</td><td>(1)</td><td>(2)</td><td>(2)</td><td>(1)</td><td>(2)</td></tr>
<tr><td>MD3 to MD0</td><td colspan="2">B'0000, B'01××</td><td>B'0010</td><td colspan="3">B'0011</td></tr>
<tr><td>IOB3 to IOB0</td><td>B'0000
B'0100
B'1×××</td><td>B'0001 to B'0011
B'0101 to B'0111</td><td>—</td><td>B'××00</td><td colspan="2">Other than B'××00</td></tr>
<tr><td>CCLR1, CCLR0</td><td>—</td><td>—</td><td>—</td><td>—</td><td>Other than B'10</td><td>B'10</td></tr>
<tr><td>Output function</td><td>—</td><td>Output compare output</td><td>—</td><td>—</td><td>PWM mode 2 output</td><td>—</td></tr>
</table>
×: Don't care</td></tr>
</table>

9.11.2 Register Configuration (On-Chip ROM Version Only)

Table 9-19 shows the port D register configuration.

Table 9-19 Port D Registers

Name	Abbreviation	R/W	Initial Value	Address *
Port D data direction register	PDDDR	W	H'00	H'FEBC
Port D data register	PDDR	R/W	H'00	H'FF6C
Port D register	PORTD	R	Undefined	H'FF5C
Port D MOS pull-up control register	PDPCR	R/W	H'00	H'FF73

Note: * Lower 16 bits of the address.

Port D Data Direction Register (PDDDR) (On-Chip ROM Version Only)

Bit	:	7	6	5	4	3	2	1	0
		PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PDDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port D. PDDDR cannot be read; if it is, an undefined value will be read.

PDDDR is initialized to H'00 by a power-on reset, and in hardware standby mode. It retains its prior state after a manual reset*, and in software standby mode.

Note: * Manual reset is only supported in the H8S/2357 ZTAT.

- Mode 7
  Setting a PDDDR bit to 1 makes the corresponding port D pin an output port, while clearing the bit to 0 makes the pin an input port.

- Modes 4 to 6
  The input/output direction specification by PDDDR is ignored, and port D is automatically designated for data I/O.

Port D Data Register (PDDR) (On-Chip ROM Version Only)

Bit	:	7	6	5	4	3	2	1	0
		PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDDR is an 8-bit readable/writable register that stores output data for the port D pins (PD_7 to PD_0).

PDDR is initialized to H'00 by a power-on reset, and in hardware standby mode. It retains its prior state after a manual reset*, and in software standby mode.

Note: * Manual reset is only supported in the H8S/2357 ZTAT.

Port G Data Direction Register (PGDDR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR
Modes 6, 7									
Initial value	:	Undefined	Undefined	Undefined	0	0	0	0	0
R/W	:	—	—	—	W	W	W	W	W
Modes 4, 5									
Initial value	:	Undefined	Undefined	Undefined	1	0	0	0	0
R/W	:	—	—	—	W	W	W	W	W

PGDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port G. PGDDR cannot be read, and bits 7 to 5 are reserved. If PGDDR is read, an undefined value will be read.

The PG4DDR bit is initialized by a power-on reset and in hardware standby mode, to 1 in modes 4 and 5, and to 0 in modes 6 and 7. It retains its prior state after a manual reset* and in software standby mode. The OPE bit in SBYCR is used to select whether the bus control output pins retain their output state or become high-impedance when a transition is made to software standby mode.

Note: * Manual reset is only supported in the H8S/2357 ZTAT.

- Mode 7*

  Setting a PGDDR bit to 1 makes the corresponding port G pin an output port, while clearing the bit to 0 makes the pin an input port.

- Modes 4 to 6*

  Pins PG_4 to PG_1 function as bus control output pins ($\overline{CS0}$ to $\overline{CS3}$) when the corresponding PGDDR bits are set to 1, and as input ports when the bits are cleared to 0.

  Pin PG_0 functions as the $\overline{CAS}$ output pin when DRAM interface is designated. Otherwise, setting the corresponding PGDDR bit to 1 makes the pin an output port, while clearing the bit to 0 makes the pin an input port. For details of the DRAM interfaces, see section 6, Bus Controller.

Note: * Modes 6 and 7 are provided in the on-chip ROM version only.

Port G Data Register (PGDR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	PG4DR	PG3DR	PG2DR	PG1DR	PG0DR
Initial value	:	Undefined	Undefined	Undefined	0	0	0	0	0
R/W	:	—	—	—	R/W	R/W	R/W	R/W	R/W

PGDR is an 8-bit readable/writable register that stores output data for the port G pins (PG_4 to PG_0).

Bits 7 to 5 are reserved; they return an undetermined value if read, and cannot be modified.

PGDR is initialized to H'00 (bits 4 to 0) by a power-on reset, and in hardware standby mode. It retains its prior state after a manual reset*, and in software standby mode.

Note: * Manual reset is only supported in the H8S/2357 ZTAT.

- Example of input capture operation

  Figure 10-13 shows an example of input capture operation.

  In this example both rising and falling edges have been selected as the TIOCA pin input capture input edge, falling edge has been selected as the TIOCB pin input capture input edge, and counter clearing by TGRB input capture has been designated for TCNT.

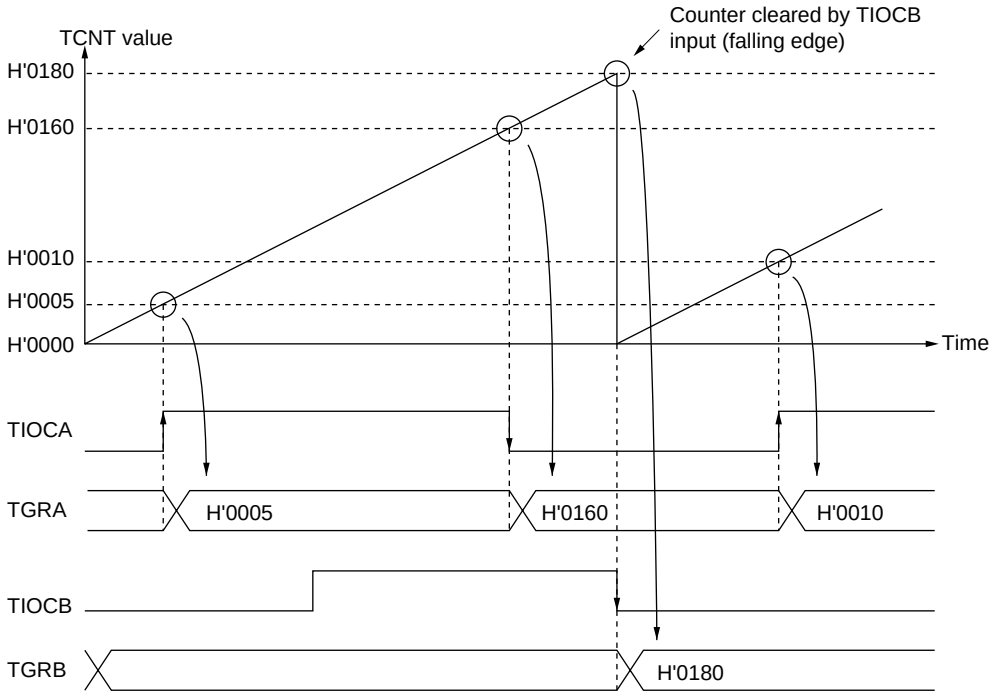


Figure 10-13 Example of Input Capture Operation

Contention between Buffer Register Write and Input Capture: If the input capture signal is generated in the T_2 state of a buffer write cycle, the buffer operation takes precedence and the write to the buffer register is not performed.

Figure 10-55 shows the timing in this case.

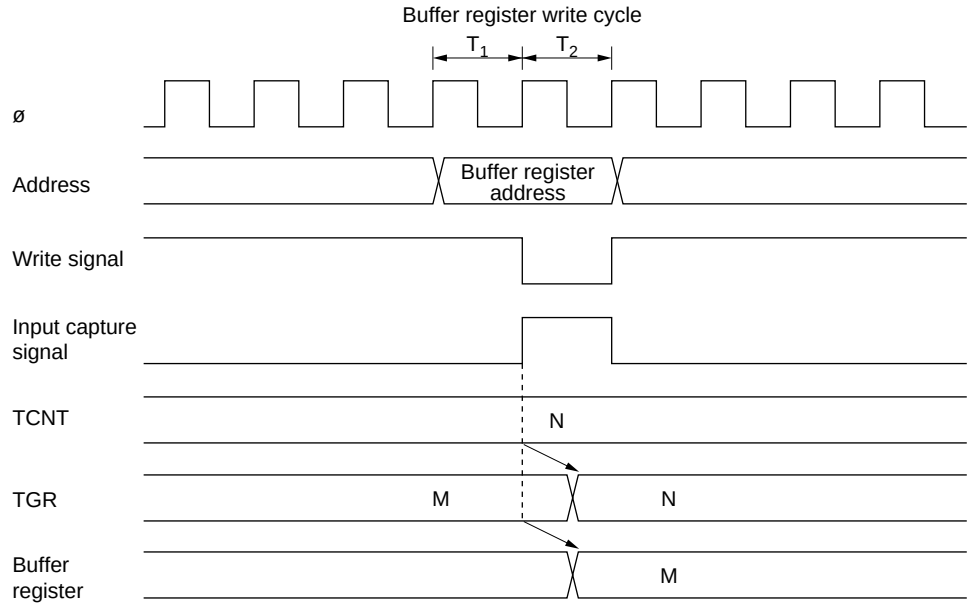


Figure 10-55 Contention between Buffer Register Write and Input Capture

Contention between Overflow/Underflow and Counter Clearing: If overflow/underflow and counter clearing occur simultaneously, the TCFV/TCFU flag in TSR is not set and TCNT clearing takes precedence.

Figure 10-56 shows the operation timing when a TGR compare match is specified as the clearing source, and H'FFFF is set in TGR.

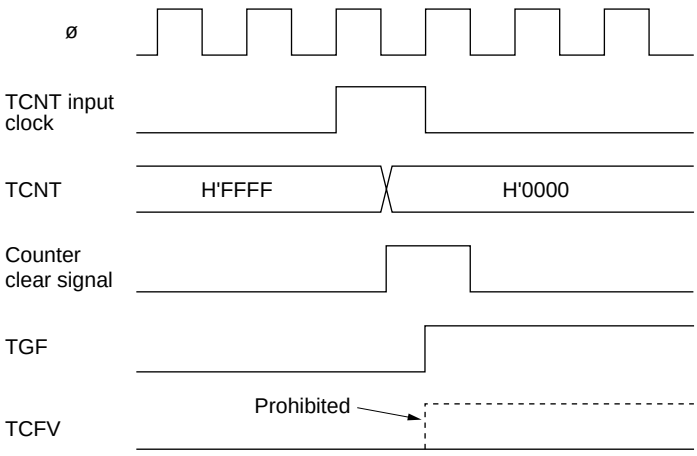
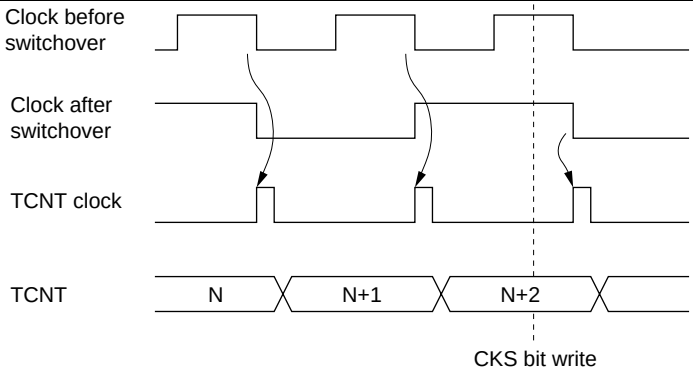


Figure 10-56 Contention between Overflow and Counter Clearing

No.	Timing of Switchover by Means of CKS1 and CKS0 Bits	TCNT Clock Operation
4	Switching from high to high	

Notes: 1. Includes switching from low to stop, and from stop to low.
2. Includes switching from stop to high.
3. Includes switching from high to stop.
4. Generated on the assumption that the switchover is a falling edge; TCNT is incremented.

12.6.6 Interrupts and Module Stop Mode

If module stop mode is entered when an interrupt has been requested, it will not be possible to clear the CPU interrupt source or the DMAC or DTC activation source. Interrupts should therefore be disabled before entering module stop mode.

Bits 2 to 0—Channel Select 2 to 0 (CH2 to CH0): Together with the SCAN bit, these bits select the analog input channels.

Only set the input channel while conversion is stopped (ADST = 0).

Group Selection	Channel Selection		Description	
CH2	**CH1**	**CH0**	**Single Mode (SCAN=0)**	**Scan Mode (SCAN=1)**
0	0	0	AN0 (Initial value)	AN0
		1	AN1	AN0, AN1
	1	0	AN2	AN0 to AN2
		1	AN3	AN0 to AN3
1	0	0	AN4	AN4
		1	AN5	AN4, AN5
	1	0	AN6	AN4 to AN6
		1	AN7	AN4 to AN7

16.2.3 A/D Control Register (ADCR)

Bit	:	7	6	5	4	3	2	1	0
		TRGS1	TRGS0	—	—	—	—	—	—
Initial value	:	0	0	1	1	1	1	1	1
R/W	:	R/W	R/W	—	—	—/(R/W)*	—/(R/W)*	—	—

Note: * Applies to the H8S/2398, H8S/2394, H8S/2392, and H8S/2390.

ADCR is an 8-bit readable/writable register that enables or disables external triggering of A/D conversion operations.

ADCR is initialized to H'3F by a reset, and in standby mode or module stop mode.

Bits 7 and 6—Timer Trigger Select 1 and 0 (TRGS1, TRGS0): Select enabling or disabling of the start of A/D conversion by a trigger signal. Only set bits TRGS1 and TRGS0 while conversion is stopped (ADST = 0).

Bit 7 TRGS1	Bit 6 TRGS0	Description	
0	0	A/D conversion start by external trigger is disabled	(Initial value)
	1	A/D conversion start by external trigger (TPU) is enabled	
1	0	A/D conversion start by external trigger (8-bit timer) is enabled	
	1	A/D conversion start by external trigger pin ($\overline{\text{ADTRG}}$) is enabled	

(1) For H8S/2357 and H8S/2352

Bits 5 to 0—Reserved: They are always read as 1 and cannot be modified.

(2) For H8S/2398, H8S/2394, H8S/2392, and H8S/2390

Bits 5, 4, 1, and 0—Reserved: They are always read as 1 and cannot be modified.

Bits 3 and 2—Reserved: Should always be written with 1.

16.2.4 Module Stop Control Register (MSTPCR)

	MSTPCRH								MSTPCRL							
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value :	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MSTPCR is a 16-bit readable/writable register that performs module stop mode control.

When the MSTP9 bit in MSTPCR is set to 1, A/D converter operation stops at the end of the bus cycle and a transition is made to module stop mode. Registers cannot be read or written to in module stop mode. For details, see section 21.5, Module Stop Mode.

MSTPCR is initialized to H'3FFF by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 9—Module Stop (MSTP9): Specifies the A/D converter module stop mode.

Bit 9 MSTP9	Description	
0	A/D converter module stop mode cleared	
1	A/D converter module stop mode set	(Initial value)

Section 20 Clock Pulse Generator

20.1 Overview

The H8S/2357 Group has a on-chip clock pulse generator (CPG) that generates the system clock (ø), the bus master clock, and internal clocks.

The clock pulse generator consists of an oscillator circuit, a duty adjustment circuit, a medium-speed clock divider, and a bus master clock selection circuit.

20.1.1 Block Diagram

Figure 20-1 shows a block diagram of the clock pulse generator.

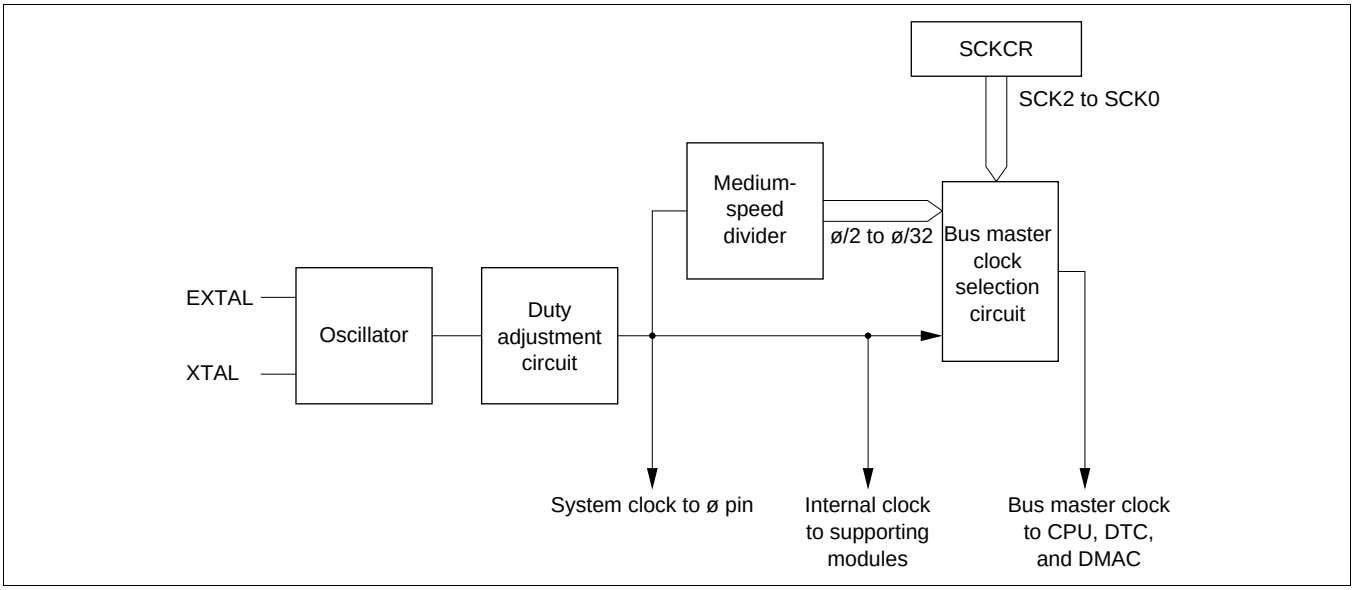


Figure 20-1 Block Diagram of Clock Pulse Generator

20.1.2 Register Configuration

The clock pulse generator is controlled by SCKCR. Table 20-1 shows the register configuration.

Table 20-1 Clock Pulse Generator Register

Name	Abbreviation	R/W	Initial Value	Address*
System clock control register	SCKCR	R/W	H'00	H'FF3A

Note:* Lower 16 bits of the address.

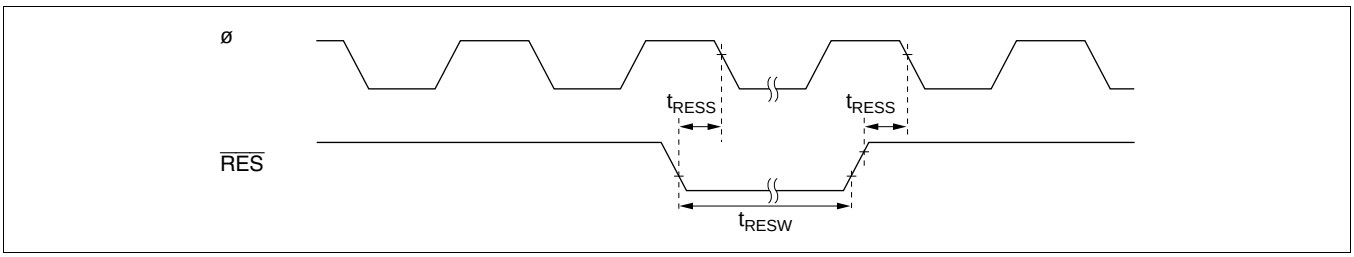


Figure 22-38 Reset Input Timing

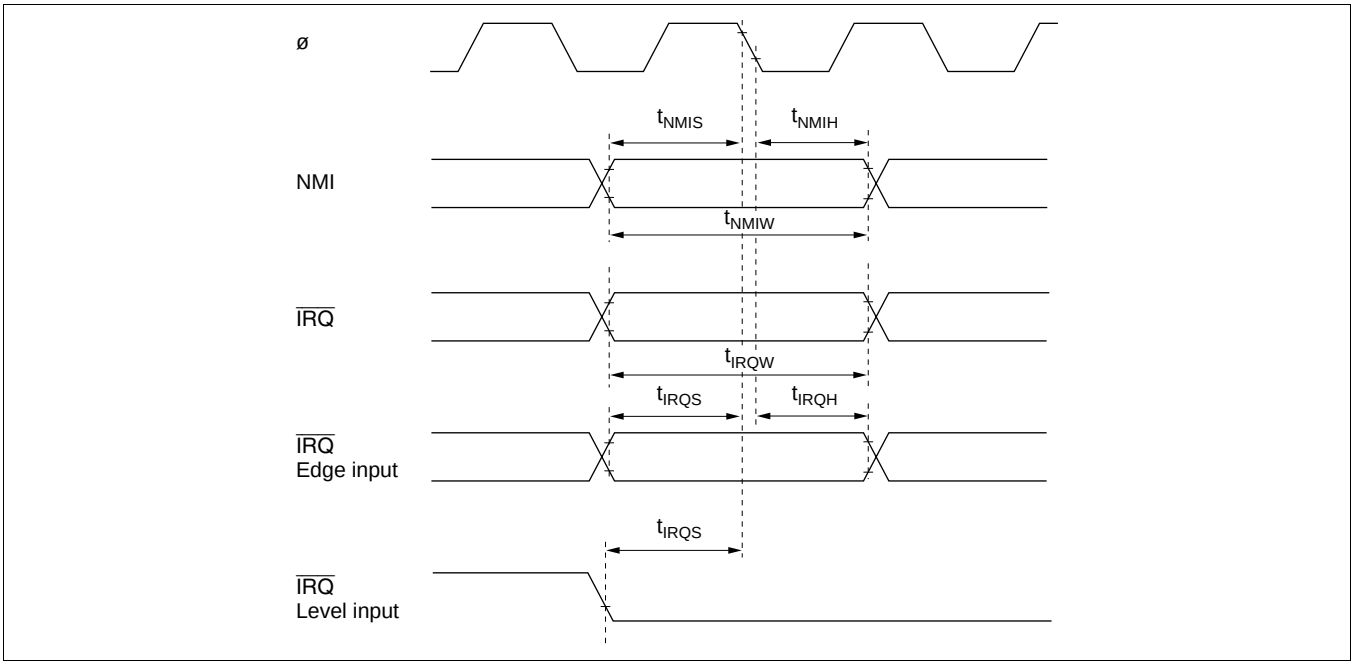


Figure 22-39 Interrupt Input Timing

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current dissipation*[2]	Normal operation	I_{CC}*[4]	—	32 (3.3 V)	80	mA	f = 13 MHz
	Sleep mode		—	22 (3.3 V)	55	mA	f = 13 MHz
	Standby mode*[3]		—	0.01	5.0	µA	$T_a \leq 50°C$
			—	—	20		$50°C < T_a$
	Flash memory programming/ erasing		—	42 (3.3 V)	80	mA	$0°C \leq T_a \leq 75°C$ f = 13 MHz
Analog power supply current	During A/D and D/A conversion	AI_{CC}	—	0.3 (3.3 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference current	During A/D and D/A conversion	AI_{CC}	—	1.6 (3.3 V)	3.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{ref} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for V_{IH} min = V_{CC} –0.5 V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 3.0$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:
I_{CC} max = 1.0 (mA) + 1.1 (mA/(MHz × V)) × V_{CC} × f [normal mode]
I_{CC} max = 1.0 (mA) + 0.75 (mA/(MHz × V)) × V_{CC} × f [sleep mode]

Table 22-35 Permissible Output Currents

Conditions: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 1, A to C	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 32 pins including ports 1 and A to C	$\sum I_{OL}$	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\sum -I_{OH}$	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 22-35.
2. When driving a darlington pair or LED directly, always insert a current-limiting resistor in the output line, as show in figures 22-65 and 22-66.

C.6 Port 6 Block Diagram

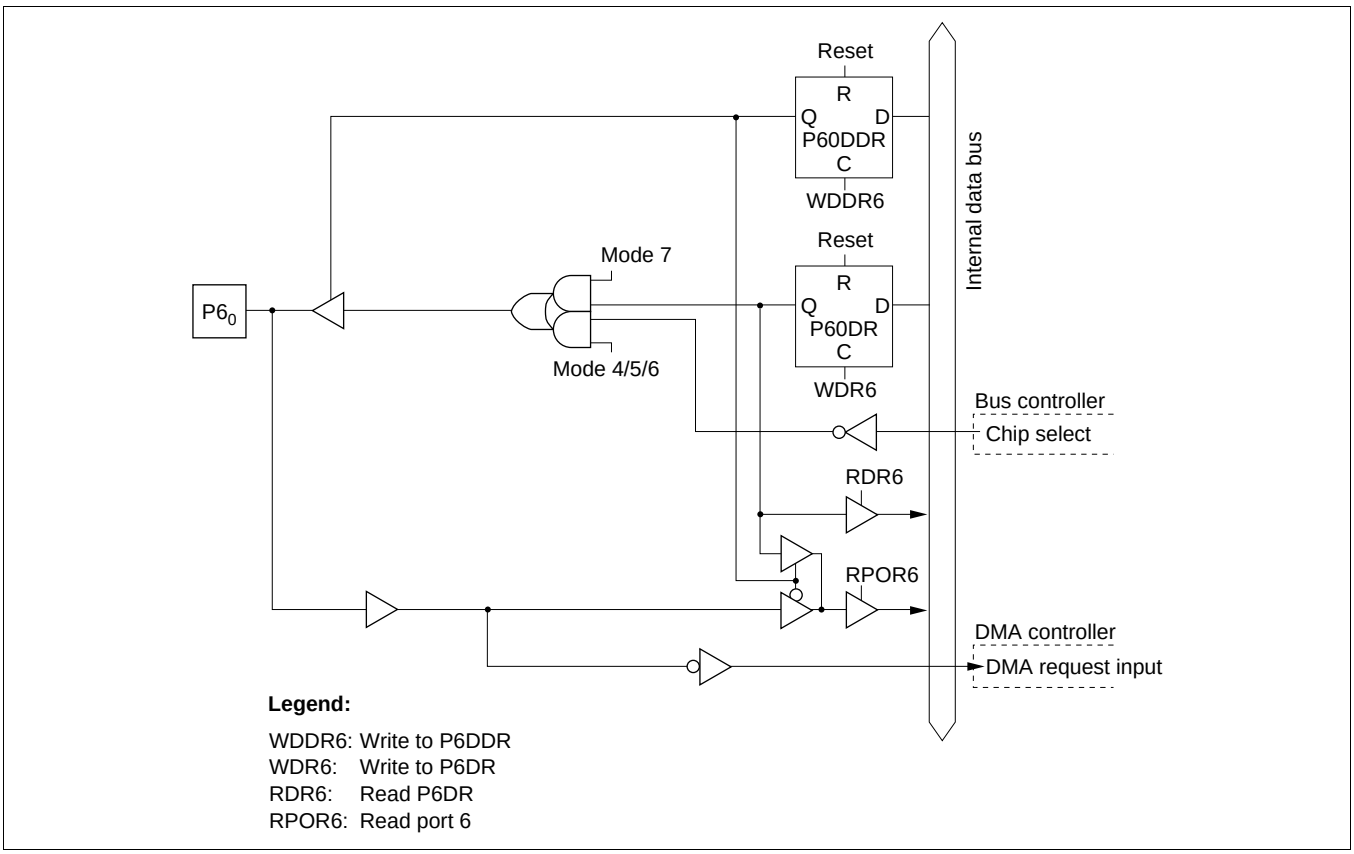


Figure C-6 (a) Port 6 Block Diagram (Pin $P6_0$)

C.10 Port D Block Diagram

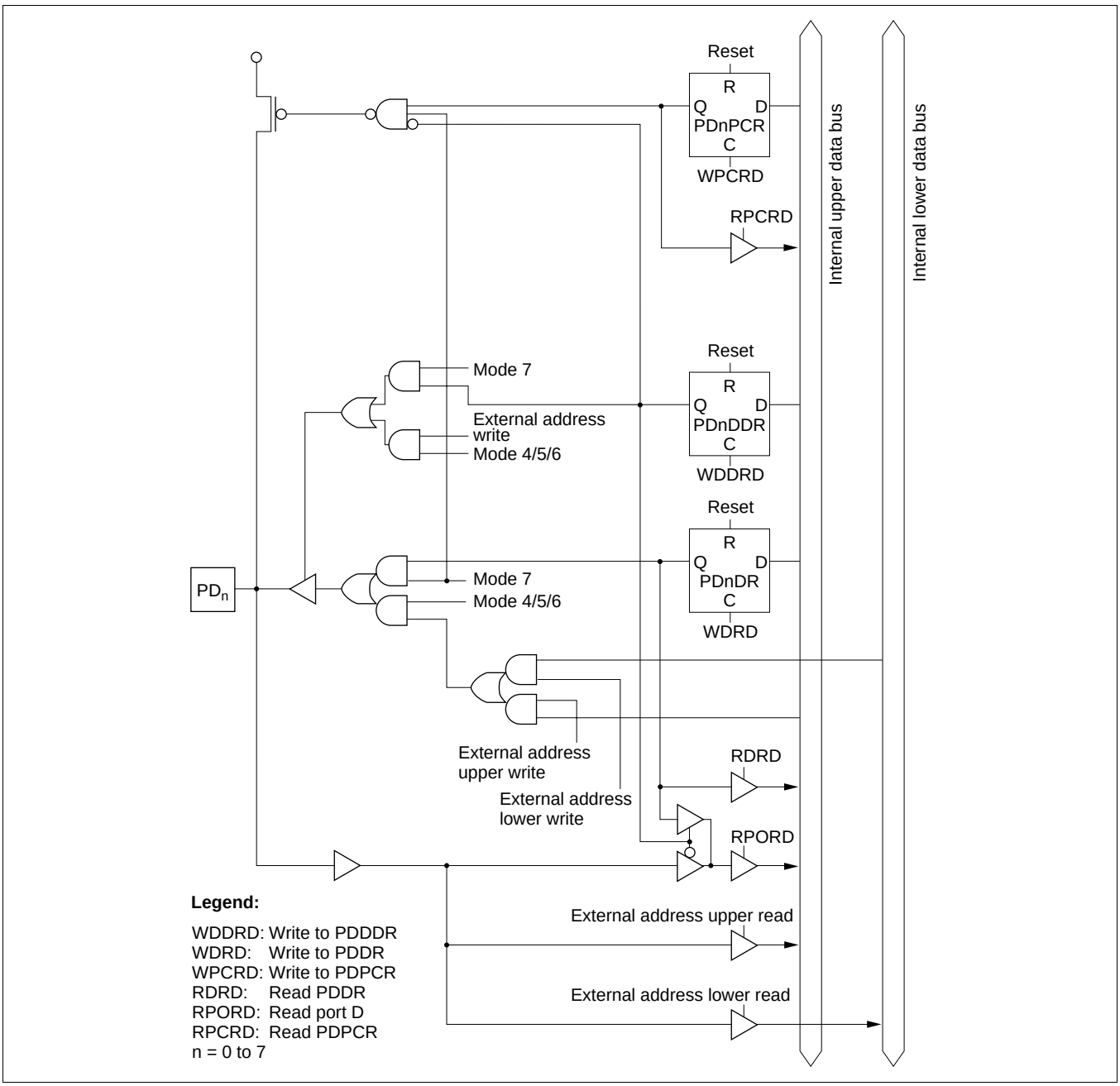


Figure C-10 Port D Block Diagram (Pin PD_0 to PD_7)

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