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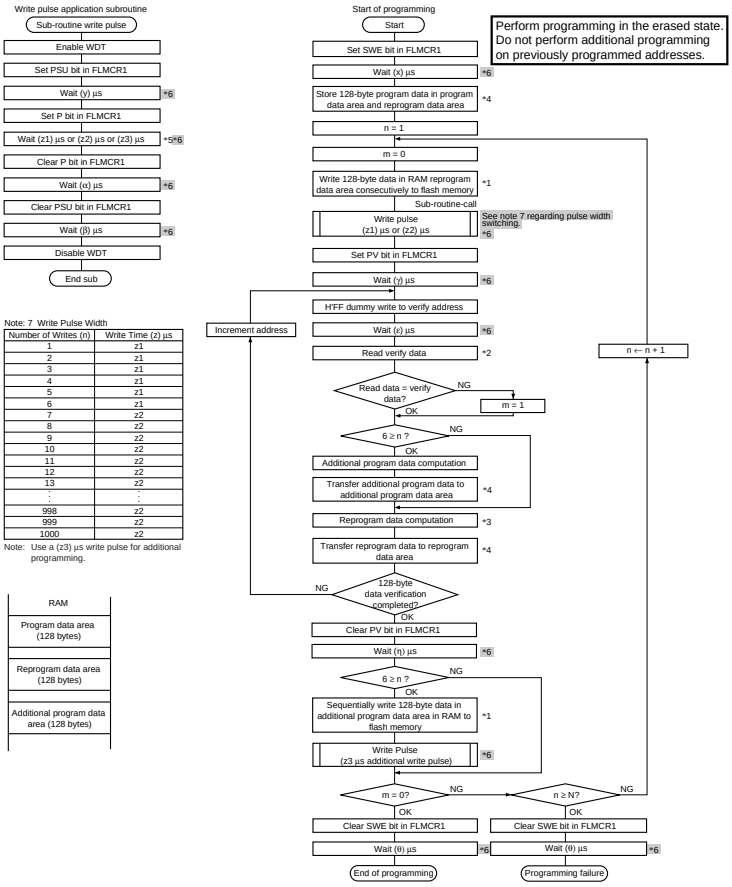
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	87
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12394te20v

Item	Page	Revision (See Manual for Details)
19.18.2 Program-Verify Mode Figure 19-48 Program/Program-Verify Flowchart	639	Figure 19-48 amended, note *6 added 
22.3.6 Flash Memory Characteristics Table 22-21 Flash Memory Characteristics (HD64F2398F20, HD64F2398TE20)	724	Table 22-21 title amended
Table 22-22 Flash Memory Characteristics (HD64F2398F20T, HD64F2398TE20T)	726	Table 22-22 added

2.5.2 Memory Data Formats

Figure 2-8 shows the data formats in memory. The CPU can access word data and longword data in memory, but word or longword data must begin at an even address. If an attempt is made to access word or longword data at an odd address, no address error occurs but the least significant bit of the address is regarded as 0, so the access starts at the preceding address. This also applies to instruction fetches.

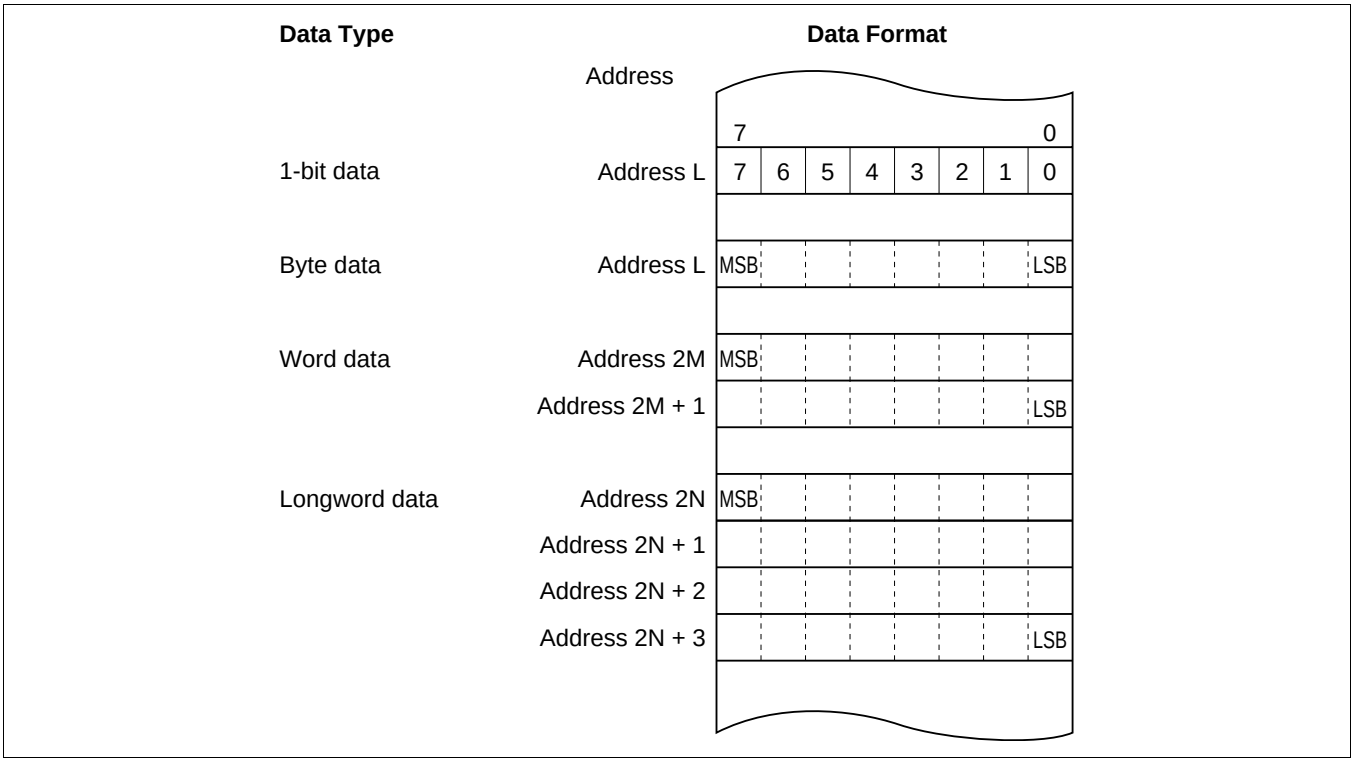


Figure 2-8 Memory Data Formats

When ER7 is used as an address register to access the stack, the operand size should be word size or longword size.

Bit 6—BREQO Pin Enable (BREQOE): Outputs a signal that requests the external bus master to drop the bus request signal ($\overline{\text{BREQ}}$) in the external bus release state, when an internal bus master performs an external space access, or when a refresh request is generated.

Bit 6 BREQOE	Description	
0	$\overline{\text{BREQO}}$ output disabled. $\overline{\text{BREQO}}$ can be used as I/O port.	(Initial value)
1	$\overline{\text{BREQO}}$ output enabled.	

Bit 5—External Address Enable (EAE): Selects whether addresses H'010000 to H'01FFFF*[2] are to be internal addresses or external addresses.

Bit 5 EAE	Description	
0	Addresses H'010000 to H'01FFFF*[2] are in on-chip ROM	
1	Addresses H'010000 to H'01FFFF*[2] are external addresses (external expansion mode) or a reserved area*[1] (single-chip mode)	(Initial value)

Notes: 1. Reserved areas should not be accessed.
2. Addresses H'010000 to H'01FFFF are in the H8S/2357. Addresses H'010000 to H'03FFFF are in the H8S/2398.

Bit 4—LCAS Select (LCASS): Write 0 to this bit when using the DRAM interface.
$\overline{\text{LCAS}}$ pin used for 2-CAS type DRAM interface $\overline{\text{LCAS}}$ signal. $\overline{\text{BREQO}}$ output and $\overline{\text{WAIT}}$ input cannot be used when $\overline{\text{LCAS}}$ signal is used.

Bit 3—DACK Timing Select (DDS): Selects the DMAC single address transfer bus timing for the DRAM interface.

Bit 3 DDS	Description	
0	When DMAC single address transfer is performed in DRAM space, full access is always executed	
	$\overline{\text{DACK}}$ signal goes low from T_r or T_1 cycle	
1	Burst access is possible when DMAC single address transfer is performed in DRAM space	
	$\overline{\text{DACK}}$ signal goes low from T_{c1} or T_2 cycle	(Initial value)

Bit 2—Reserved: Only 1 should be written to this bit.

Bit 1—Write Data Buffer Enable (WDBE): Selects whether or not the write buffer function is used for an external write cycle or DMAC single address cycle.

Bit 1 WDBE	Description	
0	Write data buffer function not used	(Initial value)
1	Write data buffer function used	

Bits 3 and 1—Data Transfer Interrupt Enable B (DTIEB): These bits enable or disable an interrupt to the CPU or DTC when transfer is interrupted. If the DTIEB bit is set to 1 when DTME = 0, the DMAC regards this as indicating a break in the transfer, and issues a transfer break interrupt request to the CPU or DTC.

A transfer break interrupt can be canceled either by clearing the DTIEB bit to 0 in the interrupt handling routine, or by performing processing to continue transfer by setting the DTME bit to 1.

Bit 3—Data Transfer Interrupt Enable 1B (DTIE1B): Enables or disables the channel 1 transfer break interrupt.

Bit 3 DTIE1B	Description	
0	Transfer break interrupt disabled	(Initial value)
1	Transfer break interrupt enabled	

Bit 1—Data Transfer Interrupt Enable 0B (DTIE0B): Enables or disables the channel 0 transfer break interrupt.

Bit 1 DTIE0B	Description	
0	Transfer break interrupt disabled	(Initial value)
1	Transfer break interrupt enabled	

Bits 2 and 0—Data Transfer End Interrupt Enable A (DTIEA): These bits enable or disable an interrupt to the CPU or DTC when transfer ends. If DTIEA bit is set to 1 when DTE = 0, the DMAC regards this as indicating the end of a transfer, and issues a transfer end interrupt request to the CPU or DTC.

A transfer end interrupt can be canceled either by clearing the DTIEA bit to 0 in the interrupt handling routine, or by performing processing to continue transfer by setting the transfer counter and address register again, and then setting the DTE bit to 1.

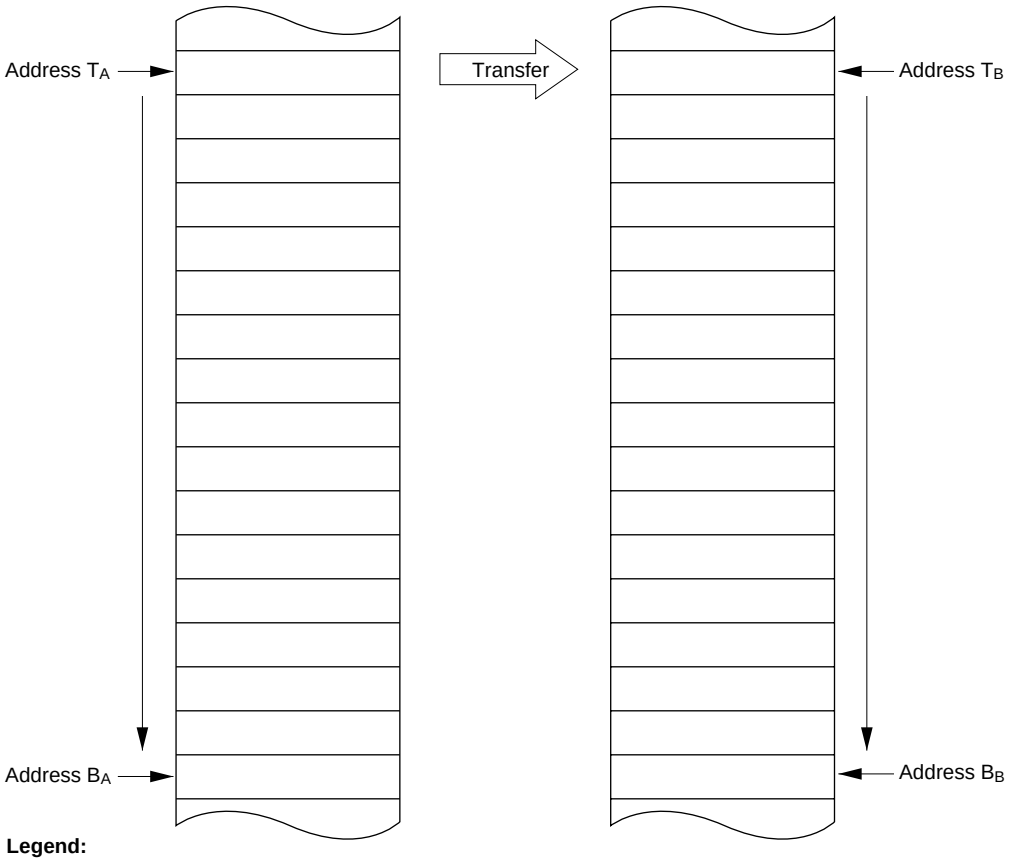
Bit 2—Data Transfer Interrupt Enable 1A (DTIE1A): Enables or disables the channel 1 transfer end interrupt.

Bit 2 DTIE1A	Description	
0	Transfer end interrupt disabled	(Initial value)
1	Transfer end interrupt enabled	

Bit 0—Data Transfer Interrupt Enable 0A (DTIE0A): Enables or disables the channel 0 transfer end interrupt.

Bit 0 DTIE0A	Description	
0	Transfer end interrupt disabled	(Initial value)
1	Transfer end interrupt enabled	

Figure 7-11 illustrates operation in normal mode.

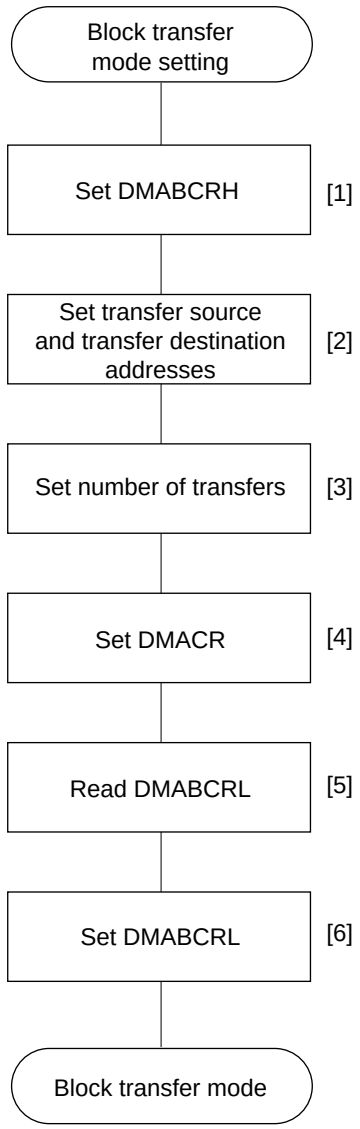


Legend:
Address $T_A = L_A$
Address $T_B = L_B$
Address $B_A = L_A + SAIDE \bullet (-1)^{SAID} \bullet (2^{DTSZ} \bullet (N-1))$
Address $B_B = L_B + DAIDE \bullet (-1)^{DAID} \bullet (2^{DTSZ} \bullet (N-1))$
Where : L_A = Value set in MARA
L_B = Value set in MARB
N = Value set in ETCRA

Figure 7-11 Operation in Normal Mode

Transfer requests (activation sources) are external requests and auto-requests.

With auto-request, the DMAC is only activated by register setting, and the specified number of transfers are performed automatically. With auto-request, cycle steal mode or burst mode can be selected. In cycle steal mode, the bus is released to another bus master each time a transfer is performed. In burst mode, the bus is held continuously until transfer ends.



[1] Set each bit in DMABCRH.
- Set the FAE bit to 1 to select full address mode.
- Specify enabling or disabling of internal interrupt clearing with the DTA bit.

[2] Set the transfer source address in MARA, and the transfer destination address in MARB.

[3] Set the block size in both ETCRAH and ETCRAL. Set the number of transfers in ETCRB.

[4] Set each bit in DMACRA and DMACRB.
- Set the transfer data size with the DTSZ bit.
- Specify whether MARA is to be incremented, decremented, or fixed, with the SAID and SAIDE bits.
- Set the BLKE bit to 1 to select block transfer mode.
- Specify whether the transfer source or the transfer destination is a block area with the BLKDIR bit.
- Specify whether MARB is to be incremented, decremented, or fixed, with the DAID and DAIDE bits.
- Select the activation source with bits DTF3 to DTF0.

[5] Read DTE = 0 and DTME = 0 in DMABCRL.

[6] Set each bit in DMABCRL.
- Specify enabling or disabling of transfer end interrupts to the CPU with the DTIE bit.
- Set both the DTME bit and the DTE bit to 1 to enable transfer.

Figure 7-16 Example of Block Transfer Mode Setting Procedure

8.3.3 DTC Vector Table

Figure 8-4 shows the correspondence between DTC vector addresses and register information.

Table 8-4 shows the correspondence between activation, vector addresses, and DTCER bits. When the DTC is activated by software, the vector address is obtained from: H'0400 + (DTVECR[6:0] << 1) (where << 1 indicates a 1-bit left shift). For example, if DTVECR is H'10, the vector address is H'0420.

The DTC reads the start address of the register information from the vector address set for each activation source, and then reads the register information from that start address. The register information can be placed at predetermined addresses in the on-chip RAM. The start address of the register information should be an integral multiple of four.

The configuration of the vector address is the same in both normal and advanced modes, a 2-byte unit being used in both cases. These two bytes specify the lower bits of the address in the on-chip RAM.

Table 10-1 TPU Functions

Item		Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
Count clock		ø/1 ø/4 ø/16 ø/64 TCLKA TCLKB TCLKC TCLKD	ø/1 ø/4 ø/16 ø/64 ø/256 TCLKA TCLKB	ø/1 ø/4 ø/16 ø/64 ø/1024 TCLKA TCLKB TCLKC	ø/1 ø/4 ø/16 ø/64 ø/256 ø/1024 ø/4096 TCLKA	ø/1 ø/4 ø/16 ø/64 ø/1024 TCLKA TCLKC	ø/1 ø/4 ø/16 ø/64 ø/256 TCLKA TCLKC TCLKD
General registers		TGR0A TGR0B	TGR1A TGR1B	TGR2A TGR2B	TGR3A TGR3B	TGR4A TGR4B	TGR5A TGR5B
General registers/ buffer registers		TGR0C TGR0D	—	—	TGR3C TGR3D	—	—
I/O pins		TIOCA0 TIOCB0 TIOCC0 TIOCD0	TIOCA1 TIOCB1	TIOCA2 TIOCB2	TIOCA3 TIOCB3 TIOCC3 TIOCD3	TIOCA4 TIOCB4	TIOCA5 TIOCB5
Counter clear function		TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture
Compare match output	0 output	○	○	○	○	○	○
	1 output	○	○	○	○	○	○
	Toggle output	○	○	○	○	○	○
Input capture function		○	○	○	○	○	○
Synchronous operation		○	○	○	○	○	○
PWM mode		○	○	○	○	○	○
Phase counting mode		—	○	○	—	○	○
Buffer operation		○	—	—	○	—	—

- When TGR is an input capture register

  Figure 10-20 shows an operation example in which TGRA has been designated as an input capture register, and buffer operation has been designated for TGRA and TGRC.

  Counter clearing by TGRA input capture has been set for TCNT, and both rising and falling edges have been selected as the TIOCA pin input capture input edge.

  As buffer operation has been set, when the TCNT value is stored in TGRA upon occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC.

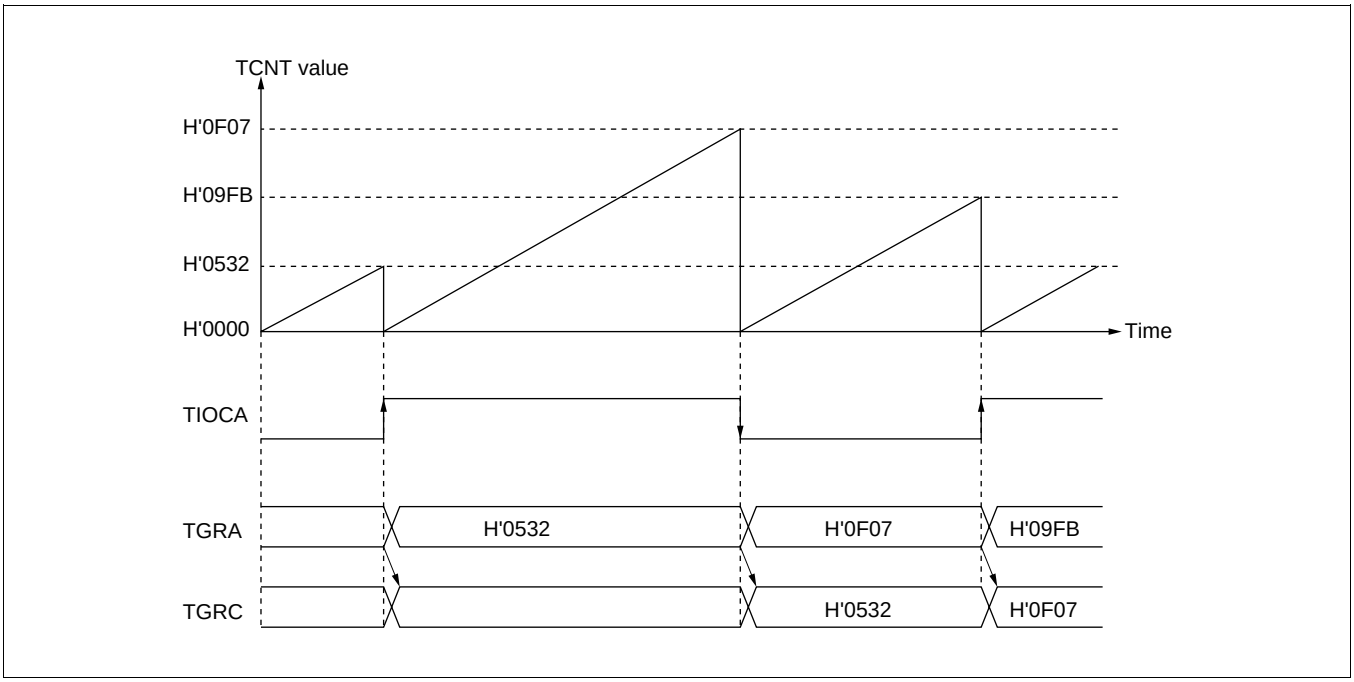


Figure 10-20 Example of Buffer Operation (2)

Bits 3 and 2—Group 1 Compare Match Select 1 and 0 (G1CMS1, G1CMS0): These bits select the compare match that triggers pulse output group 1 (pins PO7 to PO4).

		Description
Bit 3 G1CMS1	**Bit 2 G1CMS0**	**Output Trigger for Pulse Output Group 1**
0	0	Compare match in TPU channel 0
	1	Compare match in TPU channel 1
1	0	Compare match in TPU channel 2
	1	Compare match in TPU channel 3 (Initial value)

Bits 1 and 0—Group 0 Compare Match Select 1 and 0 (G0CMS1, G0CMS0): These bits select the compare match that triggers pulse output group 0 (pins PO3 to PO0).

		Description
Bit 1 G0CMS1	**Bit 0 G0CMS0**	**Output Trigger for Pulse Output Group 0**
0	0	Compare match in TPU channel 0
	1	Compare match in TPU channel 1
1	0	Compare match in TPU channel 2
	1	Compare match in TPU channel 3 (Initial value)

11.2.6 PPG Output Mode Register (PMR)

Bit	:	7	6	5	4	3	2	1	0
		G3INV	G2INV	G1INV	G0INV	G3NOV	G2NOV	G1NOV	G0NOV
Initial value	:	1	1	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PMR is an 8-bit readable/writable register that selects pulse output inversion and non-overlapping operation for each group.

The output trigger period of a non-overlapping operation PPG output waveform is set in TGRB and the non-overlap margin is set in TGRA. The output values change at compare match A and B.

For details, see section 11.3.4, Non-Overlapping Pulse Output.

PMR is initialized to H'F0 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Group 3 Inversion (G3INV): Selects direct output or inverted output for pulse output group 3 (pins PO15 to PO12).

Bit 7 G3INV	**Description**
0	Inverted output for pulse output group 3 (low-level output at pin for a 1 in PODRH)
1	Direct output for pulse output group 3 (high-level output at pin for a 1 in PODRH) (Initial value)

14.4 SCI Interrupts

The SCI has four interrupt sources: the transmit-end interrupt (TEI) request, receive-error interrupt (ERI) request, receive-data-full interrupt (RXI) request, and transmit-data-empty interrupt (TXI) request. Table 14-12 shows the interrupt sources and their relative priorities. Individual interrupt sources can be enabled or disabled with the TIE, RIE, and TEIE bits in the SCR. Each kind of interrupt request is sent to the interrupt controller independently.

When the TDRE flag in SSR is set to 1, a TXI interrupt request is generated. When the TEND flag in SSR is set to 1, a TEI interrupt request is generated. A TXI interrupt can activate the DMAC or DTC to perform data transfer. The TDRE flag is cleared to 0 automatically when data transfer is performed by the DMAC or DTC. The DMAC and DTC cannot be activated by a TEI interrupt request.

When the RDRF flag in SSR is set to 1, an RXI interrupt request is generated. When the ORER, PER, or FER flag in SSR is set to 1, an ERI interrupt request is generated. An RXI interrupt can activate the DMAC or DTC to perform data transfer. The RDRF flag is cleared to 0 automatically when data transfer is performed by the DMAC or DTC. The DMAC and DTC cannot be activated by an ERI interrupt request.

Also note that the DMAC cannot be activated by an SCI channel 2 interrupt.

19.5 Programming (H8S/2357 ZTAT)

19.5.1 Overview

Table 19-6 shows how to select the program, verify, and program-inhibit modes in PROM mode.

Table 19-6 Mode Selection in PROM Mode

	Pins						
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{PGM}$**	**V_{PP}**	**V_{CC}**	**EO_7 to EO_0**	**EA_{16} to EA_0**
Program	L	H	L	V_{PP}	V_{CC}	Data input	Address input
Verify	L	L	H	V_{PP}	V_{CC}	Data output	Address input
Program-inhibit	L	L	L	V_{PP}	V_{CC}	High impedance	Address input
	L	H	H				
	H	L	L				
	H	H	H				

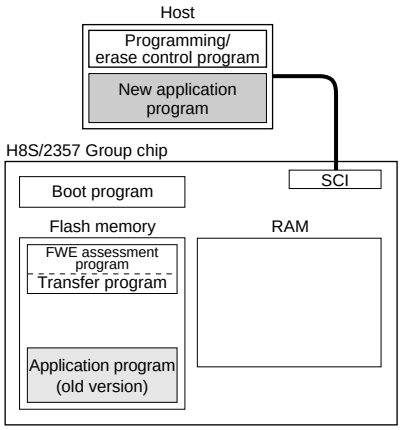
Legend:
L: Low voltage level
H: High voltage level
V_{PP}: V_{PP} voltage level
V_{CC}: V_{CC} voltage level

Programming and verification should be carried out using the same specifications as for the standard HN27C101 EPROM.

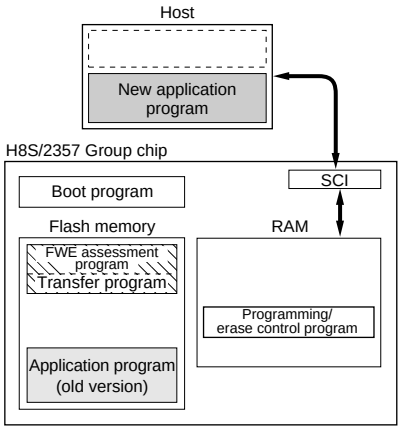
However, do not set the PROM programmer to page mode, as the H8S/2357 does not support page programming. A PROM programmer that only supports page programming cannot be used. When choosing a PROM programmer, check that it supports high-speed programming in byte units. Always set addresses within the range H'00000 to H'1FFFF.

- User program mode

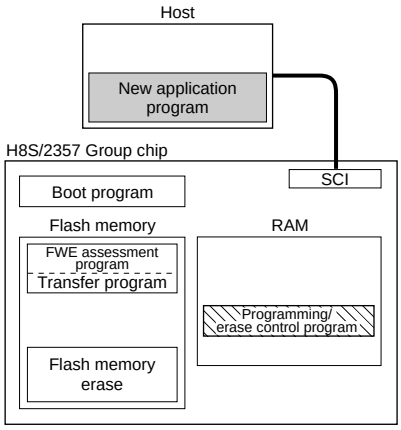
1. Initial state
   (1) The FWE assessment program that confirms that the FWE pin has been driven high, and (2) the program that will transfer the programming/ erase control program to on-chip RAM should be written into the flash memory by the user beforehand. (3) The programming/erase control program should be prepared in the host or in the flash memory.



2. Programming/erase control program transfer
   When the FWE pin is driven high, user software confirms this fact, executes the transfer program in the flash memory, and transfers the programming/erase control program to RAM.



3. Flash memory initialization
   The programming/erase program in RAM is executed, and the flash memory is initialized (to H'FF). Erasing can be performed in block units, but not in byte units.



4. Writing new application program
   Next, the new application program in the host is written into the erased flash memory blocks. Do not write to unerased blocks.

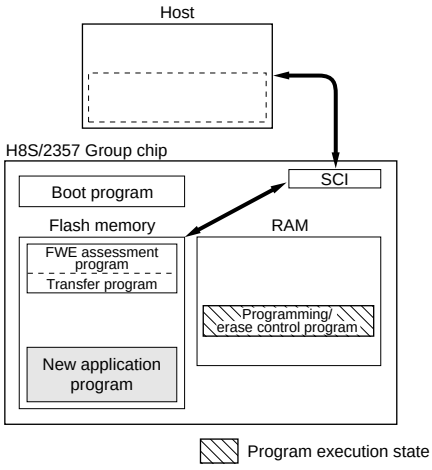


Figure 19-10 User Program Mode (Example)

19.22.2 Socket Adapters and Memory Map

In programmer mode, a socket adapter is connected to the chip as shown in figure 19-54. Figure 19-53 shows the on-chip ROM memory map and figure 19-54 show the socket adapter pin assignments.

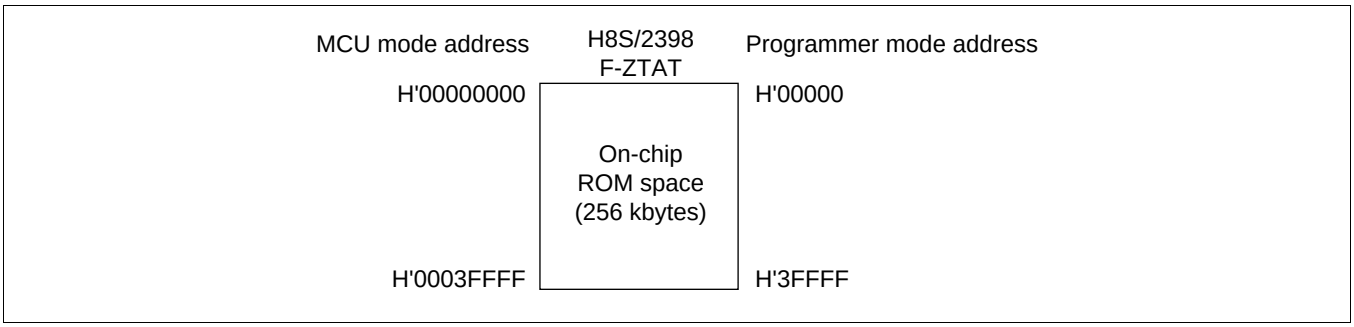


Figure 19-53 Memory Map in Programmer Mode

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current dissipation*2	Normal operation	I_{CC}*4	—	23 (3.0 V)	62	mA	f = 10 MHz
	Sleep mode		—	16 (3.0 V)	42	mA	f = 10 MHz
	Standby mode*3		—	0.01	5.0	µA	$T_a \leq 50°C$
			—	—	20.0		$50°C < T_a$
Analog power supply current	During A/D and D/A conversion	AI_{CC}	—	0.2 (3.0 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference current	During A/D and D/A conversion	AI_{CC}	—	1.4 (3.0 V)	3.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{ref} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for V_{IH} min = V_{CC} –0.5 V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:
I_{CC} max = 1.0 (mA) + 1.1 (mA/(MHz × V)) × V_{CC} × f [normal mode]
I_{CC} max = 1.0 (mA) + 0.75 (mA/(MHz × V)) × V_{CC} × f [sleep mode]

Table 22-24 DC Characteristics (3)

Conditions: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, V_{ref} = 3.0 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V*1,
T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Port 2, $P6_4$ to $P6_7$, PA_4 to PA_7	V_T^-	$V_{CC} \times 0.2$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} +0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Ports 1, 3, 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Port 4		$V_{CC} \times 0.7$	—	AV_{CC} +0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, Ports 1, 3 to 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		–0.3	—	$V_{CC} \times 0.2$	V	V_{CC} < 4.0 V
					0.8		V_{CC} = 4.0 to 5.5 V

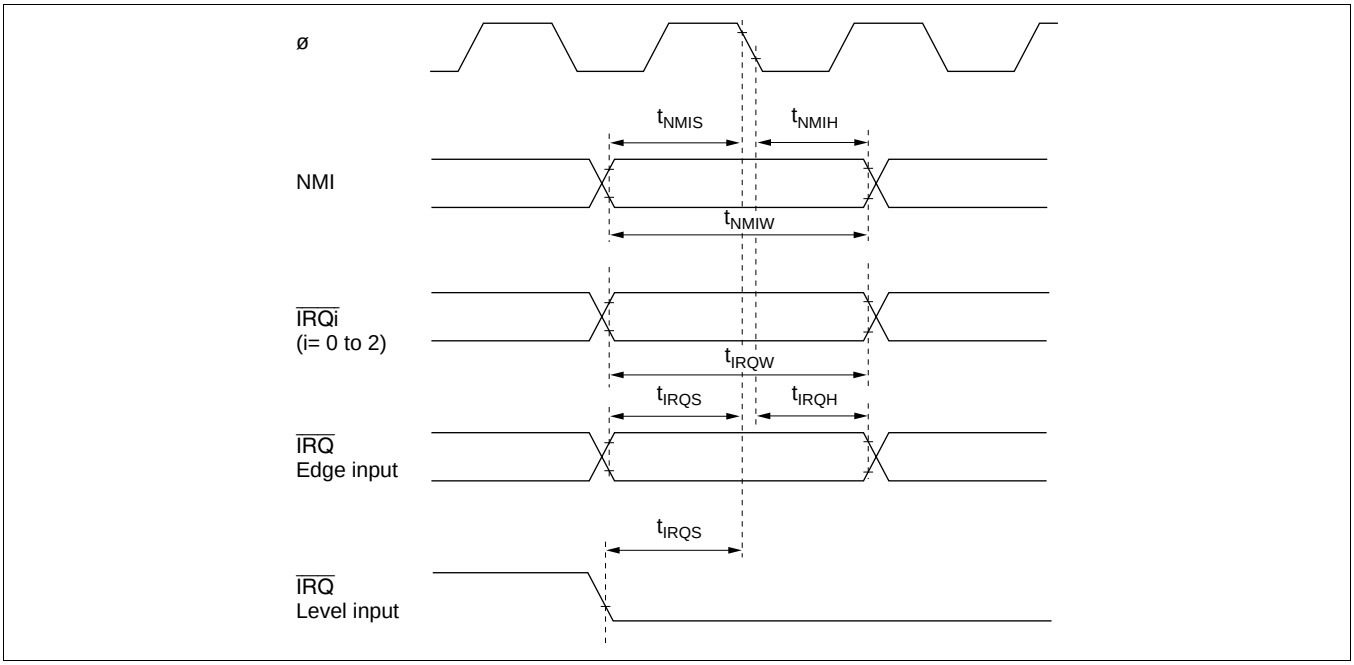


Figure 22-71 Interrupt Input Timing

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)									Operation	Condition Code					No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa	|		I	H	N	Z	V	C	Advanced
BCLR	BCLR Rn,@aa:32	B						8				(Rn8 of @aa:32)←0	—	—	—	—	—	—	6
BNOT	BNOT #xx:3,Rd	B	2									(#xx:3 of Rd8)←[¬ (#xx:3 of Rd8)]	—	—	—	—	—	—	1
	BNOT #xx:3,@ERd	B			4							(#xx:3 of @ERd)← [¬ (#xx:3 of @ERd)]	—	—	—	—	—	—	4
	BNOT #xx:3,@aa:8	B						4				(#xx:3 of @aa:8)← [¬ (#xx:3 of @aa:8)]	—	—	—	—	—	—	4
	BNOT #xx:3,@aa:16	B						6				(#xx:3 of @aa:16)← [¬ (#xx:3 of @aa:16)]	—	—	—	—	—	—	5
	BNOT #xx:3,@aa:32	B						8				(#xx:3 of @aa:32)← [¬ (#xx:3 of @aa:32)]	—	—	—	—	—	—	6
	BNOT Rn,Rd	B	2									(Rn8 of Rd8)←[¬ (Rn8 of Rd8)]	—	—	—	—	—	—	1
	BNOT Rn,@ERd	B			4							(Rn8 of @ERd)←[¬ (Rn8 of @ERd)]	—	—	—	—	—	—	4
	BNOT Rn,@aa:8	B						4				(Rn8 of @aa:8)←[¬ (Rn8 of @aa:8)]	—	—	—	—	—	—	4
	BNOT Rn,@aa:16	B						6				(Rn8 of @aa:16)← [¬ (Rn8 of @aa:16)]	—	—	—	—	—	—	5
	BNOT Rn,@aa:32	B						8				(Rn8 of @aa:32)← [¬ (Rn8 of @aa:32)]	—	—	—	—	—	—	6
BTST	BTST #xx:3,Rd	B	2									¬ (#xx:3 of Rd8)→Z	—	—	—	↕	—	—	1
	BTST #xx:3,@ERd	B			4							¬ (#xx:3 of @ERd)→Z	—	—	—	↕	—	—	3
	BTST #xx:3,@aa:8	B						4				¬ (#xx:3 of @aa:8)→Z	—	—	—	↕	—	—	3
	BTST #xx:3,@aa:16	B						6				¬ (#xx:3 of @aa:16)→Z	—	—	—	↕	—	—	4

A.3 Operation Code Map

Table A-3 shows the operation code map.

Table A-3 Operation Code Map (1)

Instruction code

1st byte		2nd byte	
AH	AL	BH	BL

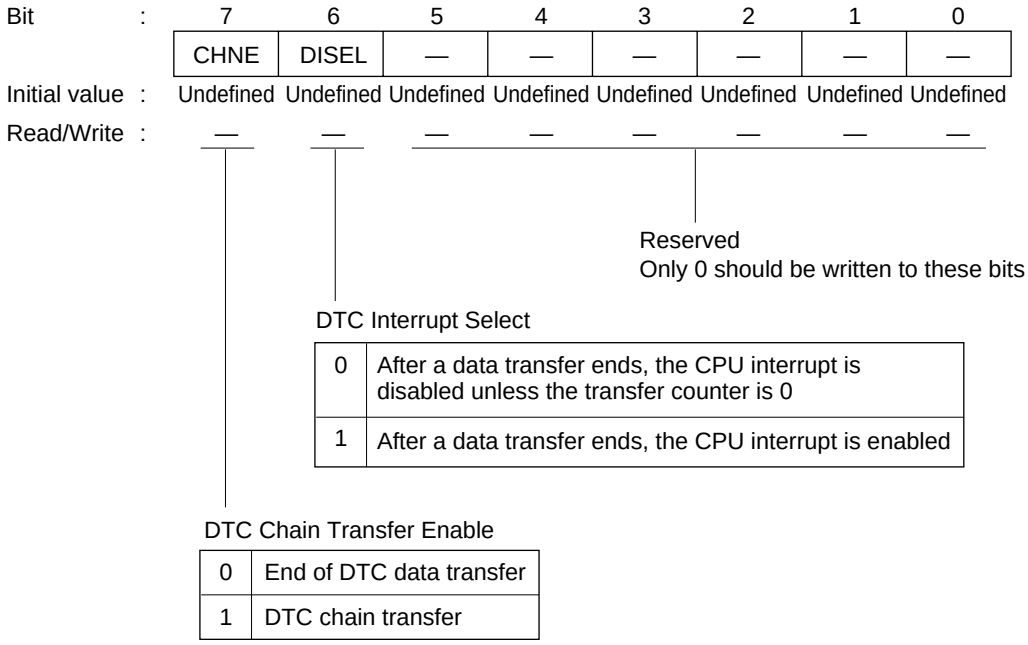
Instruction when most significant bit of BH is 0.

Instruction when most significant bit of BH is 1.

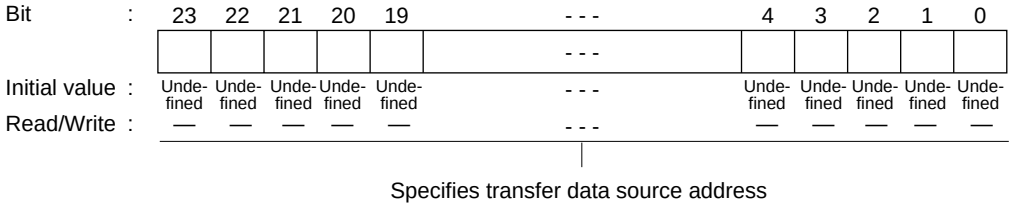
AH \ AL	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	Table A.3(2)	STC / STMAC*	LDC / LDMAC*	ORC	XORC	ANDC	LDC	ADD		Table A.3(2)	Table A.3(2)	MOV		ADDX	Table A.3(2)
1	Table A.3(2)	Table A.3(2)	Table A.3(2)	Table A.3(2)	OR	XOR	AND	Table A.3(2)	SUB		Table A.3(2)	Table A.3(2)	CMP		SUBX	Table A.3(2)
2	MOV.B															
3																
4	BRA	BRN	BHI	BLS	BCC	BCS	BNE	BEQ	BVC	BVS	BPL	BMI	BGE	BLT	BGT	BLE
5	MULXU	DIVXU	MULXU	DIVXU	RTS	BSR	RTE	TRAPA	Table A.3(2)	JMP			BSR	JSR		
6	BSET	BNOT	BCLR	BTST	OR / BOR / BIOR	XOR / BXOR / BIXOR	AND / BAND / BIAND	BST / BIST / BLD / BILD	MOV		Table A.3(2)		MOV			
7									MOV	Table A.3(2)	Table A.3(2)	EEPMOV	Table A.3(3)			
8	ADD															
9	ADDX															
A	CMP															
B	SUBX															
C	OR															
D	XOR															
E	AND															
F	MOV															

Note: * Cannot be used in the H8S/2357 Group.

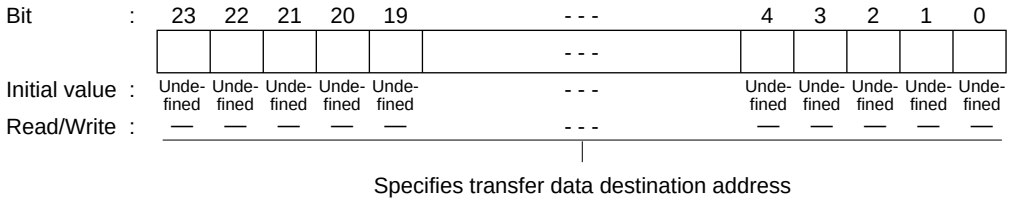
MRB—DTC Mode Register B **H'F800—H'FBFF** **DTC**



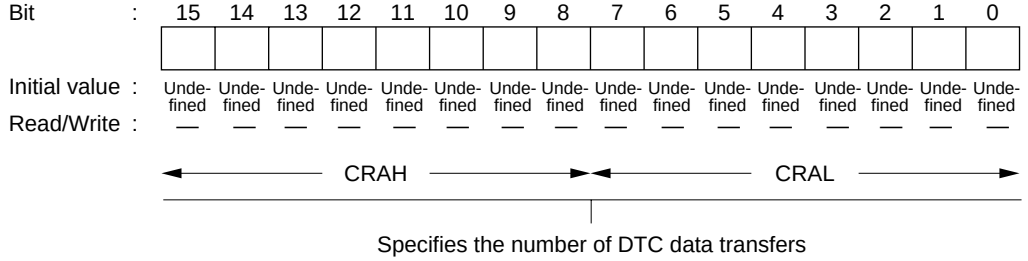
SAR—DTC Source Address Register **H'F800—H'FBFF** **DTC**



DAR—DTC Destination Address Register **H'F800—H'FBFF** **DTC**



CRA—DTC Transfer Count Register A **H'F800—H'FBFF** **DTC**



SYSCR—System Control Register H'FF39 MCU