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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	87
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2357te20iv

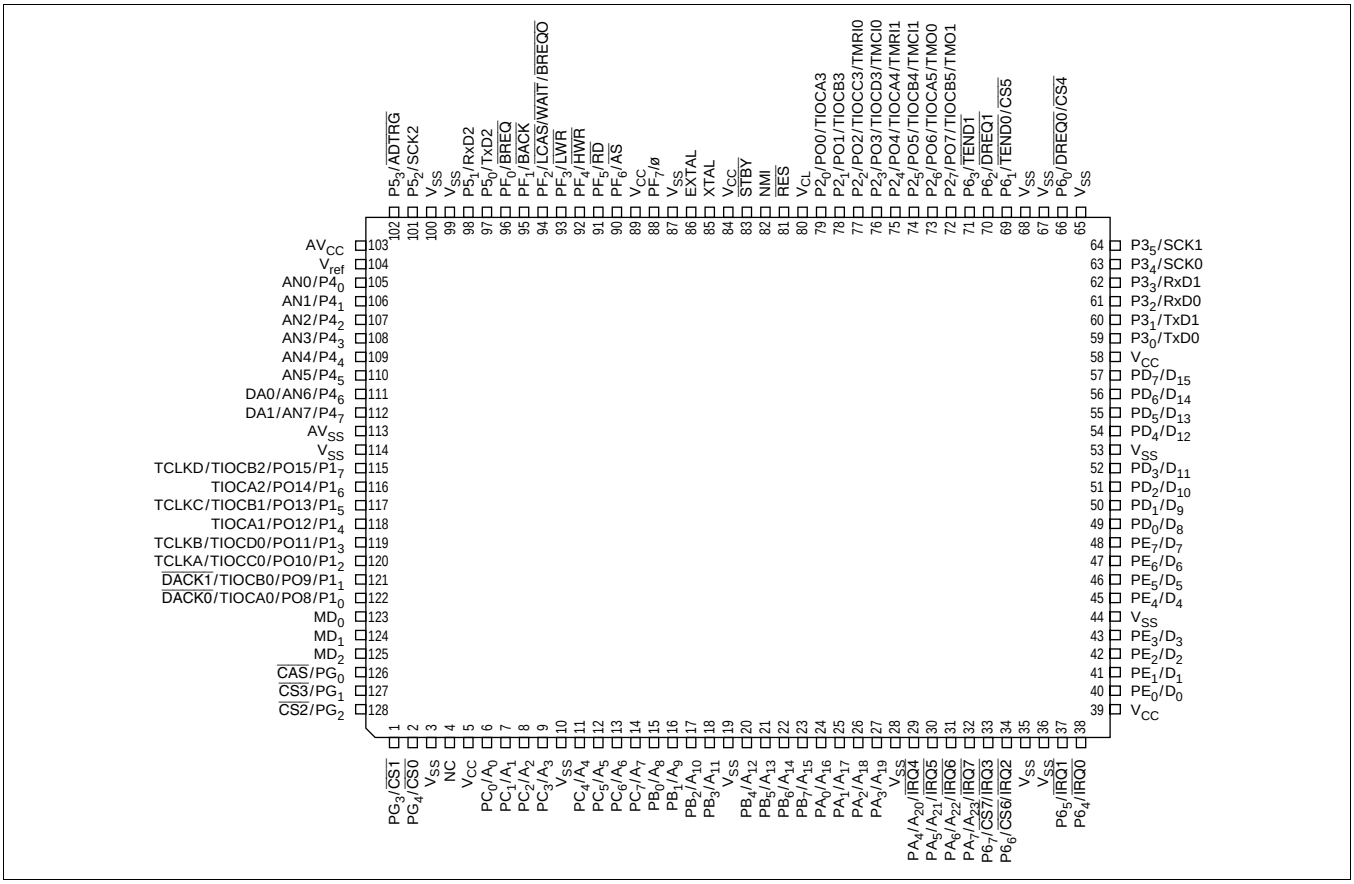
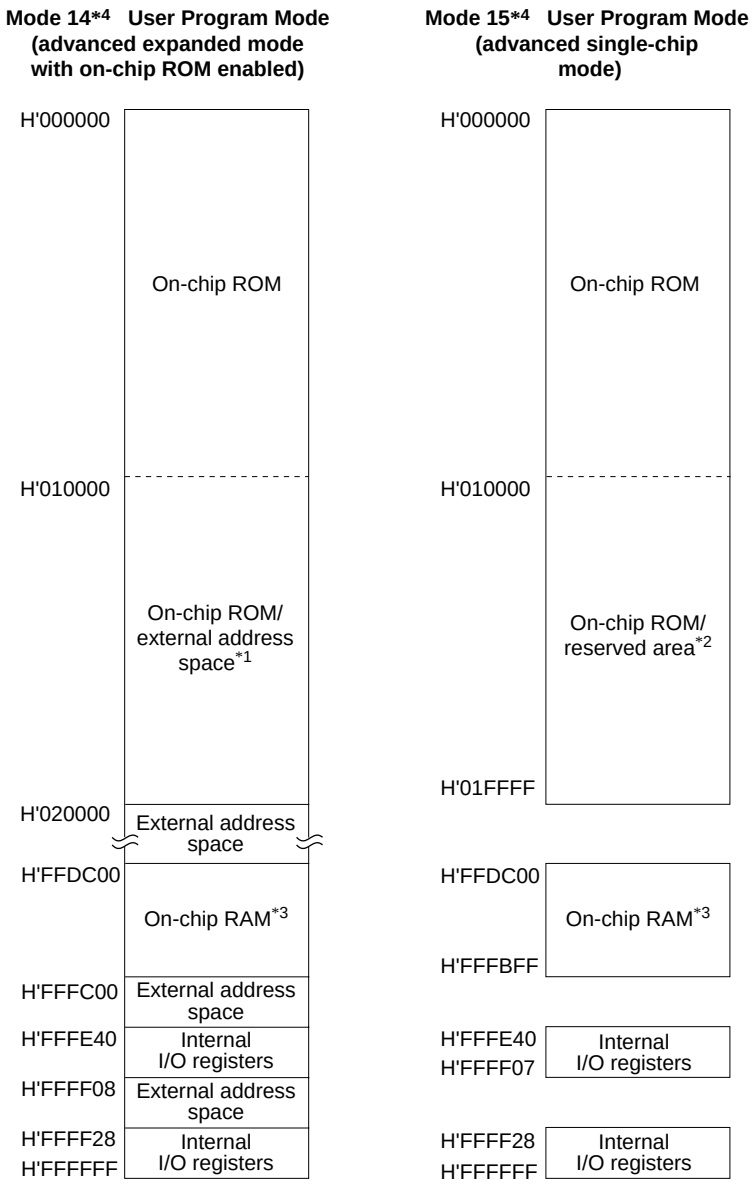


Figure 1-5 H8S/2398, H8S/2394, H8S/2392, H8S/2390 Pin Arrangement (FP-128B: Top View)

Table 2-3 Instructions Classified by Function

Type	Instruction	Size*[1]	Function
Data transfer	MOV	B/W/L	(EAs) → Rd, Rs → (Ead) Moves data between two general registers or between a general register and memory, or moves immediate data to a general register.
	MOVFPE	B	Cannot be used in the H8S/2357 Group.
	MOVTPE	B	Cannot be used in the H8S/2357 Group.
	POP	W/L	@SP+ → Rn Pops a register from the stack. POP.W Rn is identical to MOV.W @SP+, Rn. POP.L ERn is identical to MOV.L @SP+, ERn.
	PUSH	W/L	Rn → @–SP Pushes a register onto the stack. PUSH.W Rn is identical to MOV.W Rn, @–SP. PUSH.L ERn is identical to MOV.L ERn, @–SP.
	LDM	L	@SP+ → Rn (register list) Pops two or more general registers from the stack.
	STM	L	Rn (register list) → @–SP Pushes two or more general registers onto the stack.
Arithmetic operations	ADD SUB	B/W/L	Rd ± Rs → Rd, Rd ± #IMM → Rd Performs addition or subtraction on data in two general registers, or on immediate data and data in a general register. (Immediate byte data cannot be subtracted from byte data in a general register. Use the SUBX or ADD instruction.)
	ADDX SUBX	B	Rd ± Rs ± C → Rd, Rd ± #IMM ± C → Rd Performs addition or subtraction with carry or borrow on byte data in two general registers, or on immediate data and data in a general register.
	INC DEC	B/W/L	Rd ± 1 → Rd, Rd ± 2 → Rd Increments or decrements a general register by 1 or 2. (Byte operands can be incremented or decremented by 1 only.)
	ADDS SUBS	L	Rd ± 1 → Rd, Rd ± 2 → Rd, Rd ± 4 → Rd Adds or subtracts the value 1, 2, or 4 to or from data in a 32-bit register.
	DAA DAS	B	Rd decimal adjust → Rd Decimal-adjusts an addition or subtraction result in a general register by referring to the CCR to produce 4-bit BCD data.
	MULXU	B/W	Rd × Rs → Rd Performs unsigned multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
	MULXS	B/W	Rd × Rs → Rd Performs signed multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.



Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. On-chip RAM is used for flash memory programming. Do not clear the RAME bit to 0 in SYSCR.
4. Modes 14 and 15 are provided in the F-ZTAT version only.

Figure 3-1 Memory Map in Each Operating Mode (H8S/2357, H8S/2352) (3)

4.2.4 Interrupts after Reset

If an interrupt is accepted after a reset but before the stack pointer (SP) is initialized, the PC and CCR will not be saved correctly, leading to a program crash. To prevent this, all interrupt requests, including NMI, are disabled immediately after a reset. Since the first instruction of a program is always executed immediately after the reset state ends, make sure that this instruction initializes the stack pointer (example: MOV.L #xx:32, SP).

4.2.5 State of On-Chip Supporting Modules after Reset Release

After reset release, MSTPCR is initialized to H'3FFF and all modules except the DMAC and DTC enter module stop mode. Consequently, on-chip supporting module registers cannot be read or written to. Register reading and writing is enabled when module stop mode is exited.

4.3 Traces

Traces are enabled in interrupt control mode 2. Trace mode is not activated in interrupt control mode 0, irrespective of the state of the T bit. For details of interrupt control modes, see section 5, Interrupt Controller.

If the T bit in EXR is set to 1, trace mode is activated. In trace mode, a trace exception occurs on completion of each instruction.

Trace mode is canceled by clearing the T bit in EXR to 0. It is not affected by interrupt masking.

Table 4-4 shows the state of CCR and EXR after execution of trace exception handling.

Interrupts are accepted even within the trace exception handling routine.

The T bit saved on the stack retains its value of 1, and when control is returned from the trace exception handling routine by the RTE instruction, trace mode resumes.

Trace exception handling is not carried out after execution of the RTE instruction.

Table 4-4 Status of CCR and EXR after Trace Exception Handling

	CCR		EXR	
Interrupt Control Mode	**I**	**UI**	**I2 to I0**	**T**
0	Trace exception handling cannot be used.			
2	1	—	—	0

Legend:

1: Set to 1

0: Cleared to 0

—: Retains value prior to execution.

6.2 Register Descriptions

6.2.1 Bus Width Control Register (ABWCR)

Bit	:	7	6	5	4	3	2	1	0
		ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0
Modes 5 to 7									
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Mode 4									
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ABWCR is an 8-bit readable/writable register that designates each area for either 8-bit access or 16-bit access.

ABWCR sets the data bus width for the external memory space. The bus width for on-chip memory and internal I/O registers is fixed regardless of the settings in ABWCR.

After a power-on reset and in hardware standby mode, ABWCR is initialized to H'FF in modes 5 to 7,*[1] and to H'00 in mode 4. It is not initialized by a manual reset*[2] or in software standby mode.

Notes: 1. In ROMless version, modes 6 and 7 are not available.
2. Manual reset is only supported in the H8S/2357 ZTAT.

Bits 7 to 0—Area 7 to 0 Bus Width Control (ABW7 to ABW0): These bits select whether the corresponding area is to be designated for 8-bit access or 16-bit access.

Bit n ABWn	Description
0	Area n is designated for 16-bit access
1	Area n is designated for 8-bit access

(n = 7 to 0)

Table 9-1 Port Functions

Port	Description	Pins	Mode 4*[3]	Mode 5*[3]	Mode 6	Mode 7
Port 1	• 8-bit I/O port	$P1_7$/PO15/TIOCB2/TCLKD $P1_6$/PO14/TIOCA2 $P1_5$/PO13/TIOCB1/TCLKC $P1_4$/PO12/TIOCA1 $P1_3$/PO11/TIOCD0/TCLKB $P1_2$/PO10/TIOCC0/TCLKA $P1_1$/PO9/TIOCB0/$\overline{\text{DACK1}}$ $P1_0$/PO8/TIOCA0/$\overline{\text{DACK0}}$	8-bit I/O port also functioning as DMA controller output pins ($\overline{\text{DACK0}}$ and $\overline{\text{DACK1}}$), TPU I/O pins (TCLKA, TCLKB, TCLKC, TCLKD, TIOCA0, TIOCB0, TIOCC0, TIOCD0, TIOCA1, TIOCB1, TIOCA2, TIOCB2) and PPG output pins (PO15 to PO8)			
Port 2	• 8-bit I/O port • Schmitt-triggered input	$P2_7$/PO7/TIOCB5/TMO1 $P2_6$/PO6/TIOCA5/TMO0 $P2_5$/PO5/TIOCB4/TMCI1 $P2_4$/PO4/TIOCA4/TMRI1 $P2_3$/PO3/TIOCD3/TMCI0 $P2_2$/PO2/TIOCC3/TMRI0 $P2_1$/PO1/TIOCB3 $P2_0$/PO0/TIOCA3	8-bit I/O port also functioning as TPU I/O pins (TIOCA3, TIOCB3, TIOCC3, TIOCD3, TIOCA4, TIOCB4, TIOCA5, TIOCB5), 8-bit timer (channels 0 and 1) I/O pins (TMRI0, TMCI0, TMO0, TMRI1, TMCI1, TMO1) and PPG output pins (PO7 to PO0)			
Port 3	• 6-bit I/O port • Open-drain output capability	$P3_5$/SCK1 $P3_4$/SCK0 $P3_3$/RxD1 $P3_2$/RxD0 $P3_1$/TxD1 $P3_0$/TxD0	6-bit I/O port also functioning as SCI (channels 0 and 1) I/O pins (TxD0, RxD0, SCK0, TxD1, RxD1, SCK1)			
Port 4	• 8-bit input port	$P4_7$/AN7/DA1 $P4_6$/AN6/DA0 $P4_5$/AN5 $P4_4$/AN4 $P4_3$/AN3 $P4_2$/AN2 $P4_1$/AN1 $P4_0$/AN0	8-bit input port also functioning as A/D converter analog inputs (AN7 to AN0) and D/A converter analog outputs (DA1 and DA0)			
Port 5	• 4-bit I/O port	$P5_3$/$\overline{\text{ADTRG}}$ $P5_2$/SCK2 $P5_1$/RxD2 $P5_0$/TxD2	4-bit I/O port also functioning as SCI (channel 2) I/O pins (TxD2, RxD2, SCK2) and A/D converter input pin ($\overline{\text{ADTRG}}$)			
Port 6	• 8-bit I/O port • Schmitt-triggered input ($P6_4$ to $P6_7$)	$P6_7$/$\overline{\text{IRQ3}}$/$\overline{\text{CS7}}$ $P6_6$/$\overline{\text{IRQ2}}$/$\overline{\text{CS6}}$ $P6_5$/$\overline{\text{IRQ1}}$ $P6_4$/$\overline{\text{IRQ0}}$ $P6_3$/$\overline{\text{TEND1}}$ $P6_2$/$\overline{\text{DREQ1}}$ $P6_1$/$\overline{\text{TEND0}}$/$\overline{\text{CS5}}$ $P6_0$/$\overline{\text{DREQ0}}$/$\overline{\text{CS4}}$	8-bit I/O port also functioning as DMA controller I/O pins ($\overline{\text{DREQ0}}$, $\overline{\text{TEND0}}$, $\overline{\text{DREQ1}}$, $\overline{\text{TEND1}}$), bus control output pins ($\overline{\text{CS4}}$ to $\overline{\text{CS7}}$), and interrupt input pins ($\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$)			8-bit I/O port also functioning as interrupt input pins ($\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$)

9.3.3 Pin Functions

Port 2 pins also function as PPG output pins (PO7 to PO0) and TPU I/O pins (TIOCA3, TIOCB3, TIOCC3, TIOCD3, TIOCA4, TIOCB4, TIOCA5, and TIOCB5), and 8-bit timer I/O pins (TMRI0, TMCI0, TMO0, TMRI1, TMCI1, and TMO1). Port 2 pin functions are shown in table 9-5.

Table 9-5 Port 2 Pin Functions

<table>
<tr><th>Pin</th><th>Selection Method and Pin Functions</th></tr>
<tr><td>$P2_7$/PO7/TIOCB5/
TMO1</td><td>The pin function is switched as shown below according to the combination of the TPU channel 5 setting by bits MD3 to MD0 in TMDR5, bits IOB3 to IOB0 in TIOR5, bits CCLR1 and CCLR0 in TCR5, bit NDER7 in NDERL, bits OS3 to OS0 in TCSR1, and bit P27DDR.
<table>
<tr><td>OS3 to OS0</td><td colspan="4">All 0</td><td>Any 1</td></tr>
<tr><td>TPU Channel 5 Setting</td><td>Table Below (1)</td><td colspan="3">Table Below (2)</td><td>—</td></tr>
<tr><td>P27DDR</td><td>—</td><td>0</td><td>1</td><td>1</td><td>—</td></tr>
<tr><td>NDER7</td><td>—</td><td>—</td><td>0</td><td>1</td><td>—</td></tr>
<tr><td rowspan="2">Pin function</td><td rowspan="2">TIOCB5 output</td><td>$P2_7$ input</td><td>$P2_7$ output</td><td>PO7 output</td><td>TMO1 output</td></tr>
<tr><td colspan="4">TIOCB5 input *</td></tr>
</table>
Note: * TIOCB5 input when MD3 to MD0 = B'0000, B'01××, and IOB3 = 1.
<table>
<tr><td>TPU Channel 5 Setting</td><td>(2)</td><td>(1)</td><td>(2)</td><td>(2)</td><td>(1)</td><td>(2)</td></tr>
<tr><td>MD3 to MD0</td><td colspan="2">B'0000, B'01××</td><td>B'0010</td><td colspan="3">B'0011</td></tr>
<tr><td>IOB3 to IOB0</td><td>B'0000
B'0100
B'1×××</td><td>B'0001 to B'0011
B'0101 to B'0111</td><td>—</td><td>B'××00</td><td colspan="2">Other than B'××00</td></tr>
<tr><td>CCLR1, CCLR0</td><td>—</td><td>—</td><td>—</td><td>—</td><td>Other than B'10</td><td>B'10</td></tr>
<tr><td>Output function</td><td>—</td><td>Output compare output</td><td>—</td><td>—</td><td>PWM mode 2 output</td><td>—</td></tr>
</table>
×: Don't care</td></tr>
</table>

Pin	Selection Method and Pin Functions
$P2_1$/PO1/TIOCB3	The pin function is switched as shown below according to the combination of the TPU channel 3 setting by bits MD3 to MD0 in TMDR3, bits IOB3 to IOB0 in TIOR3H, bits CCLR2 to CCLR0 in TCR3, bit NDER1 in NDERL, and bit P21DDR.

TPU Channel 3 Setting	Table Below (1)	Table Below (2)		
P21DDR	—	0	1	1
NDER1	—	—	0	1
Pin function	TIOCB3 output	$P2_1$ input	$P2_1$ output	PO1 output
		TIOCB3 input *		

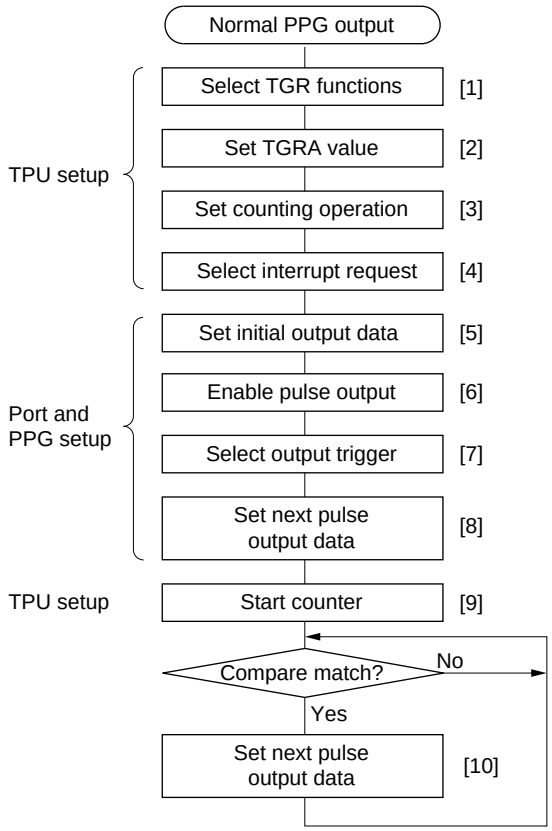
Note: * TIOCB3 input when MD3 to MD0 = B'0000, and IOB3 to IOB0 = B'10××.

TPU Channel 3 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1×××	B'0001 to B'0011 B'0101 to B'0111	—	B'××00	Other than B'××00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

×: Don't care

11.3.3 Normal Pulse Output

Sample Setup Procedure for Normal Pulse Output: Figure 11-4 shows a sample procedure for setting up normal pulse output.



[1] Set TIOR to make TGRA an output compare register (with output disabled)

[2] Set the PPG output trigger period

[3] Select the counter clock source with bits TPSC2 to TPSC0 in TCR. Select the counter clear source with bits CCLR1 and CCLR0.

[4] Enable the TGIA interrupt in TIER. The DTC or DMAC can also be set up to transfer data to NDR.

[5] Set the initial output values in PODR.

[6] Set the DDR and NDER bits for the pins to be used for pulse output to 1.

[7] Select the TPU compare match event to be used as the output trigger in PCR.

[8] Set the next pulse output values in NDR.

[9] Set the CST bit in TSTR to 1 to start the TCNT counter.

[10] At each TGIA interrupt, set the next output values in NDR.

Figure 11-4 Setup Procedure for Normal Pulse Output (Example)

14.2.4 Transmit Data Register (TDR)

Bit	:	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TDR is an 8-bit register that stores data for serial transmission.

When the SCI detects that TSR is empty, it transfers the transmit data written in TDR to TSR and starts serial transmission. Continuous serial transmission can be carried out by writing the next transmit data to TDR during serial transmission of the data in TSR.

TDR can be read or written to by the CPU at all times.

TDR is initialized to H'FF by a reset, and in standby mode or module stop mode.

14.2.5 Serial Mode Register (SMR)

Bit	:	7	6	5	4	3	2	1	0
		C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SMR is an 8-bit register used to set the SCI's serial transfer format and select the baud rate generator clock source.

SMR can be read or written to by the CPU at all times.

SMR is initialized to H'00 by a reset, and by putting the device in standby mode or module stop mode. In the H8S/2398, H8S/2394, H8S/2392, and H8S/2390, however, the value in SMR is initialized to H'00 by a reset, or in hardware standby mode, but SMR retains its current state when the device enters software standby mode or module stop mode.

Bit 7—Communication Mode (C/$\overline{A}$): Selects asynchronous mode or clocked synchronous mode as the SCI operating mode.

Bit 7 C/$\overline{A}$	Description	
0	Asynchronous mode	(Initial value)
1	Clocked synchronous mode	

Bit 6—Character Length (CHR): Selects 7 or 8 bits as the data length in asynchronous mode. In clocked synchronous mode, a fixed data length of 8 bits is used regardless of the CHR setting.

Bit 6 CHR	Description	
0	8-bit data	(Initial value)
1	7-bit data*	

Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted, and it is not possible to choose between LSB-first or MSB-first transfer.

Bit 0—Multiprocessor Bit Transfer (MPBT): When transmission is performed using multiprocessor format in asynchronous mode, MPBT stores the multiprocessor bit to be added to the transmit data.

The MPBT bit setting is invalid when multiprocessor format is not used, when not transmitting, and in clocked synchronous mode.

Bit 0 MPBT	Description	
0	Data with a 0 multiprocessor bit is transmitted	(Initial value)
1	Data with a 1 multiprocessor bit is transmitted	

14.2.8 Bit Rate Register (BRR)

Bit	:	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BRR is an 8-bit register that sets the serial transfer bit rate in accordance with the baud rate generator operating clock selected by bits CKS1 and CKS0 in SMR.

BRR can be read or written to by the CPU at all times.

BRR is initialized to H'FF by a reset, and by putting the device in standby mode or module stop mode. In the H8S/2398, H8S/2394, H8S/2392, and H8S/2390, however, the value in BRR is initialized to H'FF by a reset, or in hardware standby mode, but BRR retains its current state when the device enters software standby mode or module stop mode.

As baud rate generator control is performed independently for each channel, different values can be set for each channel.

Table 14-3 shows sample BRR settings in asynchronous mode, and table 14-4 shows sample BRR settings in clocked synchronous mode.

Table 14-3 BRR Settings for Various Bit Rates (Asynchronous Mode)

	ø = 2 MHz			ø = 2.097152 MHz			ø = 2.4576 MHz			ø = 3 MHz		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	1	141	0.03	1	148	–0.04	1	174	–0.26	1	212	0.03
150	1	103	0.16	1	108	0.21	1	127	0.00	1	155	0.16
300	0	207	0.16	0	217	0.21	0	255	0.00	1	77	0.16
600	0	103	0.16	0	108	0.21	0	127	0.00	0	155	0.16
1200	0	51	0.16	0	54	–0.70	0	63	0.00	0	77	0.16
2400	0	25	0.16	0	26	1.14	0	31	0.00	0	38	0.16
4800	0	12	0.16	0	13	–2.48	0	15	0.00	0	19	–2.34
9600	0	6	—	0	6	–2.48	0	7	0.00	0	9	–2.34
19200	0	2	—	0	2	—	0	3	0.00	0	4	–2.34
31250	0	1	0.00	0	1	—	0	1	—	0	2	0.00
38400	0	1	—	0	1	—	0	1	0.00	—	—	—

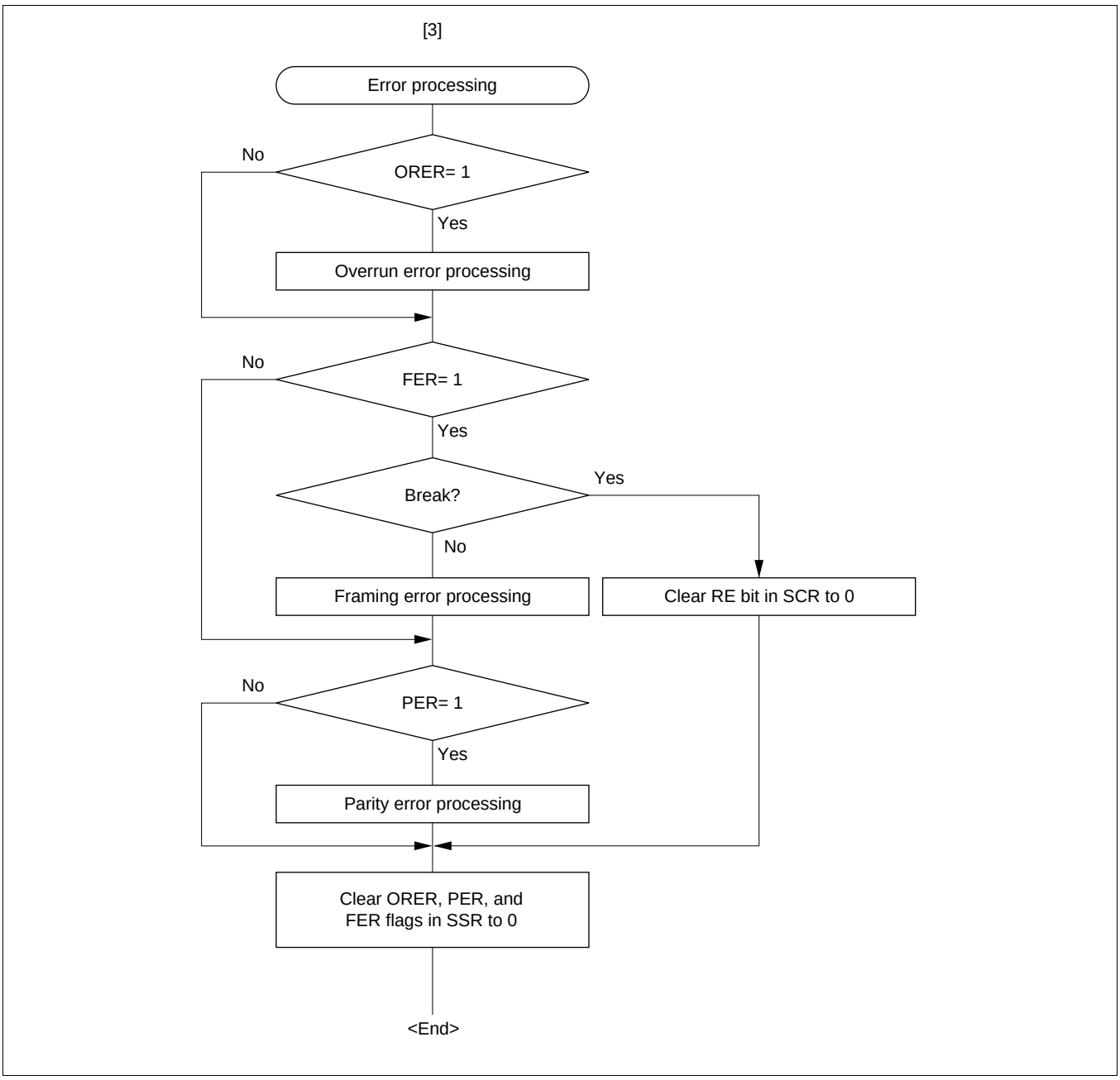
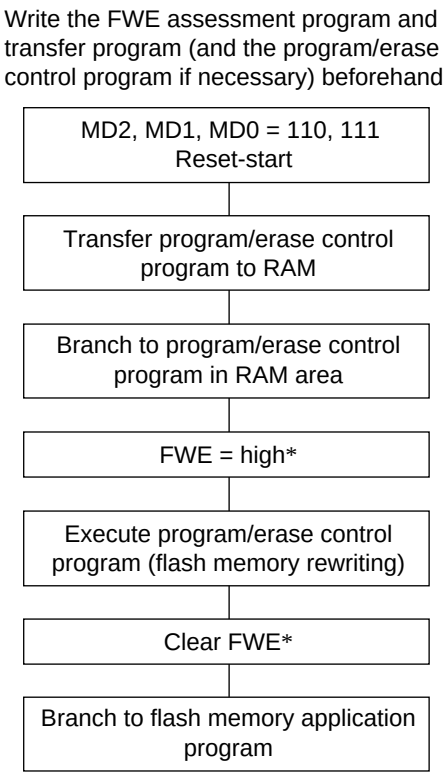


Figure 14-7 Sample Serial Reception Data Flowchart (cont)



Notes: Do not apply a constant high level to the FWE pin. Apply a high level to the FWE pin only when the flash memory is programmed or erased. Also, while a high level is applied to the FWE pin, the watchdog timer should be activated to prevent overprogramming or overerasing due to program runaway, etc.

* For further information on FWE application and disconnection, see section 19.14, Flash Memory Programming and Erasing Precautions.

Figure 19-18 User Program Mode Execution Procedure

19.9 Programming/Erasing Flash Memory

In the on-board programming modes, flash memory programming and erasing is performed by software, using the CPU. There are four flash memory operating modes: program mode, erase mode, program-verify mode, and erase-verify mode. Transitions to these modes can be made by setting the PSU and ESU bits in FLMCR2, and the P, E, PV, and EV bits in FLMCR1.

The flash memory cannot be read while being programmed or erased. Therefore, the program that controls flash memory programming/erasing (the programming control program) should be located and executed in on-chip RAM or external memory.

Notes: 1. Operation is not guaranteed if setting/resetting of the SWE, EV, PV, E, and P bits in FLMCR1, and the ESU and PSU bits in FLMCR2, is executed by a program in flash memory.
2. When programming or erasing, set FWE to 1 (programming/erasing will not be executed if FWE = 0).
3. Perform programming in the erased state. Do not perform additional programming on previously programmed addresses.

19.9.1 Program Mode

Follow the procedure shown in the program/program-verify flowchart in figure 19-19 to write data or programs to flash memory. Performing program operations according to this flowchart will enable data or programs to be written to flash memory without subjecting the device to voltage stress or sacrificing program data reliability. Programming should be carried out 32 bytes at a time.

The wait times (x, y, z, α, ß, γ, ε, η) after bits are set or cleared in flash memory control registers 1 and 2 (FLMCR1, FLMCR2) and the maximum number of programming operations (N) are shown in table 22.42 in section 22.7.6, Flash Memory Characteristics.

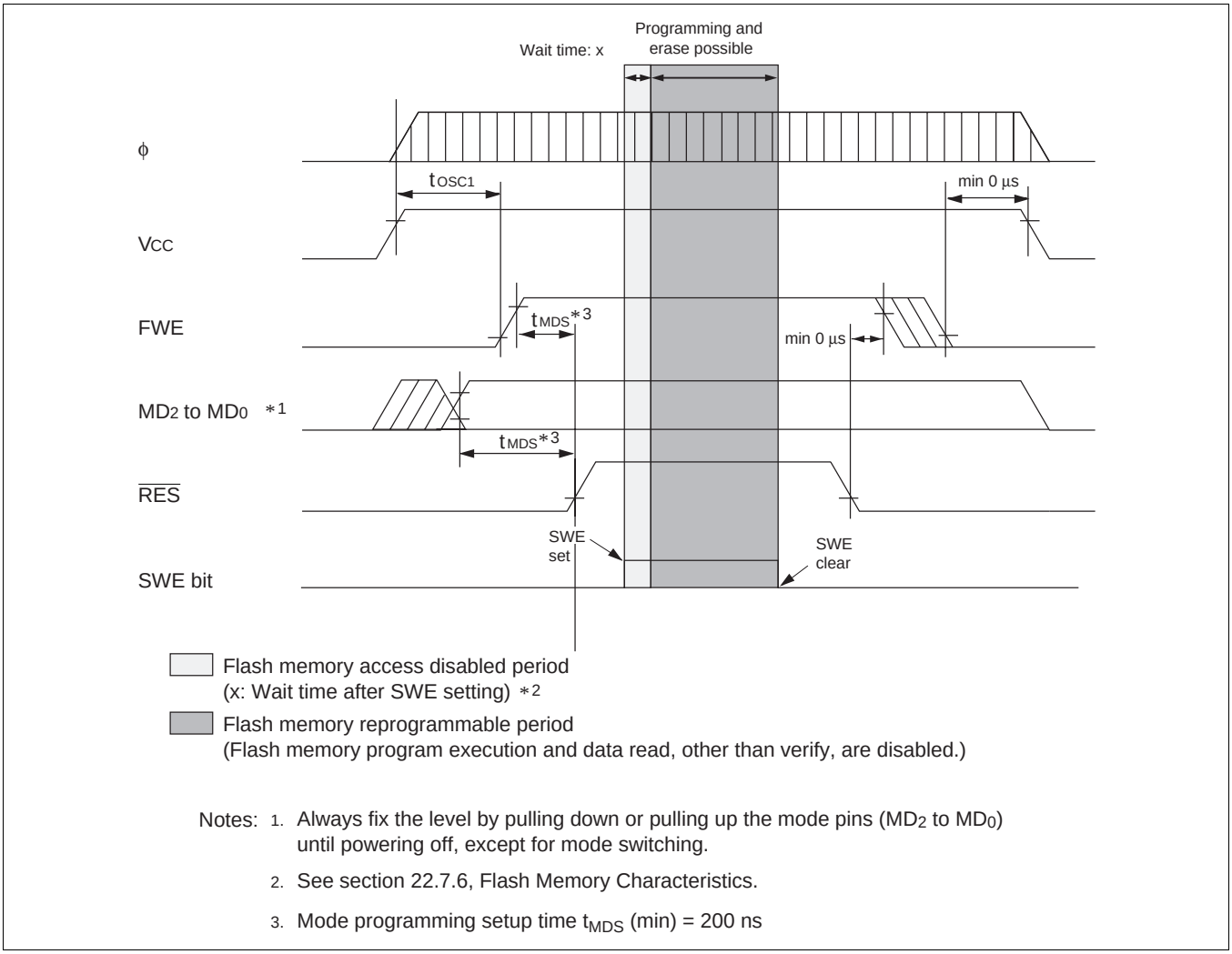
Following the elapse of (x) µs or more after the SWE bit is set to 1 in flash memory control register 1 (FLMCR1), 32-byte program data is stored in the program data area and reprogram data area, and the 32-byte data in the reprogram data area written consecutively to the write addresses. The lower 8 bits of the first address written to must be H'00, H'20, H'40, H'60, H'80, H'A0, H'C0, or H'E0. Thirty-two consecutive byte data transfers are performed. The program address and program data are latched in the flash memory. A 32-byte data transfer must be performed even if writing fewer than 32 bytes; in this case, H'FF data must be written to the extra addresses.

Next, the watchdog timer is set to prevent overprogramming in the event of program runaway, etc. Set a value greater than (y + z + α + ß) µs as the WDT overflow period. After this, preparation for program mode (program setup) is carried out by setting the PSU bit in FLMCR2, and after the elapse of (y) µs or more, the operating mode is switched to program mode by setting the P bit in FLMCR1. The time during which the P bit is set is the flash memory programming time. Make a program setting so that the time for one programming operation is within the range of (z) µs.

19.9.2 Program-Verify Mode

In program-verify mode, the data written in program mode is read to check whether it has been correctly written in the flash memory.

After the elapse of a given programming time, the programming mode is exited (the P bit in FLMCR1 is cleared to 0, then the PSU bit in FLMCR2 is cleared to 0 at least (α) µs later). Next, the watchdog timer is cleared after the elapse of (β) µs or more, and the operating mode is switched to program-verify mode by setting the PV bit in FLMCR1. Before reading in program-verify mode, a dummy write of H'FF data should be made to the addresses to be read. The dummy write should be executed after the elapse of (γ) µs or more. When the flash memory is read in this state (verify data is read in 16-bit units), the data at the latched address is read. Wait at least (ε) µs after the dummy write before performing this read operation. Next, the originally written data is compared with the verify data, and reprogram data is computed (see figure



Notes: 1. Always fix the level by pulling down or pulling up the mode pins (MD_2 to MD_0) until powering off, except for mode switching.

2. See section 22.7.6, Flash Memory Characteristics.

3. Mode programming setup time t_{MDS} (min) = 200 ns

Figure 19-33 Powering On/Off Timing (Boot Mode)

Section 22 Electrical Characteristics

22.1 Electrical Characteristics of Masked ROM Version (H8S/2398) and ROMless Versions (H8S/2394, H8S/2392, and H8S/2390)

22.1.1 Absolute Maximum Ratings

Table 22-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}*	–0.3 to +7.0	V
Input voltage (except port 4)	V_{in}	–0.3 to + V_{CC} +0.3	V
Input voltage (port 4)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Note: * Do not supply the power supply voltage to the V_{CL} pin. Doing so could permanently damage the LSI. Connect an external capacitor between the V_{CL} pin and the ground pin.

22.6.4 A/D Conversion Characteristics

Table 22-31 lists the A/D conversion characteristics.

Table 22-31 A/D Conversion Characteristics

Condition A: $V_{CC} = AV_{CC} = 2.7$ V to 5.5 V, $V_{ref} = 2.7$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V,
ø = 2 to 10 MHz, $T_a = –20$ to +75°C (regular specifications),
$T_a = –40$ to +85°C (wide-range specifications)

Condition B: $V_{CC} = AV_{CC} = 5.0$ V ± 10%, $V_{ref} = 4.5$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V,
ø = 2 to 20 MHz, $T_a = –20$ to +75°C (regular specifications),
$T_a = –40$ to +85°C (wide-range specifications)

Condition C: $V_{CC} = AV_{CC} = 3.0$ to 5.5 V, $V_{ref} = 3.0$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V,
ø = 2 to 13 MHz, $T_a = –20$ to +75°C (regular specifications),
$T_a = –40$ to +85°C (wide-range specifications)

	Condition A			Condition B			Condition C			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	10	10	10	bits
Conversion time	13.4	—	—	6.7	—	—	10.4	—	—	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*[1]	—	—	10*[3]	—	—	10*[1]	kΩ
	—	—	5*[2]	—	—	5*[4]	—	—	5*[5]	
Nonlinearity error	—	—	±7.5	—	—	±3.5	—	—	±7.5	LSB
Offset error	—	—	±7.5	—	—	±3.5	—	—	±7.5	LSB
Full-scale error	—	—	±7.5	—	—	±3.5	—	—	±7.5	LSB
Quantization	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±8.0	—	—	±4.0	—	—	±8.0	LSB

Notes: 1. $4.0 \text{ V} \le AV_{CC} \le 5.5$ V
2. $2.7 \text{ V} \le AV_{CC} < 4.0$ V
3. ø ≤ 12 MHz
4. ø > 12 MHz
5. $3.0 \text{ V} \le AV_{CC} < 4.0$ V

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)									Operation	Condition Code					No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa	|		I	H	N	Z	V	C	Advanced
JMP	JMP @ERn	—			2							PC←ERn	—	—	—	—	—	—	2
	JMP @aa:24	—						4				PC←aa:24	—	—	—	—	—	—	3
	JMP @@aa:8	—								2		PC←@aa:8	—	—	—	—	—	—	5
BSR	BSR d:8	—							2			PC→@-SP,PC←PC+d:8	—	—	—	—	—	—	4
	BSR d:16	—							4			PC→@-SP,PC←PC+d:16	—	—	—	—	—	—	5
JSR	JSR @ERn	—			2							PC→@-SP,PC←ERn	—	—	—	—	—	—	4
	JSR @aa:24	—						4				PC→@-SP,PC←aa:24	—	—	—	—	—	—	5
	JSR @@aa:8	—								2		PC→@-SP,PC←@aa:8	—	—	—	—	—	—	6
RTS	RTS	—									2	PC←@SP+	—	—	—	—	—	—	5

TGR4A—Timer General Register 4A **H'FE98** **TPU4**
TGR4B—Timer General Register 4B **H'FE9A** **TPU4**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCR5—Timer Control Register 5 **H'FEA0** **TPU5**

Bit	:	7	6	5	4	3	2	1	0
		—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	External clock: counts on TCLKC pin input
	1	0	Internal clock: counts on ø/256
		1	External clock: counts on TCLKD pin input

Note: This setting is ignored when channel 5 is in phase counting mode.

Clock Edge

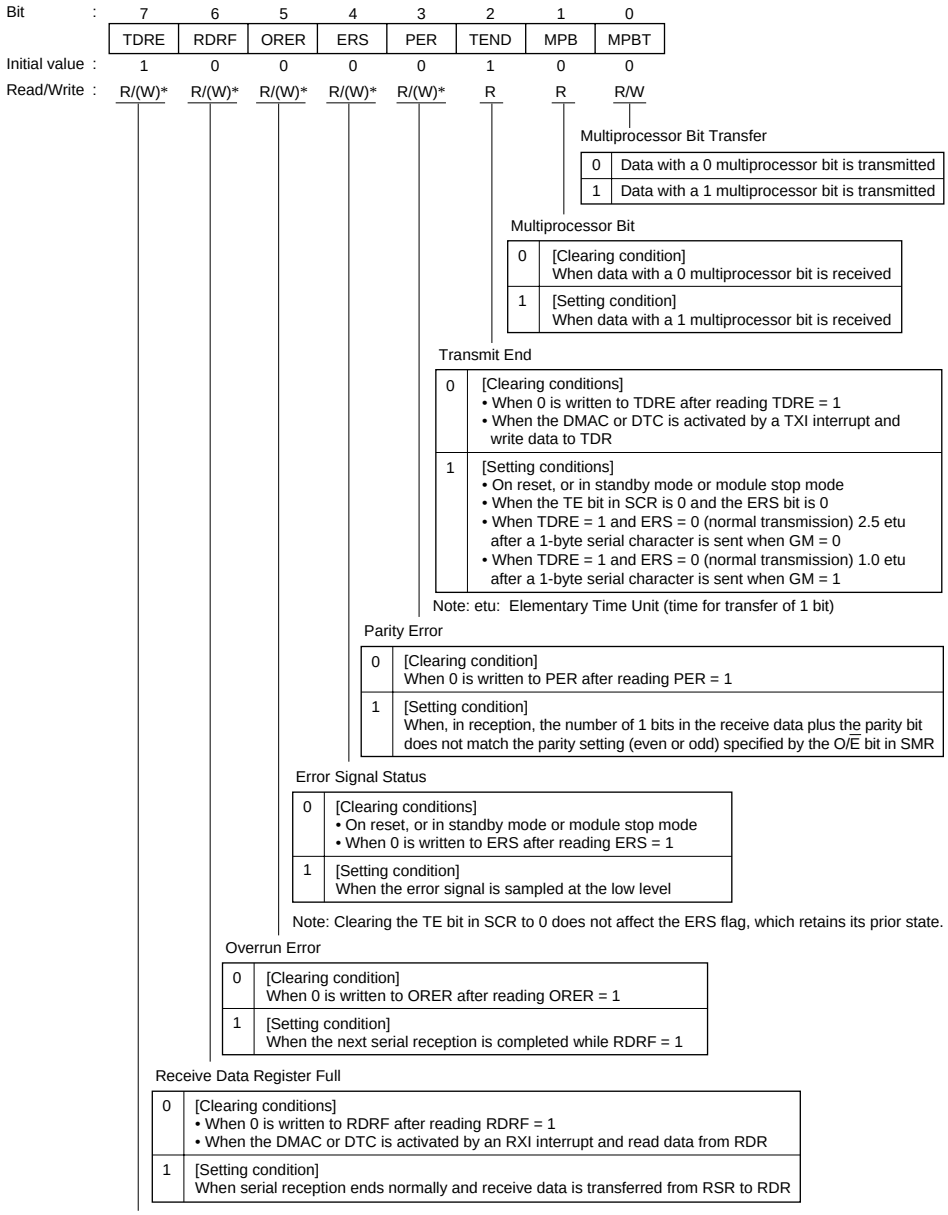
0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: This setting is ignored when channel 5 is in phase counting mode.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operating setting is performed by setting the SYNC bit TSYR to 1.



Note: * Can only be written with 0 for flag clearing.