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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	87
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2398f20v

(3) Hardware Standby Mode: A transition to hardware standby mode is made when the $\overline{\text{STBY}}$ pin goes low. In hardware standby mode, the CPU and clock halt and all MCU operations stop. The on-chip supporting modules are reset, but as long as a specified voltage is supplied, on-chip RAM contents are retained.

2.9 Basic Timing

2.9.1 Overview

The CPU is driven by a system clock, denoted by the symbol ø. The period from one rising edge of ø to the next is referred to as a "state." The memory cycle or bus cycle consists of one, two, or three states. Different methods are used to access on-chip memory, on-chip supporting modules, and the external address space.

2.9.2 On-Chip Memory (ROM, RAM)

On-chip memory is accessed in one state. The data bus is 16 bits wide, permitting both byte and word transfer instruction. Figure 2-14 shows the on-chip memory access cycle. Figure 2-15 shows the pin states.

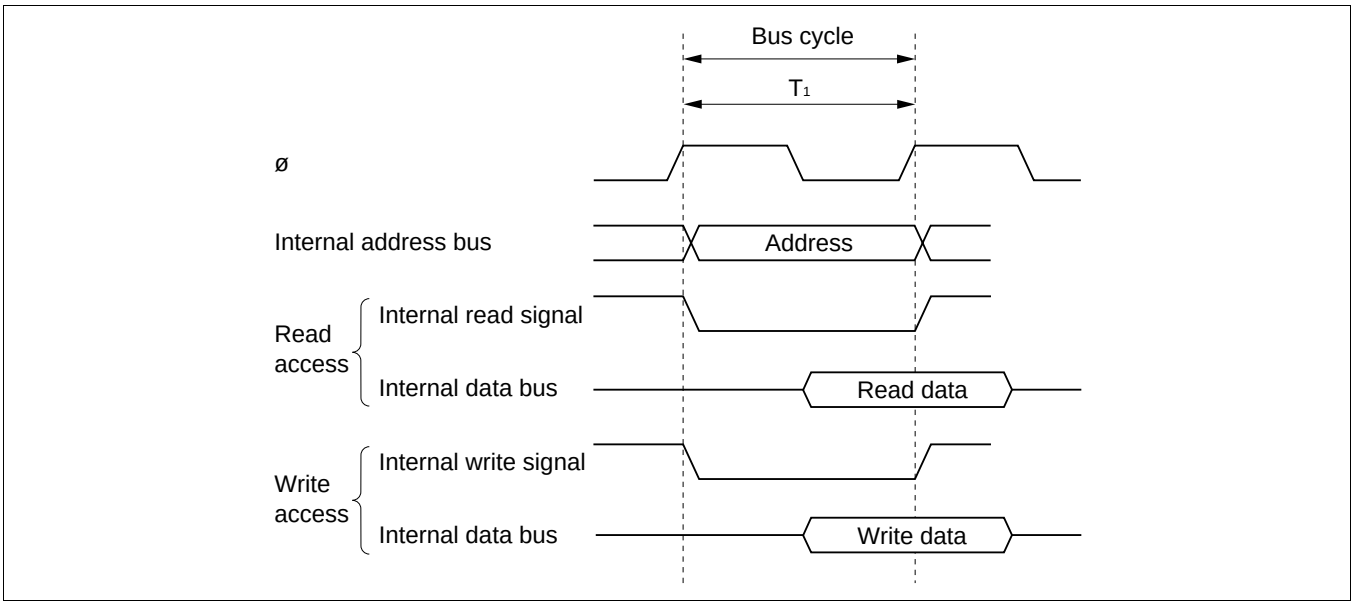


Figure 2-14 On-Chip Memory Access Cycle

5.5 Usage Notes

5.5.1 Contention between Interrupt Generation and Disabling

When an interrupt enable bit is cleared to 0 to disable interrupts, the disabling becomes effective after execution of the instruction.

In other words, when an interrupt enable bit is cleared to 0 by an instruction such as BCLR or MOV, if an interrupt is generated during execution of the instruction, the interrupt concerned will still be enabled on completion of the instruction, and so interrupt exception handling for that interrupt will be executed on completion of the instruction. However, if there is an interrupt request of higher priority than that interrupt, interrupt exception handling will be executed for the higher-priority interrupt, and the lower-priority interrupt will be ignored.

The same also applies when an interrupt source flag is cleared.

Figure 5-8 shows an example in which the TGIEA bit in the TPU's TIER0 register is cleared to 0.

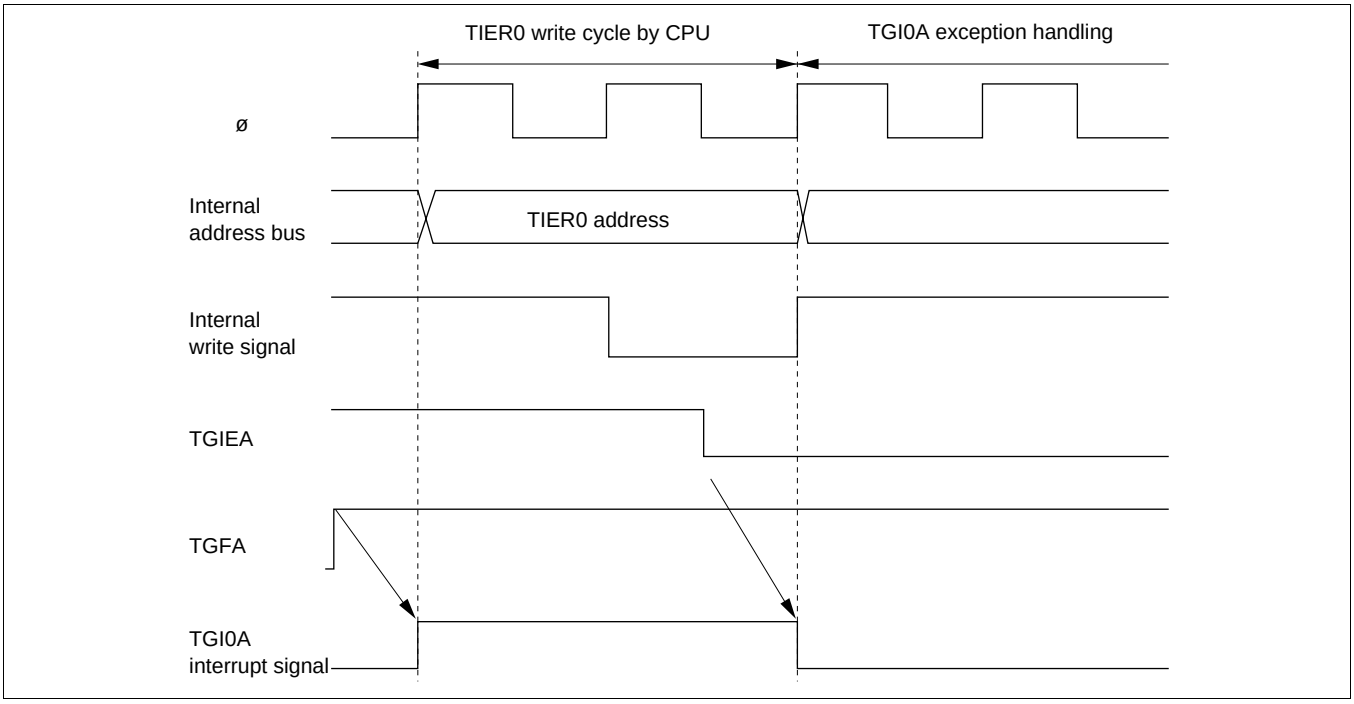


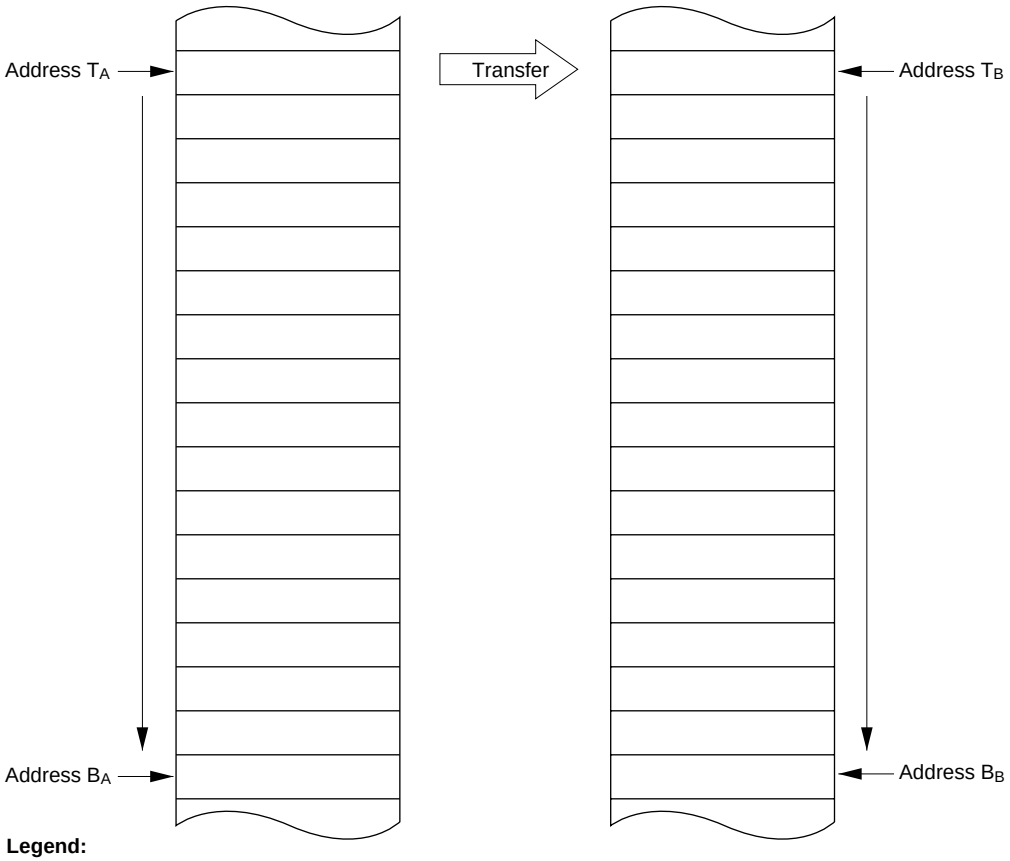
Figure 5-8 Contention between Interrupt Generation and Disabling

The above contention will not occur if an enable bit or interrupt source flag is cleared to 0 while the interrupt is masked.

5.5.2 Instructions that Disable Interrupts

Instructions that disable interrupts are LDC, ANDC, ORC, and XORC. After any of these instructions is executed, all interrupts including NMI are disabled and the next instruction is always executed. When the I bit is set by one of these instructions, the new value becomes valid two states after execution of the instruction ends.

Figure 7-11 illustrates operation in normal mode.



Legend:
Address $T_A = L_A$
Address $T_B = L_B$
Address $B_A = L_A + SAIDE \bullet (-1)^{SAID} \bullet (2^{DTSZ} \bullet (N-1))$
Address $B_B = L_B + DAIDE \bullet (-1)^{DAID} \bullet (2^{DTSZ} \bullet (N-1))$
Where : L_A = Value set in MARA
L_B = Value set in MARB
N = Value set in ETCRA

Figure 7-11 Operation in Normal Mode

Transfer requests (activation sources) are external requests and auto-requests.

With auto-request, the DMAC is only activated by register setting, and the specified number of transfers are performed automatically. With auto-request, cycle steal mode or burst mode can be selected. In cycle steal mode, the bus is released to another bus master each time a transfer is performed. In burst mode, the bus is held continuously until transfer ends.

Pin	Selection Method and Pin Functions
$P2_1$/PO1/TIOCB3	The pin function is switched as shown below according to the combination of the TPU channel 3 setting by bits MD3 to MD0 in TMDR3, bits IOB3 to IOB0 in TIOR3H, bits CCLR2 to CCLR0 in TCR3, bit NDER1 in NDERL, and bit P21DDR.

TPU Channel 3 Setting	Table Below (1)	Table Below (2)		
P21DDR	—	0	1	1
NDER1	—	—	0	1
Pin function	TIOCB3 output	$P2_1$ input	$P2_1$ output	PO1 output
		TIOCB3 input *		

Note: * TIOCB3 input when MD3 to MD0 = B'0000, and IOB3 to IOB0 = B'10××.

TPU Channel 3 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1×××	B'0001 to B'0011 B'0101 to B'0111	—	B'××00	Other than B'××00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

×: Don't care

Pin	Selection Method and Pin Functions
$P6_3$/$\overline{TEND1}$	The pin function is switched as shown below according to the combination of bit TEE1 in the DMAC DMATCR, and bit P63DDR.

TEE1	0		1
P63DDR	0	1	—
Pin function	$P6_3$ input pin	$P6_3$ output pin	$\overline{TEND1}$ output

$P6_2$/$\overline{DREQ1}$ The pin function is switched as shown below according to bit P62DDR.

P62DDR	0	1
Pin function	$P6_2$ input pin	$P6_2$ output pin
	$\overline{DERQ1}$ input	

$P6_1$/$\overline{TEND0}$/$\overline{CS5}$ The pin function is switched as shown below according to the combination of bit TEE0 in the DMAC DMATCR, and bit P61DDR.

Mode	Mode 7*			Modes 4 to 6*		
TEE0	0		1	0		1
P61DDR	0	1	—	0	1	—
Pin function	$P6_1$ input pin	$P6_1$ output pin	$\overline{TEND0}$ output	$P6_1$ input pin	$\overline{CS5}$ output pin	$\overline{TEND0}$ output

Note: * Modes 6 and 7 are provided in the on-chip ROM version only.

$P6_0$/$\overline{DREQ0}$/$\overline{CS4}$ The pin function is switched as shown below according to bit P60DDR.

Mode	Mode 7*		Modes 4 to 6*	
P60DDR	0	1	0	1
Pin function	$P6_0$ input pin	$P6_0$ output pin	$P6_0$ input pin	$\overline{CS4}$ output pin
	$\overline{DREQ0}$ input			

Note: * Modes 6 and 7 are provided in the on-chip ROM version only.

For details of PWM modes, see section 10.4.6, PWM Modes.

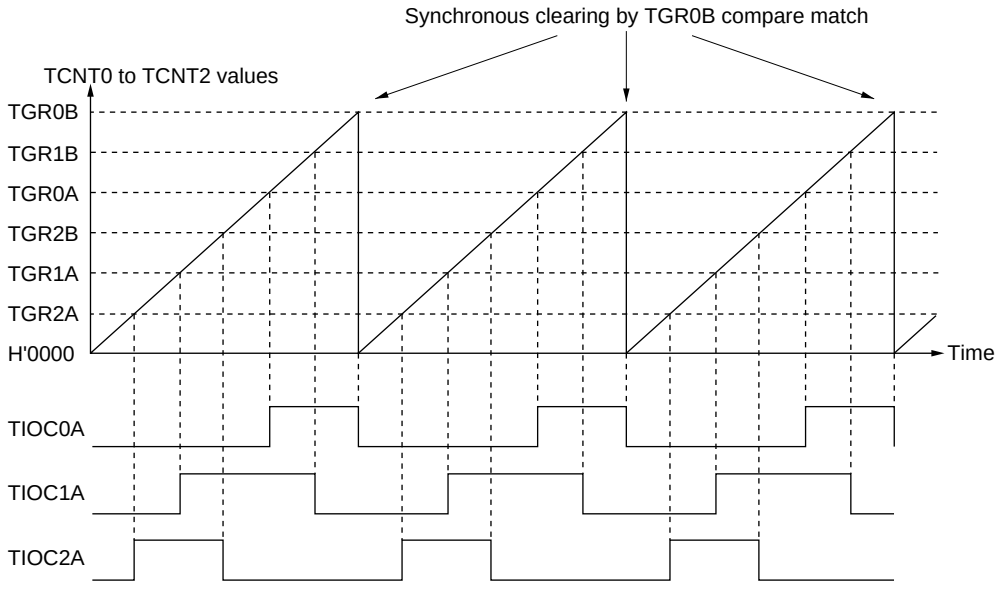


Figure 10-15 Example of Synchronous Operation

Status Flag Clearing Timing: After a status flag is read as 1 by the CPU, it is cleared by writing 0 to it. When the DTC or DMAC is activated, the flag is cleared automatically. Figure 10-46 shows the timing for status flag clearing by the CPU, and figure 10-47 shows the timing for status flag clearing by the DTC or DMAC.

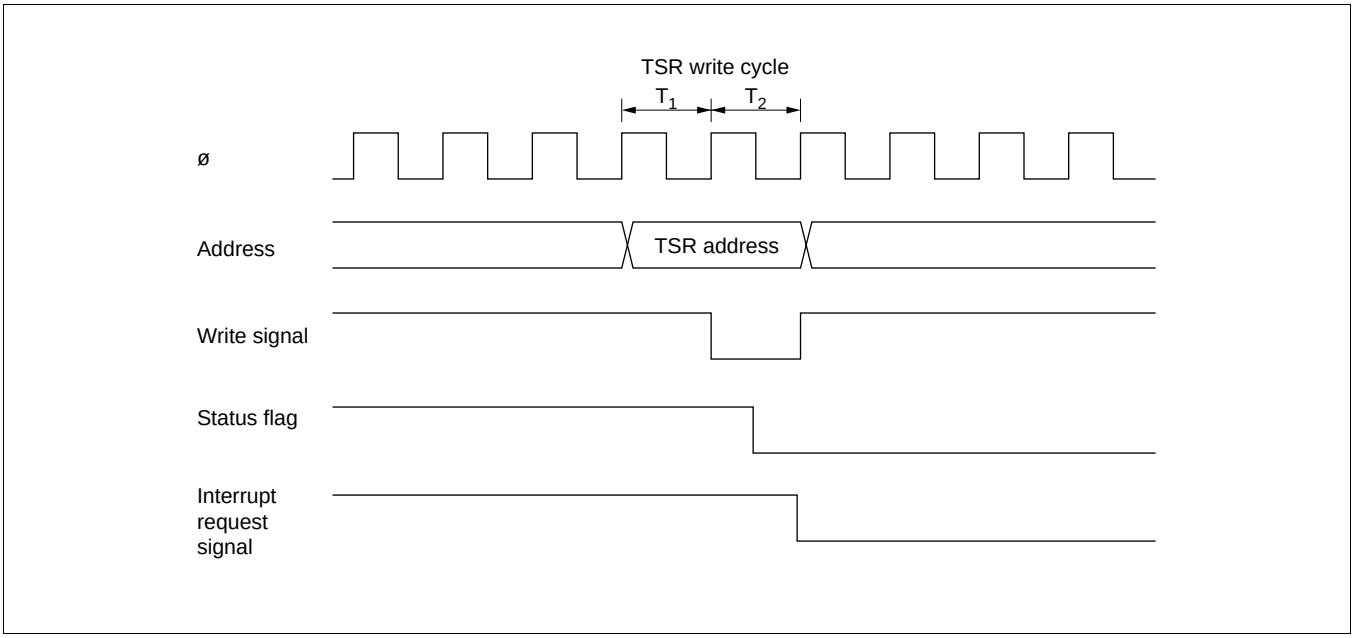


Figure 10-46 Timing for Status Flag Clearing by CPU

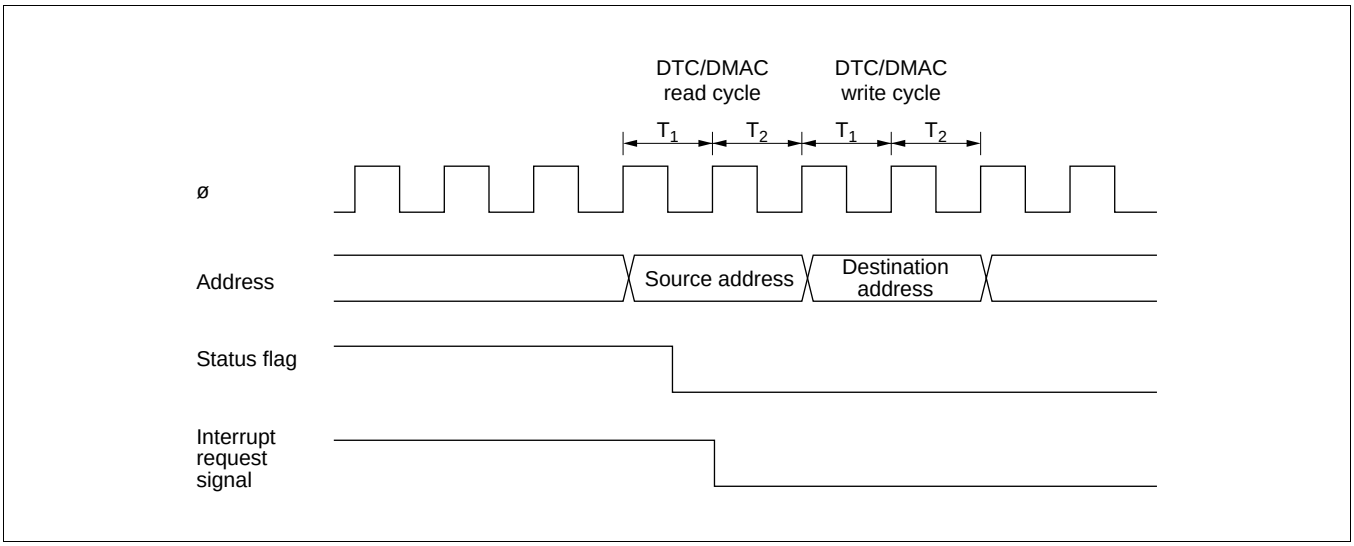


Figure 10-47 Timing for Status Flag Clearing by DTC/DMAC Activation

11.4 Usage Notes

Operation of Pulse Output Pins: Pins PO0 to PO15 are also used for other peripheral functions such as the TPU. When output by another peripheral function is enabled, the corresponding pins cannot be used for pulse output. Note, however, that data transfer from NDR bits to PODR bits takes place, regardless of the usage of the pins.

Pin functions should be changed only under conditions in which the output trigger event will not occur.

Note on Non-Overlapping Output: During non-overlapping operation, the transfer of NDR bit values to PODR bits takes place as follows.

- NDR bits are always transferred to PODR bits at compare match A.
- At compare match B, NDR bits are transferred only if their value is 0. Bits are not transferred if their value is 1.

Figure 11-10 illustrates the non-overlapping pulse output operation.

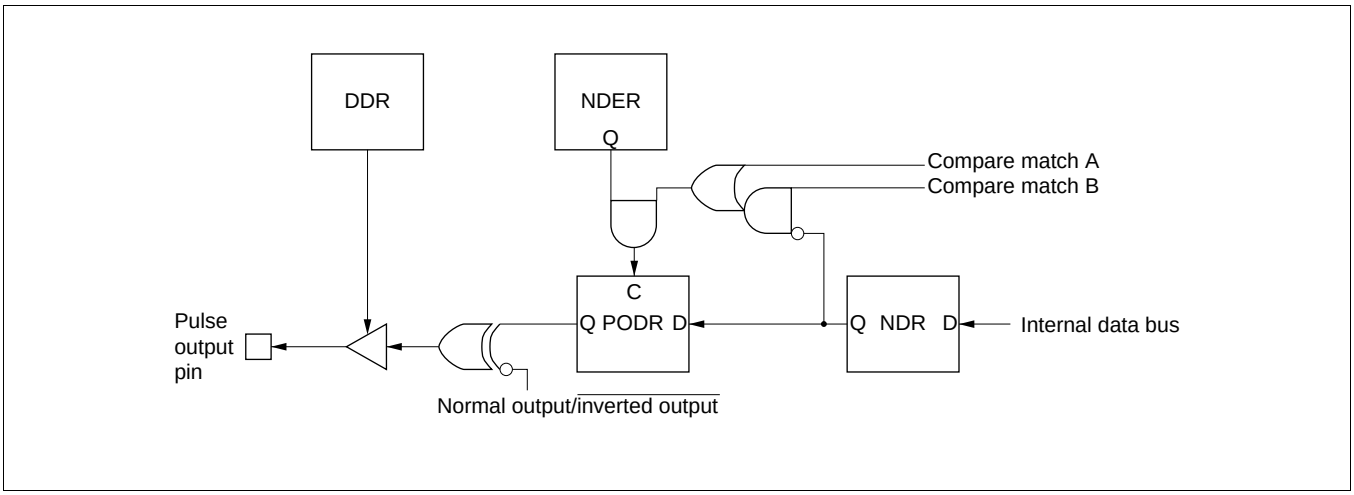


Figure 11-10 Non-Overlapping Pulse Output

12.2.6 Module Stop Control Register (MSTPCR)

	MSTPCRH								MSTPCRL							
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value :	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MSTPCR is a 16-bit readable/writable register that performs module stop mode control.

When the MSTP12 bit in MSTPCR is set to 1, the 8-bit timer operation stops at the end of the bus cycle and a transition is made to module stop mode. Registers cannot be read or written to in module stop mode. For details, see section 21.5, Module Stop Mode.

MSTPCR is initialized to H'3FFF by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 12—Module Stop (MSTP12): Specifies the 8-bit timer module stop mode.

Bit 12 MSTP12	Description	
0	8-bit timer module stop mode cleared	
1	8-bit timer module stop mode set	(Initial value)

12.5 Sample Application

In the example below, the 8-bit timer is used to generate a pulse output with a selected duty cycle, as shown in figure 12-9. The control bits are set as follows:

[1] In TCR, bit CCLR1 is cleared to 0 and bit CCLR0 is set to 1 so that the timer counter is cleared when its value matches the constant in TCORA.

[2] In TCSR, bits OS3 to OS0 are set to B'0110, causing the output to change to 1 at a TCORA compare match and to 0 at a TCORB compare match.

With these settings, the 8-bit timer provides output of pulses at a rate determined by TCORA with a pulse width determined by TCORB. No software intervention is required.

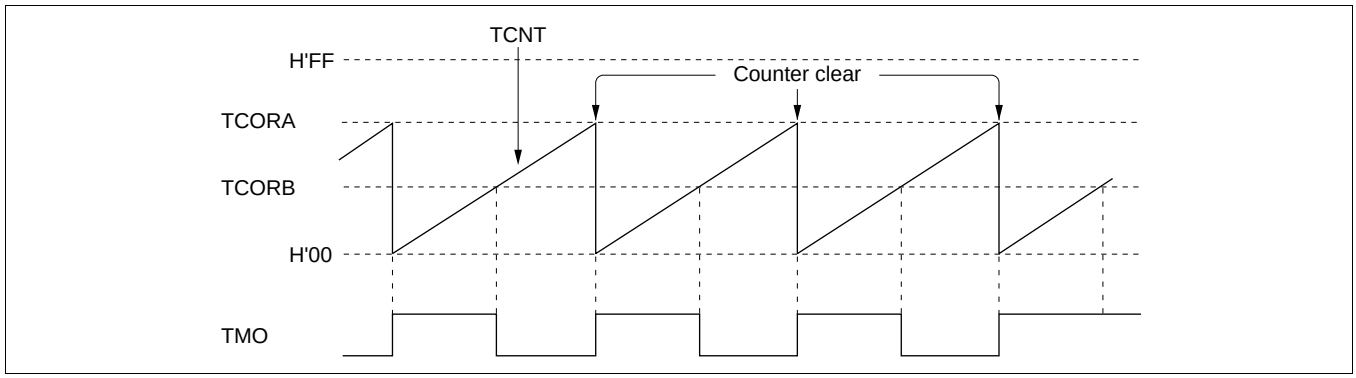


Figure 12-9 Example of Pulse Output

13.2.4 Notes on Register Access

The watchdog timer's TCNT, TCSR, and RSTCSR registers differ from other registers in being more difficult to write to. The procedures for writing to and reading these registers are given below.

Writing to TCNT and TCSR: These registers must be written to by a word transfer instruction. They cannot be written to with byte instructions.

Figure 13-2 shows the format of data written to TCNT and TCSR. TCNT and TCSR both have the same write address. For a write to TCNT, the upper byte of the written word must contain H'5A and the lower byte must contain the write data. For a write to TCSR, the upper byte of the written word must contain H'A5 and the lower byte must contain the write data. This transfers the write data from the lower byte to TCNT or TCSR.

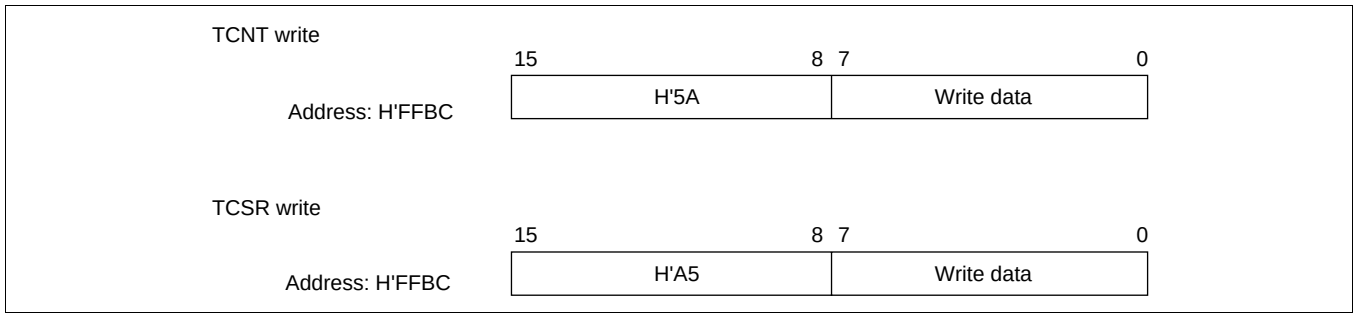


Figure 13-2 Format of Data Written to TCNT and TCSR

Writing to RSTCSR: RSTCSR must be written to by word transfer instruction to address H'FFBE. It cannot be written to with byte instructions.

Figure 13-3 shows the format of data written to RSTCSR. The method of writing 0 to the WOVF bit differs from that for writing to the RSTE and RSTS bits.

To write 0 to the WOVF bit, the write data must have H'A5 in the upper byte and H'00 in the lower byte. This clears the WOVF bit to 0, but has no effect on the RSTE and RSTS bits. To write to the RSTE and RSTS bits, the upper byte must contain H'5A and the lower byte must contain the write data. This writes the values in bits 6 and 5 of the lower byte into the RSTE and RSTS bits, but has no effect on the WOVF bit.

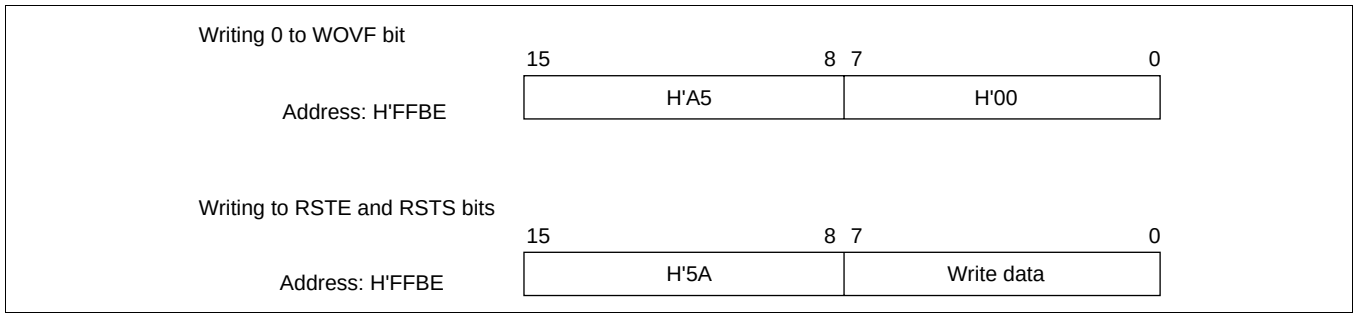


Figure 13-3 Format of Data Written to RSTCSR

Reading TCNT, TCSR, and RSTCSR: These registers are read in the same way as other registers. The read addresses are H'FFBC for TCSR, H'FFBD for TCNT, and H'FFBF for RSTCSR.

Bit 3—Parity Error (PER): Indicates that a parity error occurred during reception using parity addition in asynchronous mode, causing abnormal termination.

Bit 3 PER	Description	
0	[Clearing condition] When 0 is written to PER after reading PER = 1	(Initial value)*[1]
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR*[2]	

Notes: 1. The PER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
2. If a parity error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Also, subsequent serial reception cannot be continued while the PER flag is set to 1. In clocked synchronous mode, serial transmission cannot be continued, either.

Bit 2—Transmit End (TEND): Indicates that there is no valid data in TDR when the last bit of the transmit character is sent, and transmission has been ended.

The TEND flag is read-only and cannot be modified.

Bit 2 TEND	Description	
0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and write data to TDR	
1	[Setting conditions] • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character	(Initial value)

Bit 1—Multiprocessor Bit (MPB): When reception is performed using multiprocessor format in asynchronous mode, MPB stores the multiprocessor bit in the receive data.

MPB is a read-only bit, and cannot be modified.

Bit 1 MPB	Description	
0	[Clearing condition] When data with a 0 multiprocessor bit is received	(Initial value)*
1	[Setting condition] When data with a 1 multiprocessor bit is received	

Note: * Retains its previous state when the RE bit in SCR is cleared to 0 with multiprocessor format.

15.3 Operation

15.3.1 Overview

The main functions of the Smart Card interface are as follows.

- One frame consists of 8-bit data plus a parity bit.
- In transmission, a guard time of at least 2 etu (Elementary Time Unit: the time for transfer of 1 bit) is left between the end of the parity bit and the start of the next frame.
- If a parity error is detected during reception, a low error signal level is output for one etu period, 10.5 etu after the start bit.
- If the error signal is sampled during transmission, the same data is transmitted automatically after the elapse of 2 etu or longer.
- Only asynchronous communication is supported; there is no clocked synchronous communication function.

15.3.2 Pin Connections

Figure 15-2 shows a schematic diagram of Smart Card interface related pin connections.

In communication with an IC card, since both transmission and reception are carried out on a single data transmission line, the TxD pin and RxD pin should be connected with the LSI pin. The data transmission line should be pulled up to the V_{CC} power supply with a resistor.

When the clock generated on the Smart Card interface is used by an IC card, the SCK pin output is input to the CLK pin of the IC card. No connection is needed if the IC card uses an internal clock.

LSI port output is used as the reset signal.

Other pins must normally be connected to the power supply or ground.

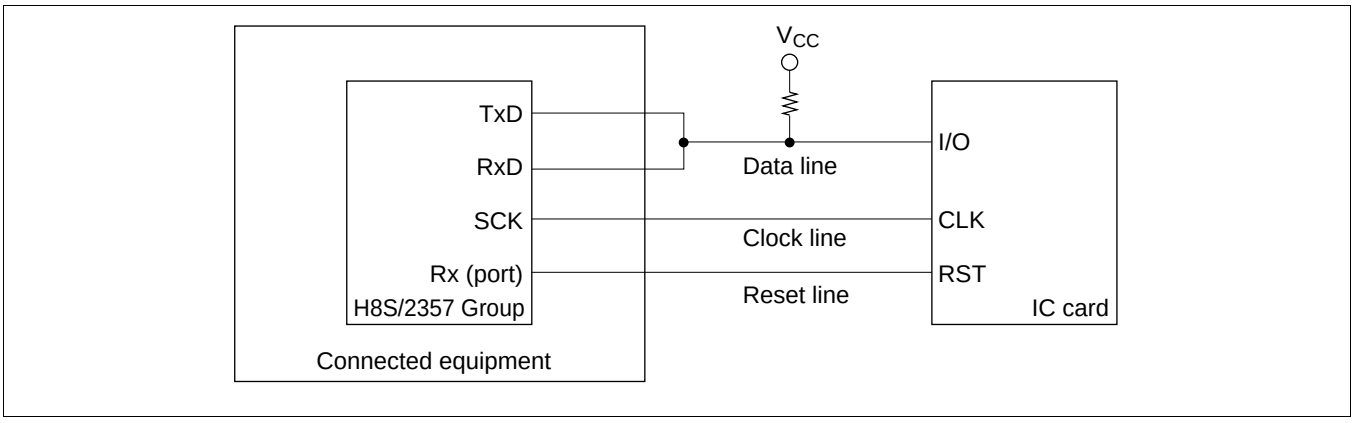


Figure 15-2 Schematic Diagram of Smart Card Interface Pin Connections

Note: If an IC card is not connected, and the TE and RE bits are both set to 1, closed transmission/reception is possible, enabling self-diagnosis to be carried out.

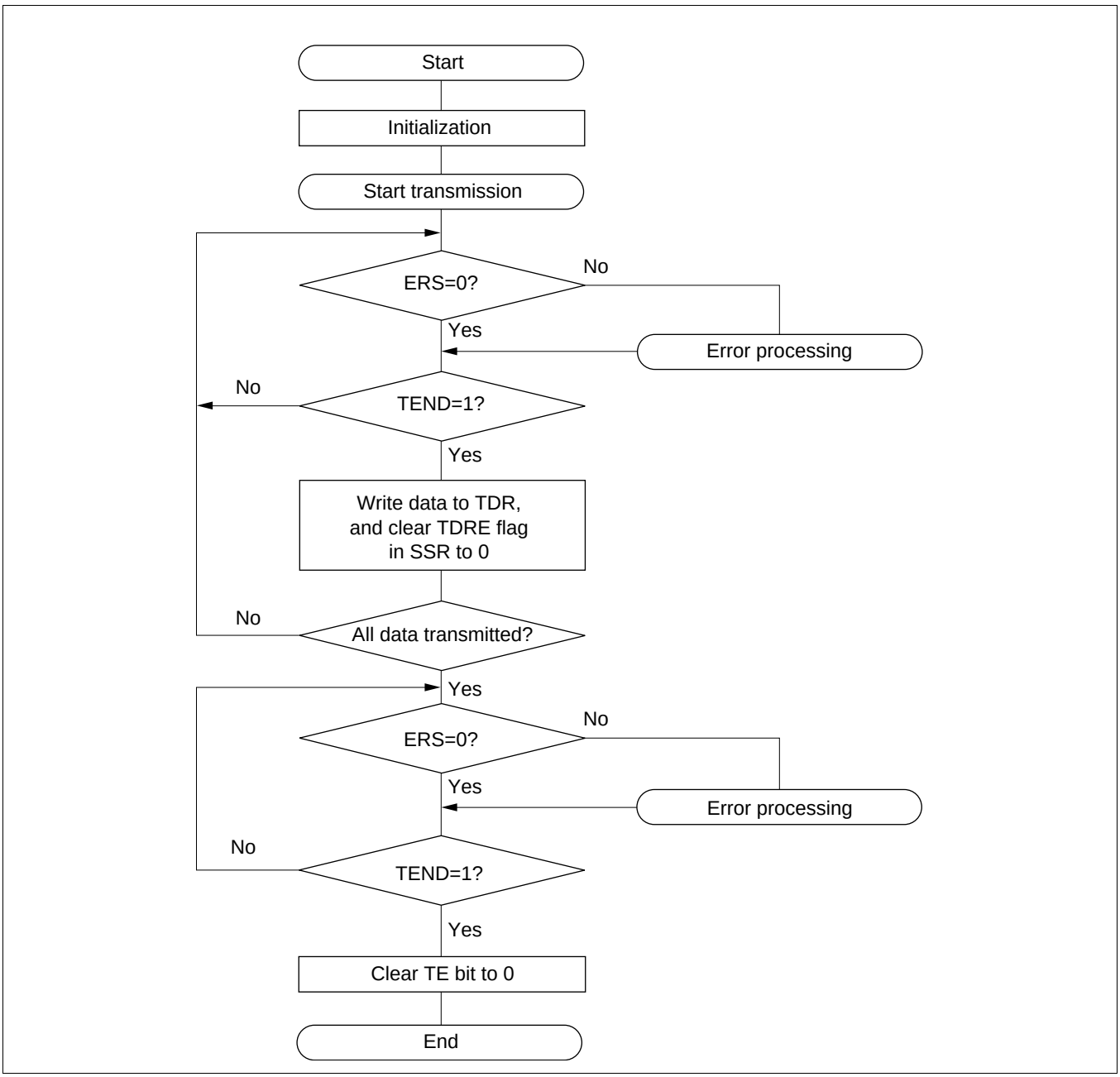
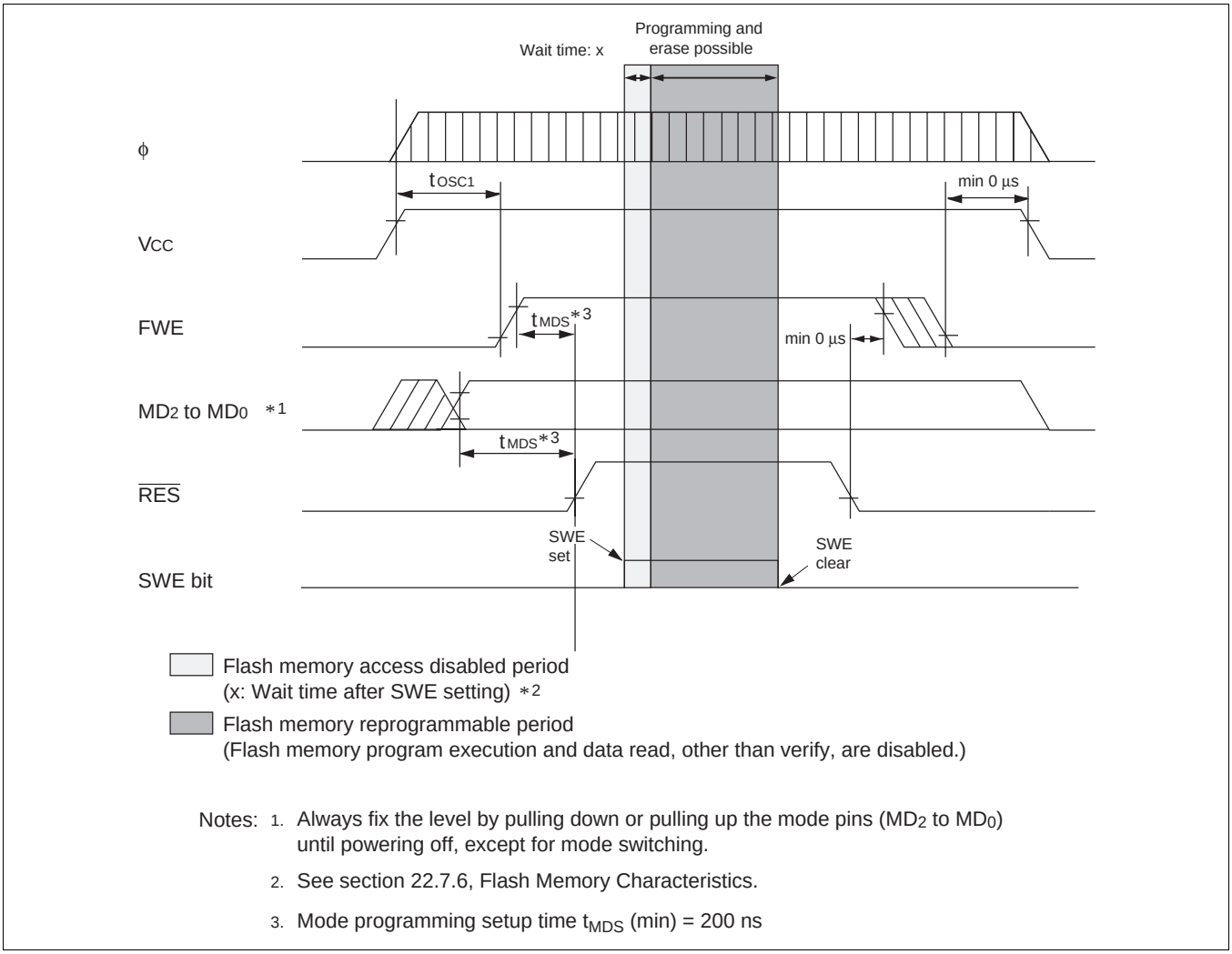


Figure 15-4 Example of Transmission Processing Flow



Notes: 1. Always fix the level by pulling down or pulling up the mode pins (MD_2 to MD_0) until powering off, except for mode switching.

2. See section 22.7.6, Flash Memory Characteristics.

3. Mode programming setup time t_{MDS} (min) = 200 ns

Figure 19-33 Powering On/Off Timing (Boot Mode)

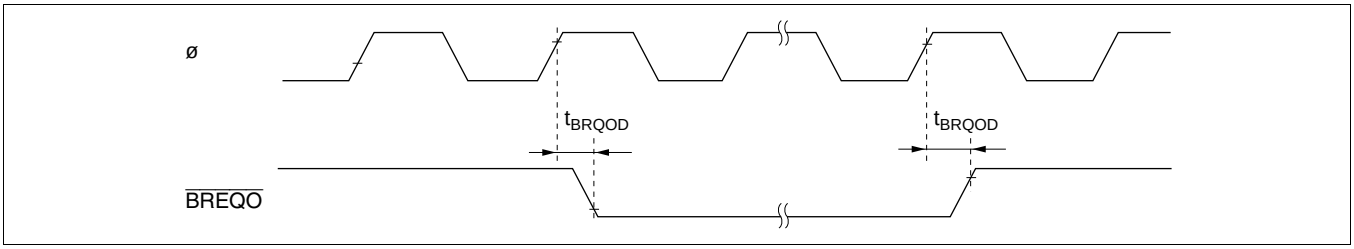


Figure 22-49 External Bus Request Output Timing

(4) DMAC Timing

Table 22-17 lists the DMAC timing.

Table 22-17 DMAC Timing

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, ø = 10 to 20 MHz, T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Item	Symbol	Condition Min	Condition Max	Unit	Test Conditions
$\overline{\text{DREQ}}$ setup time	t_{DRQS}	30	—	ns	Figure 22-53
$\overline{\text{DREQ}}$ hold time	t_{DRQH}	10	—		
$\overline{\text{TEND}}$ delay time	t_{TED}	—	20		Figure 22-52
$\overline{\text{DACK}}$ delay time 1	t_{DACD1}	—	20	ns	Figure 22-50, Figure 22-51
$\overline{\text{DACK}}$ delay time 2	t_{DACD2}	—	20		

Table A-1 Instruction Set

(1) Data Transfer Instructions

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)									Operation	Condition Code						No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa	—		I	H	N	Z	V	C	Advanced
MOV	MOV.B #xx:8,Rd	B	2									#xx:8→Rd8	—	—	↕	↕	0	—	1
	MOV.B Rs,Rd	B		2								Rs8→Rd8	—	—	↕	↕	0	—	1
	MOV.B @ERs,Rd	B			2							@ERs→Rd8	—	—	↕	↕	0	—	2
	MOV.B @(d:16,ERs),Rd	B				4						@(d:16,ERs)→Rd8	—	—	↕	↕	0	—	3
	MOV.B @(d:32,ERs),Rd	B				8						@(d:32,ERs)→Rd8	—	—	↕	↕	0	—	5
	MOV.B @ERs+,Rd	B					2					@ERs→Rd8,ERs32+1→ERs32	—	—	↕	↕	0	—	3
	MOV.B @aa:8,Rd	B						2				@aa:8→Rd8	—	—	↕	↕	0	—	2
	MOV.B @aa:16,Rd	B						4				@aa:16→Rd8	—	—	↕	↕	0	—	3
	MOV.B @aa:32,Rd	B						6				@aa:32→Rd8	—	—	↕	↕	0	—	4
	MOV.B Rs,@ERd	B			2							Rs8→@ERd	—	—	↕	↕	0	—	2
	MOV.B Rs,@(d:16,ERd)	B				4						Rs8→@(d:16,ERd)	—	—	↕	↕	0	—	3
	MOV.B Rs,@(d:32,ERd)	B				8						Rs8→@(d:32,ERd)	—	—	↕	↕	0	—	5
	MOV.B Rs,@-ERd	B					2					ERd32-1→ERd32,Rs8→@ERd	—	—	↕	↕	0	—	3
	MOV.B Rs,@aa:8	B						2				Rs8→@aa:8	—	—	↕	↕	0	—	2
	MOV.B Rs,@aa:16	B						4				Rs8→@aa:16	—	—	↕	↕	0	—	3
	MOV.B Rs,@aa:32	B						6				Rs8→@aa:32	—	—	↕	↕	0	—	4
	MOV.W #xx:16,Rd	W	4									#xx:16→Rd16	—	—	↕	↕	0	—	2
	MOV.W Rs,Rd	W		2								Rs16→Rd16	—	—	↕	↕	0	—	1
	MOV.W @ERs,Rd	W			2							@ERs→Rd16	—	—	↕	↕	0	—	2

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)									Operation	Condition Code						No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa	|		I	H	N	Z	V	C	Advanced
EXTS	EXTS.W Rd	W		2								(<bit 7> of Rd16)→ (<bit 15 to 8> of Rd16)	—	—	↕	↕	0	—	1
	EXTS.L ERd	L		2								(<bit 15> of ERd32)→ (<bit 31 to 16> of ERd32)	—	—	↕	↕	0	—	1
TAS	TAS @ERd*3	B			4							@ERd-0→CCR set, (1)→ (<bit 7> of @ERd)	—	—	↕	↕	0	—	4
MAC	MAC @ERn+, @ERm+	Cannot be used in the H8S/2357 Group																	[2]
CLRMAC	CLRMAC																		
LDMAC	LDMAC ERs,MACH																		
	LDMAC ERs,MACL																		
STMAC	STMAC MACH,ERd																		
	STMAC MACL,ERd																		

Instruction	Mnemonic	Size	Instruction Format																	
			1st byte		2nd byte		3rd byte		4th byte		5th byte		6th byte		7th byte		8th byte		9th byte	10th byte
MOV	MOV.W @ERs+,Rd	W	6	D	0 ers	rd														
	MOV.W @aa:16,Rd	W	6	B	0	rd	abs													
	MOV.W @aa:32,Rd	W	6	B	2	rd	abs													
	MOV.W Rs,@ERd	W	6	9	1 erd	rs														
	MOV.W Rs,@(d:16,ERd)	W	6	F	1 erd	rs	disp													
	MOV.W Rs,@(d:32,ERd)	W	7	8	0 erd	0	6	B	A	rs	disp									
	MOV.W Rs,@-ERd	W	6	D	1 erd	rs														
	MOV.W Rs,@aa:16	W	6	B	8	rs	abs													
	MOV.W Rs,@aa:32	W	6	B	A	rs	abs													
	MOV.L #xx:32,ERd	L	7	A	0	0 erd	IMM													
	MOV.L ERs,ERd	L	0	F	1 ers	0 erd														
	MOV.L @ERs,ERd	L	0	1	0	0	6	9	0 ers	0 erd										
	MOV.L @(d:16,ERs),ERd	L	0	1	0	0	6	F	0 ers	0 erd	disp									
	MOV.L @(d:32,ERs),ERd	L	0	1	0	0	7	8	0 ers	0	6	B	2	0 erd	disp					
	MOV.L @ERs+,ERd	L	0	1	0	0	6	D	0 ers	0 erd										
	MOV.L @aa:16 ,ERd	L	0	1	0	0	6	B	0	0 erd	abs									
	MOV.L @aa:32 ,ERd	L	0	1	0	0	6	B	2	0 erd	abs									
	MOV.L ERs,@ERd	L	0	1	0	0	6	9	1 erd	0 ers										
	MOV.L ERs,@(d:16,ERd)	L	0	1	0	0	6	F	1 erd	0 ers	disp									
	MOV.L ERs,@(d:32,ERd)*[1]	L	0	1	0	0	7	8	0 erd	0	6	B	A	0 ers	disp					
	MOV.L ERs,@-ERd	L	0	1	0	0	6	D	1 erd	0 ers										
	MOV.L ERs,@aa:16	L	0	1	0	0	6	B	8	0 ers	abs									
	MOV.L ERs,@aa:32	L	0	1	0	0	6	B	A	0 ers	abs									
MOVFPE	MOVFPE @aa:16,Rd	B	Cannot be used in the H8S/2357 Group																	
MOVTPE	MOVTPE Rs,@aa:16	B																		
MULXS	MULXS.B Rs,Rd	B	0	1	C	0	5	0	rs	rd										
	MULXS.W Rs,ERd	W	0	1	C	0	5	2	rs	0 erd										
MULXU	MULXU.B Rs,Rd	B	5	0	rs	rd														
	MULXU.W Rs,ERd	W	5	2	rs	0 erd														

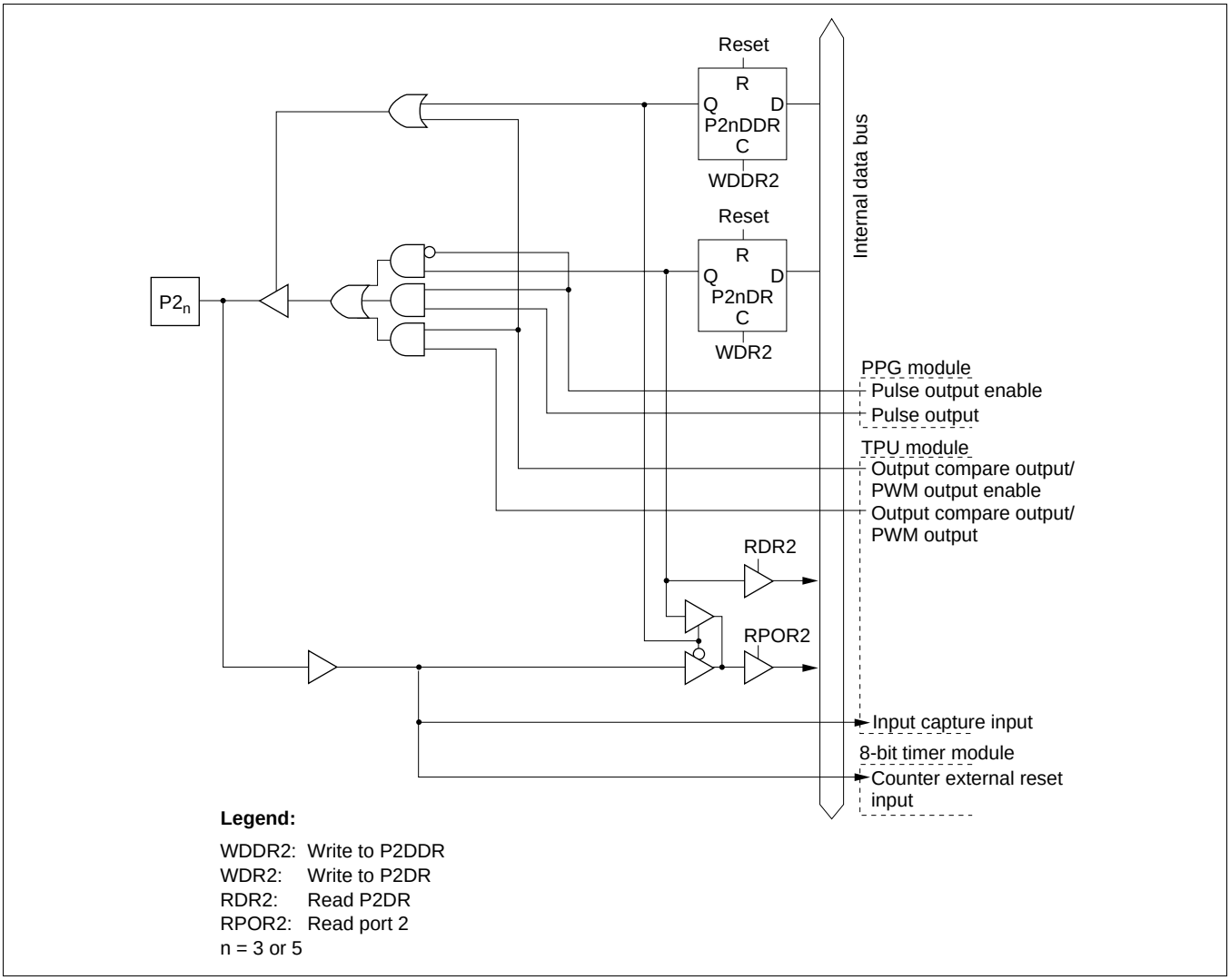


Figure C-2 (c) Port 2 Block Diagram (Pins $P2_3$ and $P2_5$)