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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

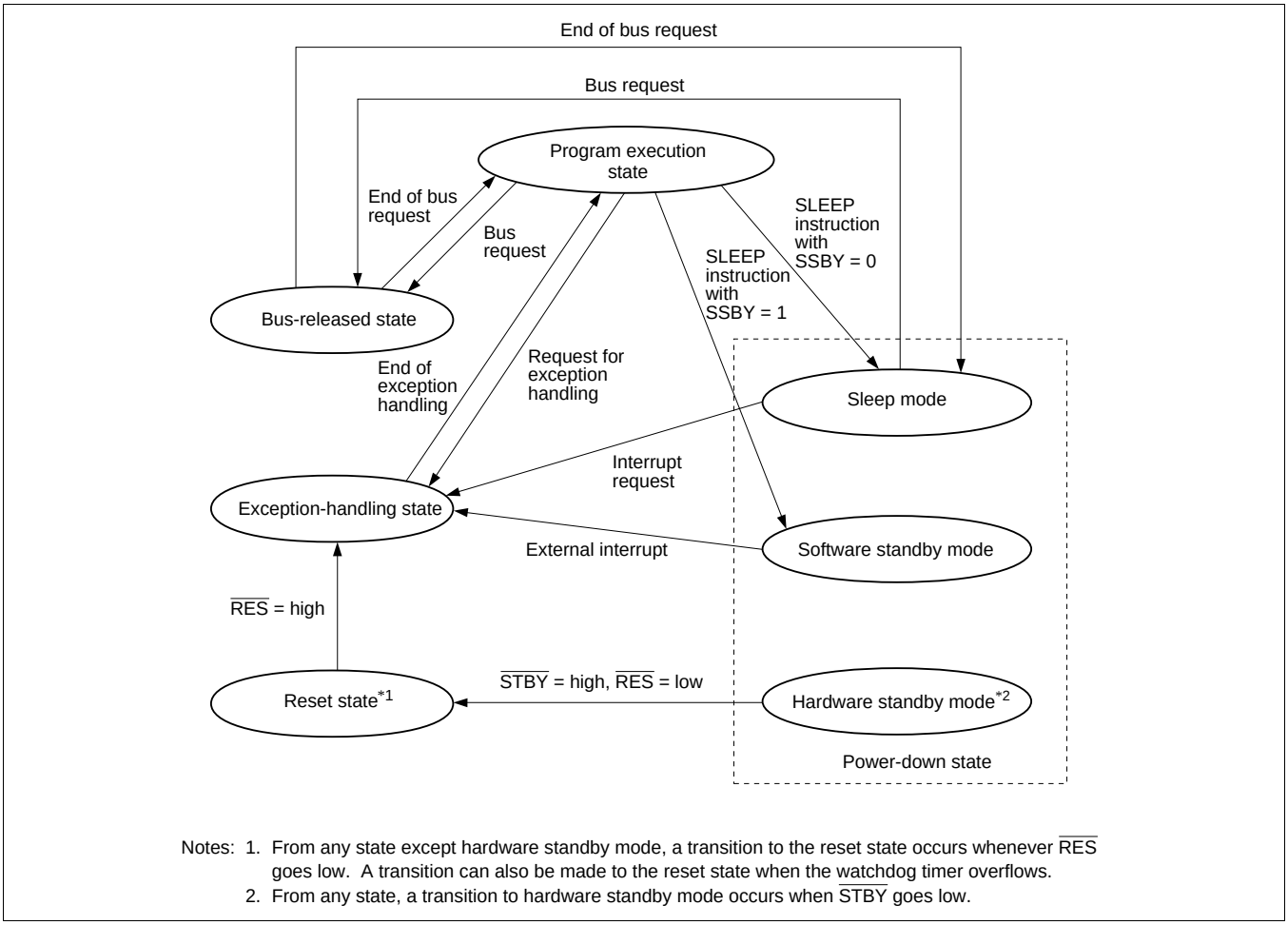
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	87
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2398te20v

Item	Page	Revision (See Manual for Details)
G. Product Code Lineup Table G-2 H8S/2398, H8S/2394, H8S/2392, H8S/2390 Group Product Code Lineup	1014	Table G-2 amended

Product Type		Product Code	Mark Code	Package (Package Code)
H8S/2398	Masked ROM	HD6432398	HD6432398TE*1	120-pin TQFP (TFP-120)
			HD6432398F*1	128-pin QFP (FP-128B)
	F-ZTAT	HD64F2398	HD64F2398TE*1	120-pin TQFP (TFP-120)
			HD64F2398F*1	128-pin QFP (FP-128B)
			HD64F2398TET	120-pin TQFP (TFP-120)
			HD64F2398FT	128-pin QFP (FP-128B)

H. Package Dimensions Figure H-1 TFP-120 Package Dimension	1015	Figure H-1 replaced



Notes: 1. From any state except hardware standby mode, a transition to the reset state occurs whenever $\overline{RES}$ goes low. A transition can also be made to the reset state when the watchdog timer overflows.
2. From any state, a transition to hardware standby mode occurs when $\overline{STBY}$ goes low.

Figure 2-12 State Transitions

2.8.2 Reset State

When the $\overline{RES}$ input goes low all current processing stops and the CPU enters the reset state. The CPU enters the power-on reset state when the NMI pin is high, or the manual reset* state when the NMI pin is low. All interrupts are masked in the reset state. Reset exception handling starts when the $\overline{RES}$ signal changes from low to high.

The reset state can also be entered by a watchdog timer overflow. For details, refer to section 13, Watchdog Timer.

Note: * Manual reset is only supported in the H8S/2357 ZTAT.

2.8.3 Exception-Handling State

The exception-handling state is a transient state that occurs when the CPU alters the normal processing flow due to a reset, interrupt, or trap instruction. The CPU fetches a start address (vector) from the exception vector table and branches to that address.

(1) Types of Exception Handling and Their Priority

Exception handling is performed for traces, resets, interrupts, and trap instructions. Table 2-7 indicates the types of exception handling and their priority. Trap instruction exception handling is always accepted, in the program execution state.

Exception handling and the stack structure depend on the interrupt control mode set in SYSCR.

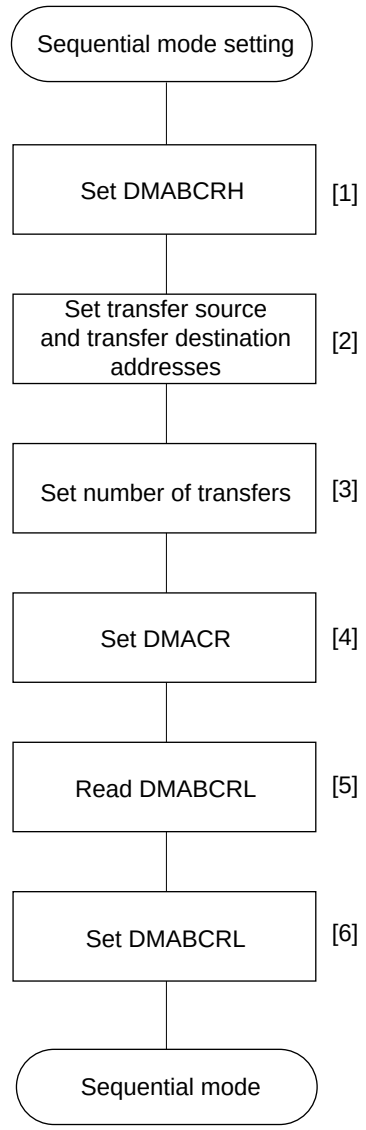
6.12 Resets and the Bus Controller

In a power-on reset, the H8S/2357 Group, including the bus controller, enters the reset state at that point, and an executing bus cycle is discontinued.

In a manual reset*, the bus controller's registers and internal state are maintained, and an executing external bus cycle is completed. In this case, $\overline{\text{WAIT}}$ input is ignored. Also, since the DMAC is initialized by a manual reset*, $\overline{\text{DACK}}$ and $\overline{\text{TEND}}$ output is disabled and these pins become I/O ports controlled by DDR and DR.

Note: * Manual reset is only supported in the H8S/2357 ZTAT.

Figure 7-4 shows an example of the setting procedure for sequential mode.



[1] Set each bit in DMABCRH.
- Clear the FAE bit to 0 to select short address mode.
- Specify enabling or disabling of internal interrupt clearing with the DTA bit.

[2] Set the transfer source address and transfer destination address in MAR and IOAR.

[3] Set the number of transfers in ETCR.

[4] Set each bit in DMACR.
- Set the transfer data size with the DTSZ bit.
- Specify whether MAR is to be incremented or decremented with the DTID bit.
- Clear the RPE bit to 0 to select sequential mode.
- Specify the transfer direction with the DTDIR bit.
- Select the activation source with bits DTF3 to DTF0.

[5] Read the DTE bit in DMABCRL as 0.

[6] Set each bit in DMABCRL.
- Specify enabling or disabling of transfer end interrupts with the DTIE bit.
- Set the DTE bit to 1 to enable transfer.

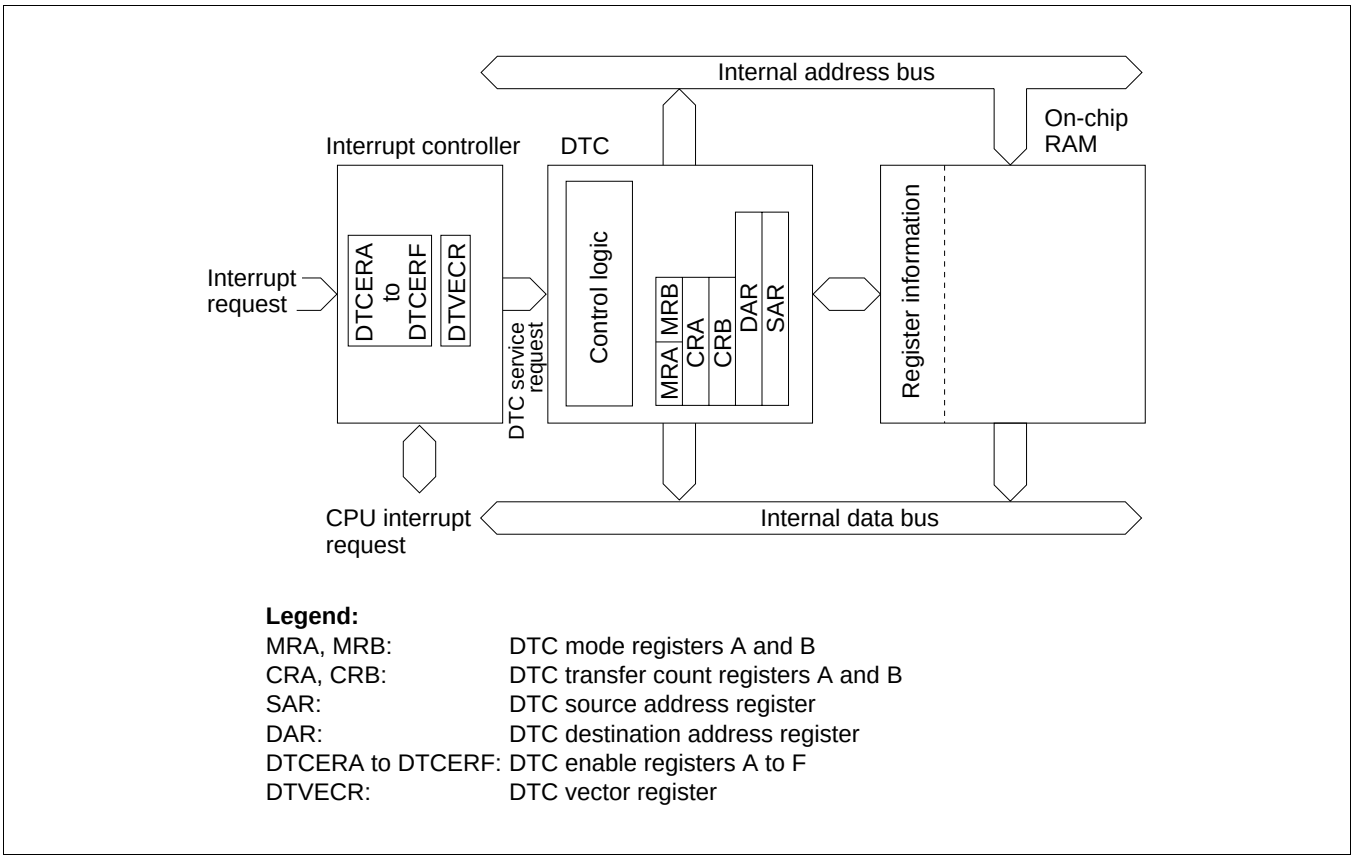
Figure 7-4 Example of Sequential Mode Setting Procedure

8.1.2 Block Diagram

Figure 8-1 shows a block diagram of the DTC.

The DTC's register information is stored in the on-chip RAM*. A 32-bit bus connects the DTC to the on-chip RAM (1 kbyte), enabling 32-bit/1-state reading and writing of the DTC register information and hence helping to increase processing speed.

Note: * When the DTC is used, the RAME bit in SYSCR must be set to 1.



Legend:

MRA, MRB:	DTC mode registers A and B
CRA, CRB:	DTC transfer count registers A and B
SAR:	DTC source address register
DAR:	DTC destination address register
DTCERA to DTCERF:	DTC enable registers A to F
DTVECR:	DTC vector register

Figure 8-1 Block Diagram of DTC

Bit 7—DTC Software Activation Enable (SWDTE): Enables or disables DTC activation by software.

When clearing the SWDTE bit to 0 by software, write 0 to SWDTE after reading SWDTE set to 1.

Bit 7 SWDTE	Description	
0	DTC software activation is disabled	(Initial value)
	[Clearing condition]	
	When the DISEL bit is 0 and the specified number of transfers have not ended	
1	DTC software activation is enabled	
	[Holding conditions]	
	• When the DISEL bit is 1 and data transfer has ended	
	• When the specified number of transfers have ended	
	• During data transfer due to software activation	

Bits 6 to 0—DTC Software Activation Vectors 6 to 0 (DTVEC6 to DTVEC0): These bits specify a vector number for DTC software activation.

The vector address is expressed as H'0400 + ((vector number) << 1). <<1 indicates a one-bit left-shift. For example, when DTVEC6 to DTVEC0 = H'10, the vector address is H'0420.

8.2.9 Module Stop Control Register (MSTPCR)

	MSTPCRH								MSTPCRL							
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value :	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MSTPCR is a 16-bit readable/writable register that performs module stop mode control.

When the MSTP14 bit in MSTPCR is set to 1, the DTC operation stops at the end of the bus cycle and a transition is made to module stop mode. However, 1 cannot be written in the MSTP14 bit while the DTC is operating. For details, see section 21.5, Module Stop Mode.

MSTPCR is initialized to H'3FFF by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 14—Module Stop (MSTP14): Specifies the DTC module stop mode.

Bit 14 MSTP14	Description	
0	DTC module stop mode cleared	(Initial value)
1	DTC module stop mode set	

8.3.5 Normal Mode

In normal mode, one operation transfers one byte or one word of data.

From 1 to 65,536 transfers can be specified. Once the specified number of transfers have ended, a CPU interrupt can be requested.

Table 8-5 lists the register information in normal mode and figure 8-6 shows memory mapping in normal mode.

Table 8-5 Register Information in Normal Mode

Name	Abbreviation	Function
DTC source address register	SAR	Designates source address
DTC destination address register	DAR	Designates destination address
DTC transfer count register A	CRA	Designates transfer count
DTC transfer count register B	CRB	Not used

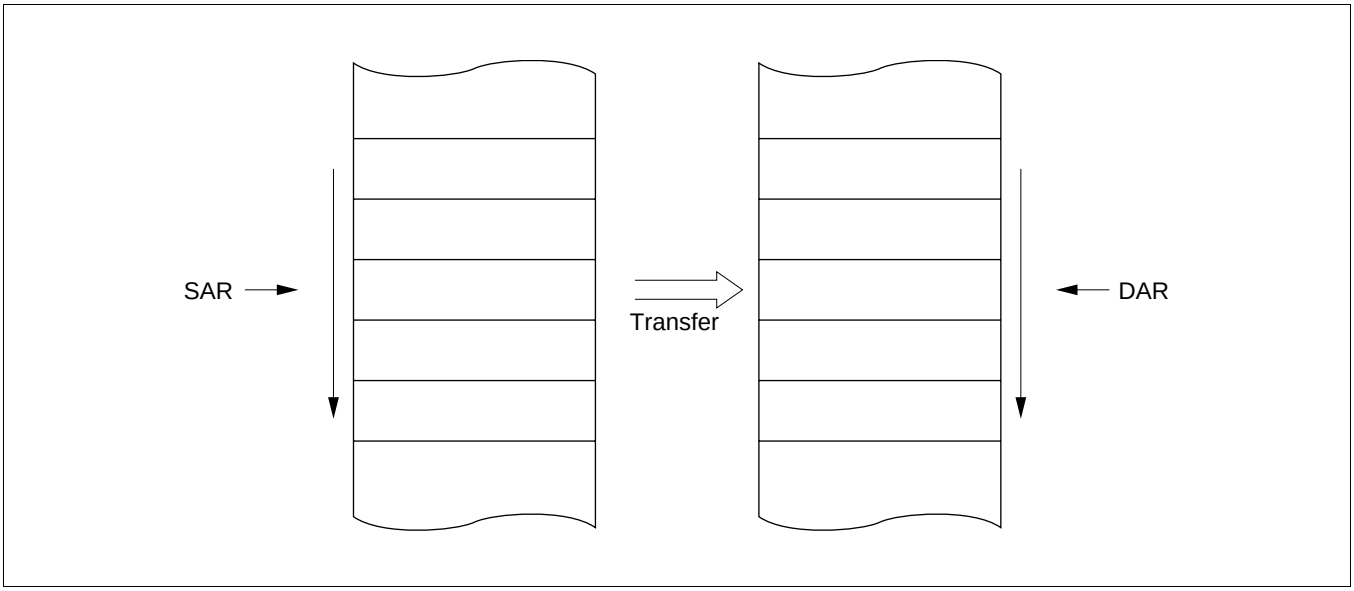


Figure 8-6 Memory Mapping in Normal Mode

10.3 Interface to Bus Master

10.3.1 16-Bit Registers

TCNT and TGR are 16-bit registers. As the data bus to the bus master is 16 bits wide, these registers can be read and written to in 16-bit units.

These registers cannot be read or written to in 8-bit units; 16-bit access must always be used.

An example of 16-bit register access operation is shown in figure 10-2.

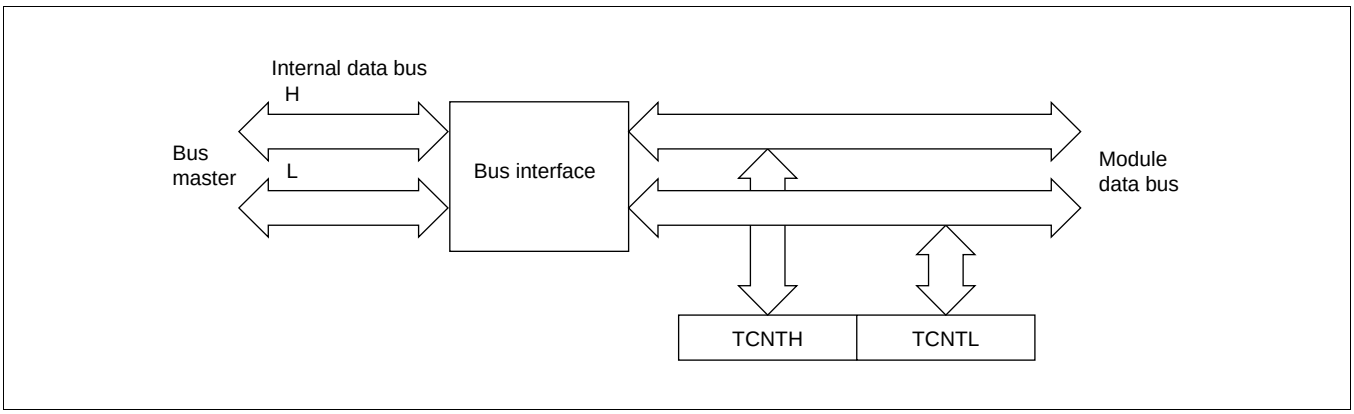


Figure 10-2 16-Bit Register Access Operation [Bus Master ↔ TCNT (16 Bits)]

Figure 10-27 shows examples of PWM waveform output with 0% duty and 100% duty in PWM mode.

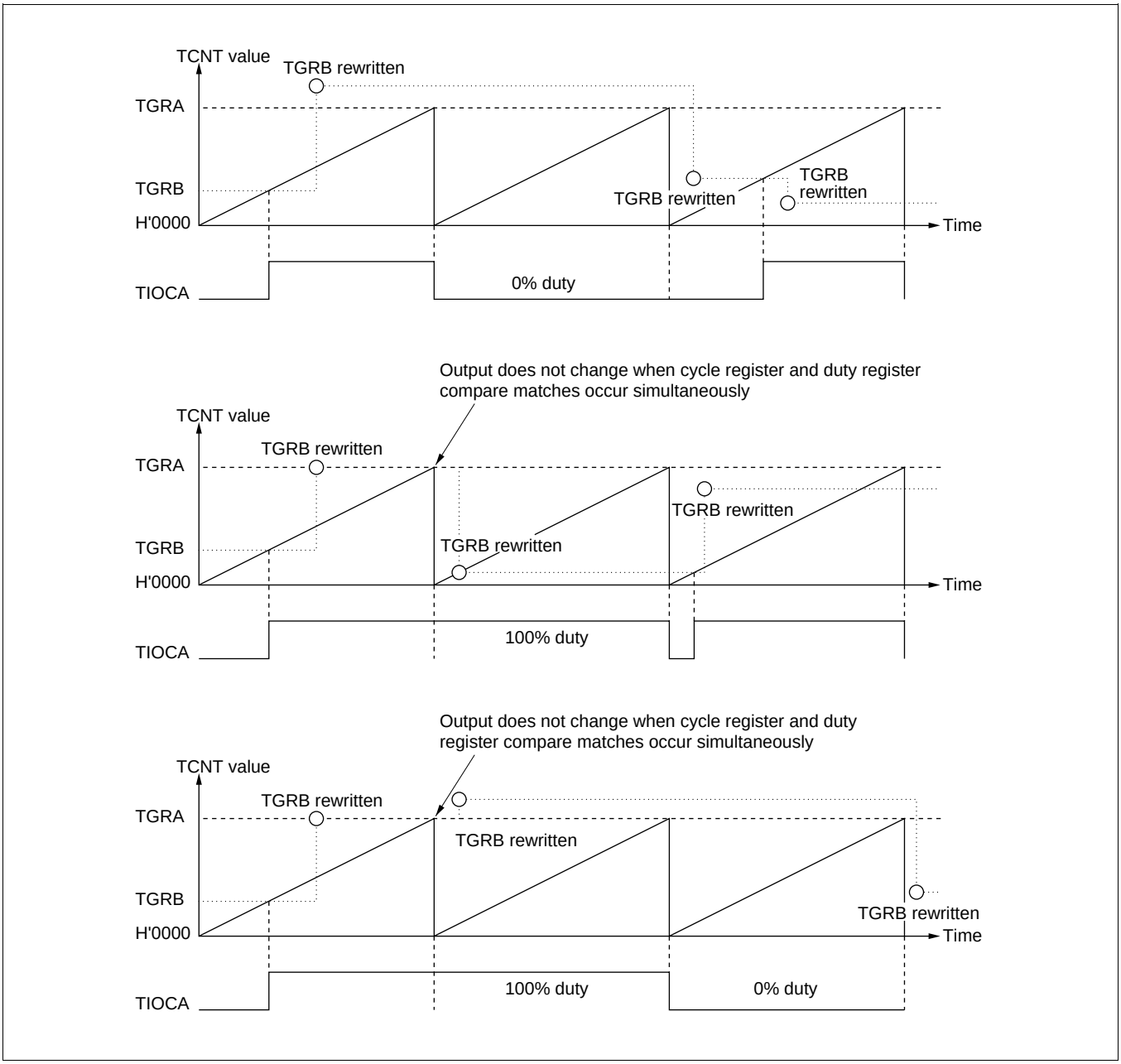


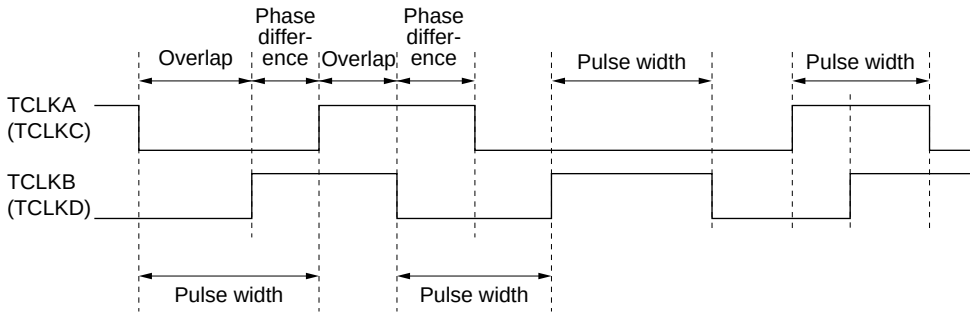
Figure 10-27 Example of PWM Mode Operation (3)

10.7 Usage Notes

Note that the kinds of operation and contention described below occur during TPU operation.

Input Clock Restrictions: The input clock pulse width must be at least 1.5 states in the case of single-edge detection, and at least 2.5 states in the case of both-edge detection. The TPU will not operate properly with a narrower pulse width.

In phase counting mode, the phase difference and overlap between the two input clocks must be at least 1.5 states, and the pulse width must be at least 2.5 states. Figure 10-48 shows the input clock conditions in phase counting mode.



Notes: Phase difference and overlap: 1.5 states or more
Pulse width : 2.5 states or more

Figure 10-48 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

Caution on Period Setting: When counter clearing by compare match is set, TCNT is cleared in the final state in which it matches the TGR value (the point at which the count value matched by TCNT is updated). Consequently, the actual counter frequency is given by the following formula:

$$f = \frac{ø}{(N + 1)}$$

Where f : Counter frequency
ø : Operating frequency
N : TGR set value

Contention between Buffer Register Write and Input Capture: If the input capture signal is generated in the T_2 state of a buffer write cycle, the buffer operation takes precedence and the write to the buffer register is not performed.

Figure 10-55 shows the timing in this case.

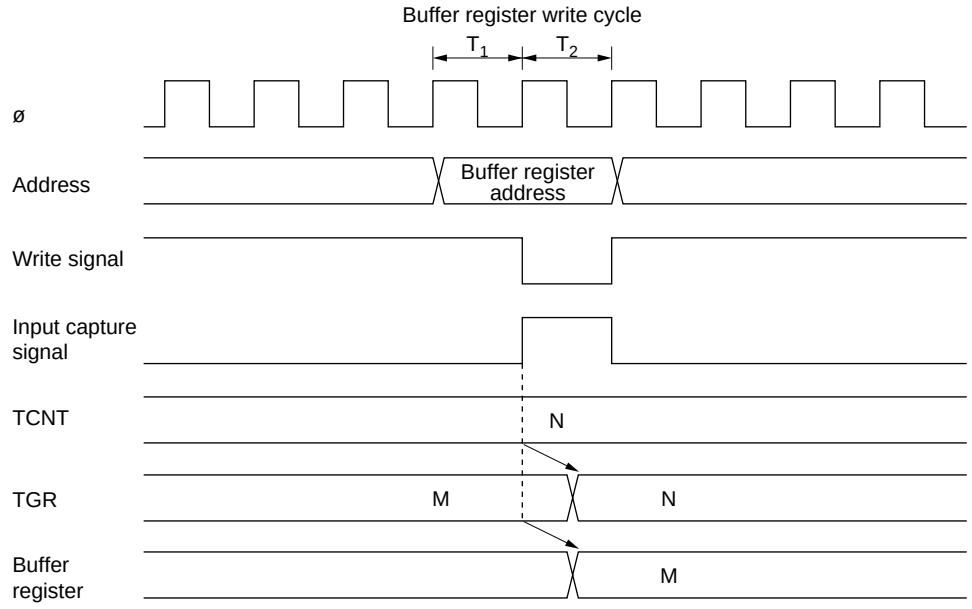


Figure 10-55 Contention between Buffer Register Write and Input Capture

Contention between Overflow/Underflow and Counter Clearing: If overflow/underflow and counter clearing occur simultaneously, the TCFV/TCFU flag in TSR is not set and TCNT clearing takes precedence.

Figure 10-56 shows the operation timing when a TGR compare match is specified as the clearing source, and H'FFFF is set in TGR.

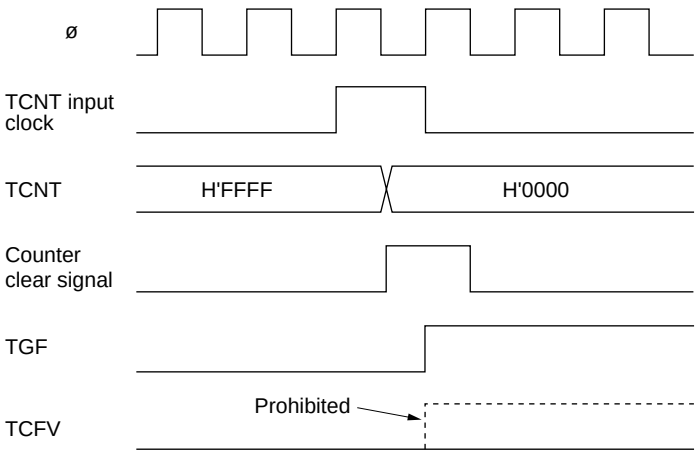


Figure 10-56 Contention between Overflow and Counter Clearing

15.3.4 Register Settings

Table 15-3 shows a bit map of the registers used by the Smart Card interface.

Bits indicated as 0 or 1 must be set to the value shown. The setting of other bits is described below.

Table 15-3 Smart Card Interface Register Settings

	Bit							
Register	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SMR	GM	0	1	O/$\overline{E}$	1	0	CKS1	CKS0
BRR	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0
SCR	TIE	RIE	TE	RE	0	0	CKE1*	CKE0
TDR	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
SSR	TDRE	RDRF	ORER	ERS	PER	TEND	0	0
RDR	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0
SCMR	—	—	—	—	SDIR	SINV	—	SMIF

Notes: — : Not used.
* The CKE1 bit must be cleared to 0 when the GM bit in SMR is cleared to 0.

SMR Setting: The GM bit is cleared to 0 in normal Smart Card interface mode, and set to 1 in GSM mode. The O/$\overline{E}$ bit is cleared to 0 if the IC card is of the direct convention type, and set to 1 if of the inverse convention type.

Bits CKS1 and CKS0 select the clock source of the on-chip baud rate generator. See section 15.3.5, Clock.

BRR Setting: BRR is used to set the bit rate. See section 15.3.5, Clock, for the method of calculating the value to be set.

SCR Setting: The function of the TIE, RIE, TE, and RE bits is the same as for the normal SCI. For details, see section 14, Serial Communication Interface (SCI).

Bits CKE1 and CKE0 specify the clock output. When the GM bit in SMR is cleared to 0, set these bits to B'00 if a clock is not to be output, or to B'01 if a clock is to be output. When the GM bit in SMR is set to 1, clock output is performed. The clock output can also be fixed high or low.

Smart Card Mode Register (SCMR) Setting:
The SDIR bit is cleared to 0 if the IC card is of the direct convention type, and set to 1 if of the inverse convention type.

The SINV bit is cleared to 0 if the IC card is of the direct convention type, and set to 1 if of the inverse convention type.

The SMIF bit is set to 1 in the case of the Smart Card interface.

Examples of register settings and the waveform of the start character are shown below for the two types of IC card (direct convention and inverse convention).

Bit 7—A/D End Flag (ADF): Status flag that indicates the end of A/D conversion.

Bit 7 ADF	Description	
0	[Clearing conditions] • When 0 is written to the ADF flag after reading ADF = 1 • When the DTC is activated by an ADI interrupt and ADDR is read	(Initial value)
1	[Setting conditions] • Single mode: When A/D conversion ends • Scan mode: When A/D conversion ends on all specified channels	

Bit 6—A/D Interrupt Enable (ADIE): Selects enabling or disabling of interrupt (ADI) requests at the end of A/D conversion.

Bit 6 ADIE	Description	
0	A/D conversion end interrupt (ADI) request disabled	(Initial value)
1	A/D conversion end interrupt (ADI) request enabled	

Bit 5—A/D Start (ADST): Selects starting or stopping on A/D conversion. Holds a value of 1 during A/D conversion.

The ADST bit can be set to 1 by software, a timer conversion start trigger, or the A/D external trigger input pin ($\overline{\text{ADTRG}}$).

Bit 5 ADST	Description	
0	• A/D conversion stopped	(Initial value)
1	• Single mode: A/D conversion is started. Cleared to 0 automatically when conversion on the specified channel ends. • Scan mode: A/D conversion is started. Conversion continues sequentially on the selected channels until ADST is cleared to 0 by software, a reset, or a transition to standby mode or module stop mode.	

Bit 4—Scan Mode (SCAN): Selects single mode or scan mode as the A/D conversion operating mode. See section 16.4, Operation, for single mode and scan mode operation. Only set the SCAN bit while conversion is stopped (ADST = 0).

Bit 4 SCAN	Description	
0	Single mode	(Initial value)
1	Scan mode	

Bit 3—Clock Select (CKS): Sets the A/D conversion time. Only change the conversion time while conversion is stopped (ADST = 0).

Bit 3 CKS	Description	
0	Conversion time = 266 states (max.)	(Initial value)
1	Conversion time = 134 states (max.)	

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current dissipation*2	Normal operation	I_{CC}*4	—	46 (5.0 V)	69	mA	f = 20 MHz
	Sleep mode		—	37 (5.0 V)	56	mA	f = 20 MHz
	Standby mode*3		—	0.01	10	µA	$T_a \leq 50°C$
			—	—	80		$50°C < T_a$
Analog power supply current	During A/D and D/A conversion	AI_{CC}	—	0.8 (5.0 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference current	During A/D and D/A conversion	AI_{CC}	—	2.2 (5.0 V)	3.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{ref} pins open. Connect AV_{CC} and V_{ref} to V_{CC} pin, and connect AV_{SS} to V_{SS} pin.

2. Current dissipation values are for V_{IH} min = V_{CC} -0.2 V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up MOS in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 4.5$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:
   I_{CC} max = 3.0 (mA) + 0.60 (mA/(MHz × V)) × V_{CC} × f [normal mode]
   I_{CC} max = 3.0 (mA) + 0.48 (mA/(MHz × V)) × V_{CC} × f [sleep mode]

Table 22-13 Permissible Output Currents

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 1, A to C	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 32 pins including ports 1 and A to C	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 22-13.

2. When driving a darlington pair or LED directly, always insert a current-limiting resistor in the output line, as show in figures 22-33 and 22-34.

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)										Operation	Condition Code						No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa	—			I	H	N	Z	V	C	Advanced
SHLR	SHLR.B Rd	B		2										—	—	0	↕	0	↕	1
	SHLR.B #2,Rd	B		2										—	—	0	↕	0	↕	1
	SHLR.W Rd	W		2									0 → MSB → LSB → C	—	—	0	↕	0	↕	1
	SHLR.W #2,Rd	W		2										—	—	0	↕	0	↕	1
	SHLR.L ERd	L		2										—	—	0	↕	0	↕	1
	SHLR.L #2,ERd	L		2										—	—	0	↕	0	↕	1
ROTXL	ROTXL.B Rd	B		2										—	—	↕	↕	0	↕	1
	ROTXL.B #2,Rd	B		2										—	—	↕	↕	0	↕	1
	ROTXL.W Rd	W		2									C ← MSB ← LSB	—	—	↕	↕	0	↕	1
	ROTXL.W #2,Rd	W		2										—	—	↕	↕	0	↕	1
	ROTXL.L ERd	L		2										—	—	↕	↕	0	↕	1
	ROTXL.L #2,ERd	L		2										—	—	↕	↕	0	↕	1
ROTXR	ROTXR.B Rd	B		2										—	—	↕	↕	0	↕	1
	ROTXR.B #2,Rd	B		2										—	—	↕	↕	0	↕	1
	ROTXR.W Rd	W		2									MSB → LSB → C	—	—	↕	↕	0	↕	1
	ROTXR.W #2,Rd	W		2										—	—	↕	↕	0	↕	1
	ROTXR.L ERd	L		2										—	—	↕	↕	0	↕	1
	ROTXR.L #2,ERd	L		2										—	—	↕	↕	0	↕	1

TIOR4—Timer I/O Control Register 4 H'FE92 TPU4

Bit	:	7	6	5	4	3	2	1	0
		IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR4A I/O Control

0	0	0	0	TGR4A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR4A is input capture register	Capture input source is TIOCA4 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	×			Input capture at both edges
	1	×	×		Capture input source is TGR3A compare match/ input capture	Input capture at generation of TGR3A compare match/input capture

×: Don't care

TGR4B I/O Control

0	0	0	0	TGR4B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR4B is input capture register	Capture input source is TIOCB4 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	×			Input capture at both edges
	1	×	×		Capture input source is TGR3C compare match/ input capture	Input capture at generation of TGR3C compare match/input capture

× : Don't care

P6DDR—Port 6 Data Direction Register H'FEB5 Port 6

Bit	7	6	5	4	3	2	1	0
	P67DDR	P66DDR	P65DDR	P64DDR	P63DDR	P62DDR	P61DDR	P60DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port 6 pins

PADDR—Port A Data Direction Register H'FEB9 Port A

Bit	7	6	5	4	3	2	1	0
	PA7DDR	PA6DDR	PA5DDR	PA4DDR	PA3DDR	PA2DDR	PA1DDR	PA0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port A pins

PBDDR—Port B Data Direction Register H'FEBA Port B
[On-chip ROM version Only]

Bit	7	6	5	4	3	2	1	0
	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port B pins

PCDDR—Port C Data Direction Register H'FEBB Port C
[On-chip ROM version Only]

Bit	7	6	5	4	3	2	1	0
	PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port C pins

TIER0—Timer Interrupt Enable Register 0 H'FFD4 TPU0

Bit	:	7	6	5	4	3	2	1	0
		TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Initial value	:	0	1	0	0	0	0	0	0
Read/Write	:	R/W	—	—	R/W	R/W	R/W	R/W	R/W

TGR Interrupt Enable A

0	Interrupt requests (TGIA) by TGFA bit disabled
1	Interrupt requests (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt requests (TGIB) by TGFB bit disabled
1	Interrupt requests (TGIB) by TGFB bit enabled

TGR Interrupt Enable C

0	Interrupt requests (TGIC) by TGFC bit disabled
1	Interrupt requests (TGIC) by TGFC bit enabled

TGR Interrupt Enable D

0	Interrupt requests (TGID) by TGFD bit disabled
1	Interrupt requests (TGID) by TGFD bit enabled

Overflow Interrupt Enable

0	Interrupt requests (TCIV) by TCFV disabled
1	Interrupt requests (TCIV) by TCFV enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

C.10 Port D Block Diagram

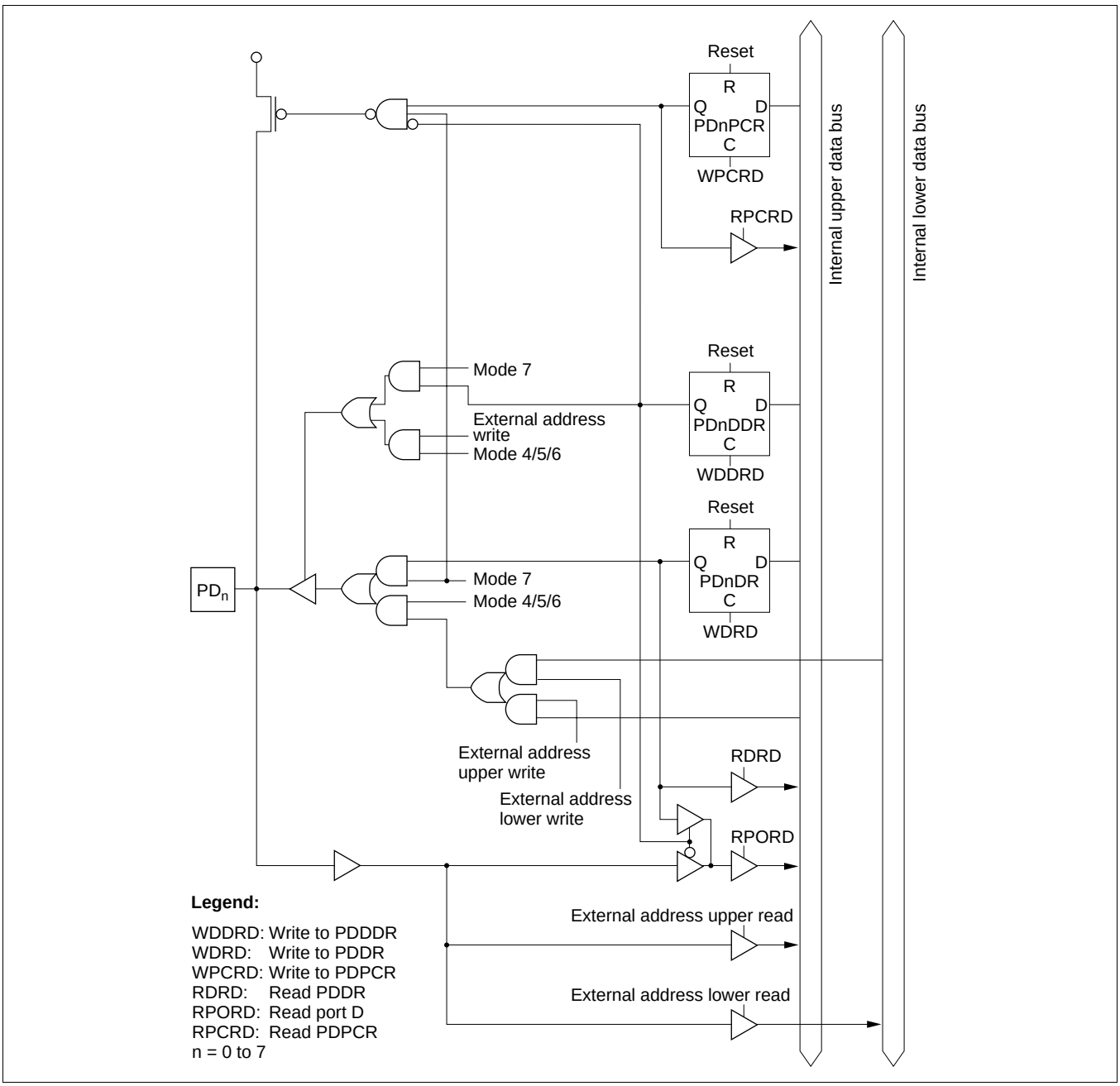


Figure C-10 Port D Block Diagram (Pin PD_0 to PD_7)

H8S/2357 Group, H8S/2357F-ZTAT™, H8S/2398F-ZTAT™ Hardware Manual

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