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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 10K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s010t-1fgg484

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Table 4 • Recommended Operating Conditions (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
3.3 V DC supply voltage	V_{DDIX}	3.15	3.3	3.45	V	
LVDS differential I/O	V_{DDIX}	2.375	2.5	3.45	V	
B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O	V_{DDIX}	2.375	2.5	2.625	V	
LVPECL differential I/O	V_{DDIX}	3.15	3.3	3.45	V	
Reference voltage supply for FDDR (Bank0) and MDDR (Bank5)	V_{REFX}	0.49 × V_{DDIX}	0.5 × V_{DDIX}	0.51 × V_{DDIX}	V	
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V_{PP} .	V_{PPNVM}	2.375 3.15	2.5 3.3	2.625 3.45	V	2.5 V range 3.3 V range

1. Programming at Industrial temperature range is available only with $V_{PP} = 3.3$ V.

Note: Power supply ramps must all be strictly monotonic, without plateaus.

Table 5 • FPGA Operating Limits

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Digest Temperature	Digest Cycles	Retention (Biased/Unbiased)
Commercial	FPGA	Min $T_J = 0$ °C Max $T_J = 85$ °C	Min $T_J = 0$ °C Max $T_J = 85$ °C	500	Min $T_J = 0$ °C Max $T_J = 85$ °C	2000	20 years
Industrial ¹	FPGA	Min $T_J = -40$ °C Max $T_J = 100$ °C	Min $T_J = -40$ °C Max $T_J = 100$ °C	500	Min $T_J = -40$ °C Max $T_J = 100$ °C	2000	20 years

1. Programming at Industrial temperature range is available only with $V_{PP} = 3.3$ V.

Note: The retention specification is defined as the total number of programming and digest cycles. For example, 20 years of retention after 500 programming cycles.

Note: The digest cycle specification is 2000 digest cycles for every program cycle with a maximum of 500 programming cycles.

Note: If your product qualification requires accelerated programming cycles, see [Microsemi SoC Products Quality and Reliability Report](#) about recommended methodologies.

Table 9 • Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices (continued)

Device	Still Air	1.0 m/s	2.5 m/s	θ_{JB}	θ_{JC}	Unit
	θ_{JA}					
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W
FCS536	15.01	12.06	10.76	3.69	1.55	°C/W
FCV484	16.21	13.11	11.84	6.73	0.10	°C/W

2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

$$\begin{aligned}\theta_{JA} &= 14.7 \text{ °C/W (taken from Table 9, page 10).} \\ T_A &= 85 \text{ °C}\end{aligned}$$

$$\text{Maximum power allowed} = \frac{100 \text{ °C} - 85 \text{ °C}}{14.7 \text{ °C/W}} = 1.088 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

2.3.1.3 ESD Performance

See *RT0001: Microsemi Corporation - SoC Products Reliability Report* for information about ESD.

Table 43 • LVCMOS 2.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.2	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	$\Omega\sigma$
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 44 • LVCMOS 2.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	4 mA	4 mA	$V_{DDI} - 0.4$	0.4	4	4
6 mA	6 mA	6 mA	$V_{DDI} - 0.4$	0.4	6	6
8 mA	8 mA	8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	12 mA	12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA		16 mA	$V_{DDI} - 0.4$	0.4	16	16

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 45 • LVCMOS 2.5 V Receiver Characteristics (Input Buffers)

	On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
		-1	-Std	-1	-Std	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.29	2.694	2.305	2.712	ns

Table 46 • LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

Table 67 • LVCMOS 1.5 V Receiver Characteristics for DDRIO I/O Bank with Fixed Codes (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.051	2.413	2.086	2.455	ns

Table 68 • LVCMOS 1.5 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	3.311	3.896	3.285	3.865	ns
50	3.654	4.299	3.623	4.263	ns
75	3.533	4.156	3.501	4.119	ns
150	3.415	4.018	3.388	3.986	ns

Table 69 • LVCMOS 1.5 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.959	3.481	2.93	3.447	ns
50	3.298	3.88	3.268	3.845	ns
75	3.162	3.719	3.128	3.68	ns
150	3.053	3.592	3.021	3.554	ns

Table 70 • LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	5.122	6.026	4.31	5.07	5.145	6.052	5.258	6.186	4.672	5.496	ns
	Medium	4.58	5.389	3.86	4.54	4.6	5.411	4.977	5.855	4.357	5.126	ns
	Medium fast	4.323	5.086	3.629	4.269	4.341	5.107	4.804	5.652	4.228	4.974	ns
	Fast	4.296	5.054	3.609	4.245	4.314	5.075	4.791	5.636	4.219	4.963	ns
4 mA	Slow	4.449	5.235	3.707	4.361	4.443	5.227	6.058	7.127	5.458	6.421	ns
	Medium	3.961	4.66	3.264	3.839	3.954	4.651	5.778	6.797	5.116	6.018	ns
	Medium fast	3.729	4.387	3.043	3.579	3.72	4.376	5.63	6.624	4.981	5.86	ns
	Fast	3.704	4.358	3.027	3.56	3.695	4.347	5.624	6.617	4.973	5.851	ns

Table 85 • LVCMOS 1.2 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.883	4.568	4.868	5.726	5.329	6.269	7.994	9.404	7.527	8.855	ns
4 mA	Slow	3.774	4.44	4.188	4.926	4.613	5.426	8.972	10.555	8.315	9.782	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.11 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to MSIO Bank Only)

Table 86 • PCI/PCI-X DC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

Table 87 • PCI/PCI-X DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	3.45	V
Input current high ¹	$I_{IH}(DC)$			
Input current low ¹	$I_{IL}(DC)$			

1. See Table 24, page 22.

Table 88 • PCI/PCI-X DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}		Per PCI specification		V
DC output logic low	V_{OL}		Per PCI specification		V

Table 89 • PCI/PCI-X Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (MSIO I/O bank)	D_{MAX}	630	Mbps	AC Loading: per JEDEC specifications

Table 90 • PCI/PCI-X AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path (falling edge)	V_{TRIP}	$0.615 \times V_{DDI}$	V
Measuring/trip point for data path (rising edge)	V_{TRIP}	$0.285 \times V_{DDI}$	V
Resistance for data test path	R_{TT_TEST}	25	Ω
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	10	pF

Table 95 • HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only

Parameter	Symbol	Min	Max	Unit
HSTL Class I				
DC output logic high	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current (MSIO and DDRIO I/O banks)	I_{OH} at V_{OH}	-8.0		mA
Output minimum sink current (MSIO and DDRIO I/O banks)	I_{OL} at V_{OL}	8.0		mA
HSTL Class II				
DC output logic high	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current	I_{OH} at V_{OH}	-16.0		mA
Output minimum sink current	I_{OL} at V_{OL}	16.0		mA

Table 96 • HSTL DC Differential Voltage Specification

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.2	V

Table 97 • HSTL AC Differential Voltage Specifications

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF}	0.4		V
AC differential cross point voltage	V_x	0.68	0.9	V

Table 98 • HSTL Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications

Table 99 • HSTL Impedance Specification

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	R_{REF}	25.5, 47.8	Ω	Reference resistance = 191 Ω
Effective impedance value (ODT for DDRIO I/O bank only)	R_{TT}	47.8	Ω	Reference resistance = 191 Ω

Table 112 • SSTL2 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

	On-Die Termination (ODT)	T_{PY}		Unit
		-1	-Std	
Pseudo differential	None	2.798	3.293	ns
True differential	None	2.733	3.215	ns

Table 113 • DDR1/SSTL2 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

	On-Die Termination (ODT)	T_{PY}		Unit
		-1	-Std	
Pseudo differential	None	2.476	2.913	ns
True differential	None	2.475	2.911	ns

Table 114 • SSTL2 Class I Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.26	2.66	1.99	2.341	1.985	2.335	2.135	2.512	2.13	2.505	ns
Differential	2.26	2.658	2.202	2.591	2.201	2.589	2.393	2.815	2.392	2.814	ns

Table 115 • DDR1/SSTL2 Class I Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.055	2.417	2.037	2.396	2.03	2.388	2.068	2.433	2.061	2.425	ns
Differential	2.192	2.58	2.434	2.864	2.425	2.852	2.164	2.545	2.156	2.536	ns

Table 116 • DDR1/SSTL2 Class I Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	1.512	1.779	1.462	1.72	1.462	1.72	1.676	1.972	1.676	1.971	ns
Differential	1.676	1.971	1.774	2.087	1.766	2.077	1.854	2.181	1.845	2.171	ns

Table 117 • DDR1/SSTL2 Class II Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.122	2.497	1.906	2.243	1.902	2.237	2.061	2.424	2.056	2.418	ns
Differential	2.127	2.501	2.042	2.402	2.043	2.403	2.363	2.78	2.365	2.781	ns

2.3.7.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 173 • B-LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 174 • B-LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	2.925	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 175 • B-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 176 • B-LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	65	460	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	1.1	1.5	V
Input common mode voltage	V_{ICM}	0.05	2.4	V
Input differential voltage	V_{ID}	0.1	V_{DDI}	V

Table 177 • B-LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 178 • B-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	27	Ω

Table 179 • B-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

2.3.10.2 Timing Characteristics

The following table lists the combinatorial cell propagation delays in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

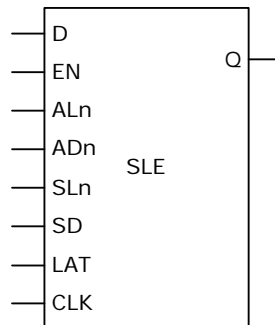
Table 223 • Combinatorial Cell Propagation Delays

Combinatorial Cell	Equation	Symbol	-1	-Std	Unit
INV	$Y = !A$	T_{PD}	0.1	0.118	ns
AND2	$Y = A \cdot B$	T_{PD}	0.164	0.193	ns
NAND2	$Y = !(A \cdot B)$	T_{PD}	0.147	0.173	ns
OR2	$Y = A + B$	T_{PD}	0.164	0.193	ns
NOR2	$Y = !(A + B)$	T_{PD}	0.147	0.173	ns
XOR2	$Y = A \oplus B$	T_{PD}	0.164	0.193	ns
XOR3	$Y = A \oplus B \oplus C$	T_{PD}	0.225	0.265	ns
AND3	$Y = A \cdot B \cdot C$	T_{PD}	0.209	0.246	ns
AND4	$Y = A \cdot B \cdot C \cdot D$	T_{PD}	0.287	0.338	ns

2.3.10.3 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

Figure 15 • Sequential Module



The following table lists the 010 device global resources in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 229 • 010 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.626	0.669	0.627	0.668	ns
Input high delay for global clock	T_{RCKH}	1.112	1.182	1.308	1.393	ns
Maximum skew for global clock	T_{RCKSW}		0.07		0.085	ns

The following table lists the 005 device global resources in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 230 • 005 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.625	0.66	0.628	0.66	ns
Input high delay for global clock	T_{RCKH}	1.126	1.187	1.325	1.397	ns
Maximum skew for global clock	T_{RCKSW}		0.061		0.072	ns

2.3.12 FPGA Fabric SRAM

See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

2.3.12.1 FPGA Fabric Large SRAM (LSRAM)

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 1K × 18 in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 231 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register				0.334	0.393	ns
Read access time without pipeline register	T_{CLK2Q}			2.273	2.674	ns
Access time with feed-through write timing				1.529	1.799	ns
Address setup time	T_{ADDRSU}	0.441		0.519		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.341		0.401		ns
Data hold time	T_{DHD}	0.107		0.126		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns

Table 238 • μ SRAM (RAM64x16) in 64 x 16 Mode (continued)

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	-0.026		-0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 128 x 9 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 239 • μ SRAM (RAM128x9) in 128 x 9 Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register				1.677		1.973
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode			1.856		2.184	
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode			-0.778		-0.915	
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns

Table 240 • μ SRAM (RAM128x8) in 128 x 8 Mode (continued)

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		-0.778		-0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.982	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	-0.026		-0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 270 • Math Block with Input Register Used and Output in Bypass Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input register setup time	T_{MISU}	0.149		0.176		ns
Input register hold time	T_{MIHD}	0.185		0.218		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	0.08		0.094		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	-0.012		-0.014		ns
Asynchronous reset removal time	$T_{MARSTREM}$	-0.005		-0.005		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Input register clock to output delay	T_{MICQ}		2.52		2.964	ns
CDIN to output delay	$T_{MCDIN2Q}$		1.951		2.295	ns

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 271 • Math Block with Input and Output in Bypass Mode

Parameter	Symbol	-1	-Std	Unit
		Max	Max	
Input to output delay	T_{MIQ}	2.568	3.022	ns
CDIN to output delay	$T_{MCDIN2Q}$	1.951	2.295	ns

2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 272 • eNVM Read Performance

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$F_{MAXREAD}$	eNVM maximum read frequency	25	25	25	25	25	25	MHz

The following table lists the eNVM page programming in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 273 • eNVM Page Programming

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$T_{PAGEPGM}$	eNVM page programming time	40	40	40	40	40	40	ms

Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz) (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Startup time (with regard to stable oscillator output)	SUXTAL			0.8	ms	005, 010, 025, and 050 devices
				1.0	ms	090 and 150 devices

Table 278 • Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		2		MHz	
Accuracy	ACCXTAL			0.00105	%	050 devices
				0.003	%	005, 010, 025, 090, and 150 devices
				0.004	%	060 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		1	5	ns	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		1	5	ns	
Operating current	IDYNXTAL		0.3		mA	
Input logic level high	VIHXTAL	0.9 V _{PP}			V	
Input logic level low	VILXTAL			0.1 V _{PP}	V	
Startup time (with regard to stable oscillator output)	SUXTAL			4.5	ms	010 and 050 devices
				5	ms	005 and 025 devices
				7	ms	090 and 150 devices

Table 279 • Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		32		kHz	
Accuracy	ACCXTAL			0.004	%	005, 010, 025, 050, 060, and 090 devices
				0.005	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		150	300	ns	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		150	300	ns	
Operating current	IDYNXTAL		0.044		mA	010 and 050 devices
			0.060		mA	005, 025, 060, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V _{PP}			V	
Input logic level low	VILXTAL			0.1 V _{PP}	V	
Startup time (with regard to stable oscillator output)	SUXTAL			115	ms	005, 025, 050, 090, and 150 devices
				126	ms	010 devices

2.3.30 SerDes Electrical and Timing AC and DC Characteristics

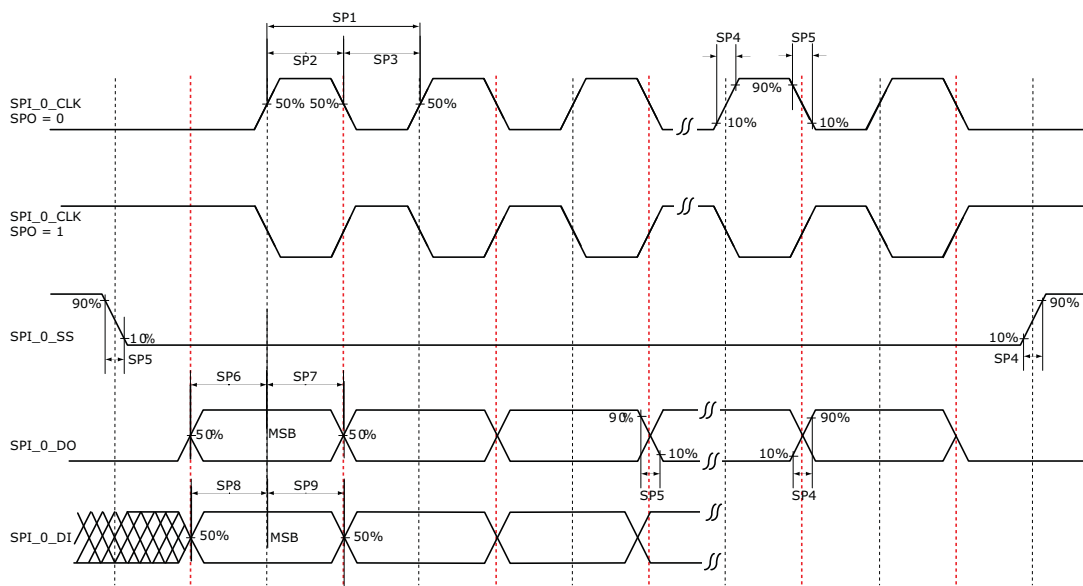
PCIe is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

The following table lists the transmitter parameters in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 296 • Transmitter Parameters

Symbol	Description	Min	Max	Unit
VTX-DIFF-PP	Differential swing (2.5 Gbps, 5.0 Gbps)	0.8	1.2	V
VTX-CM-AC-P	Output common mode voltage (2.5 Gbps)		20	mV
VTX-CM-AC-PP	Output common mode voltage (5.0 Gbps)		100	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%, 2.5 Gbps)	0.125		UI
	Rise and fall time (20% to 80%, 5.0 Gbps)	0.15		UI
ZTX-DIFF-DC	Output impedance–differential	80	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SerDes block (2.5 Gbps)		500 ps + 2 UI	ps
	Lane-to-lane TX skew within a SerDes block (5.0 Gbps)		500 ps + 4 UI	ps
RLTX-DIFF	Return loss differential mode (2.5 Gbps)	–10		dB
	Return loss differential mode (5.0 Gbps) 0.05 GHz to 1.25 GHz	–10		dB
	1.25 GHz to 2.5 GHz	–8		dB
RLTX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	–6		dB
TX-LOCK-RST	Transmit PLL lock time from reset		10	μs
VTX-AMP	100 mV setting	90	150	mV
	400 mV setting	320	480	mV
	800 mV setting	660	940	mV
	1200 mV setting	950	1400	mV

Figure 22 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)



2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 306 • CAN Controller Characteristics

Parameter	Description	-1	-Std	Unit
FCANREFCLK ¹	Internally sourced CAN reference clock frequency	160	136	MHz
BAUDCANMAX	Maximum CAN performance baud rate	1	1	Mbps
BAUDCANMIN	Minimum CAN performance baud rate	0.05	0.05	Mbps

1. PCLK to CAN controller must be a multiple of 8 MHz.

2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 307 • USB Characteristics

Parameter	Description	-1	-Std	Unit
FUSBREFCLK	Internally sourced USB reference clock frequency	166	142	MHz
TUSBCLK	USB clock period	16.66	16.66	ns
TUSBPD	Clock to USB data propagation delay	9.0	9.0	ns
TUSBSU	Setup time for USB data	6.0	6.0	ns
TUSBHD	Hold time for USB data	0	0	ns