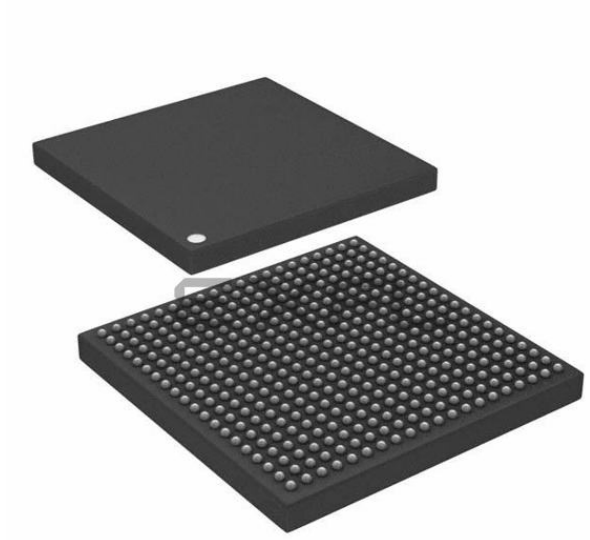


Welcome to E-XFL.COM

## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 256KB |
| RAM Size | 64KB |
| Peripherals | DDR, PCIe, SERDES |
| Connectivity | CANbus, Ethernet, I²C, SPI, UART/USART, USB |
| Speed | 166MHz |
| Primary Attributes | FPGA - 10K Logic Modules |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 400-LFBGA |
| Supplier Device Package | 400-VFBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2s010t-vf400 |

Table 15 Inrush Currents at Power up, 40 °C <= T $_J$ <= 100 °C Typical Process

| Power Supplies | Voltage (V) | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | 1.26 | 25 | 32 | 38 | 48 | 45 | 77 | 109 | mA |
| $V_{PP}$ | 3.46 | 33 | 49 | 36 | 180 | 13 | 36 | 51 | mA |
| $V_{DDI}$ | 2.62 | 134 | 141 | 161 | 187 | 93 | 272 | 388 | mA |
| Number of banks | | 7 | 8 | 8 | 10 | 10 | 9 | 19 | |

## 2.3.3 Average Fabric Temperature and Voltage Derating Factors

The following table lists the average temperature and voltage derating factors for fabric timing delays normalized to $T_J$ = 85 °C, in worst-case $V_{DD}$ = 1.14 V.

Table 16 Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays

| Array Voltage V $_{DD}$ (V) | 40 °C | 0 °C | 25 °C | 70 °C | 85 °C | 100 °C |
|---|---|---|---|---|---|---|
| 1.14 | 0.83 | 0.89 | 0.92 | 0.98 | 1.00 | 1.02 |
| 1.2 | 0.75 | 0.80 | 0.83 | 0.89 | 0.91 | 0.93 |
| 1.26 | 0.69 | 0.73 | 0.76 | 0.81 | 0.83 | 0.85 |

### 2.3.5.5 Detailed I/O Characteristics

Table 24 Input Capacitance, Leakage Current, and Ramp Time

| Symbol | Description | Maximum | Unit | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | 10 | pF | |
| $I_{IL}$ (dc) | Input current low (Applicable to HSTL/SSTL inputs only) | 400 | µA | $V_{DDI}$ = 2.5 V |
| | | 500 | µA | $V_{DDI}$ = 1.8 V |
| | | 600 | µA | $V_{DDI}$ = 1.5 V[1] |
| | Input current low (Applicable to all other digital inputs) | 10 | µA | |
| $I_{IH}$ (dc) | Input current high (Applicable to HSTL/SSTL inputs only) | 400 | µA | $V_{DDI}$ = 2.5 V |
| | | 500 | µA | $V_{DDI}$ = 1.8 V |
| | | 600 | µA | $V_{DDI}$ = 1.5 V[1] |
| | Input current high (Applicable to all other digital inputs) | 10 | µA | |
| $T_{RAMPIN}$[2] | Input ramp time (Applicable to all digital inputs) | 50 | ns | |

1. Applicable when I/O pair is programmed with an HSTL/SSTL I/O type on IOP and an un-terminated I/O type (LVCMOS, for example) on ION pad.
2. Voltage ramp must be monotonic.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of DDRIO I/O bank at $V_{OH}$/$V_{OL}$ Level.

Table 25 I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank

| | R(WEAK PULL-UP) at $V_{OH}$ ( : ) | | R(WEAK PULL-DOWN) at $V_{OL}$ ( : | |
|---|---|---|---|---|
| $V_{DDI}$ Domain | Min | Max | Min | Max |
| 2.5 V[1, 2] | 10K | 17.8K | 9.98K | 18K |
| 1.8 V[1, 2] | 10.3K | 19.1K | 10.3K | 19.5K |
| 1.5 V[1, 2] | 10.6K | 20.2K | 10.6K | 21.1K |
| 1.2 V[1, 2] | 11.1K | 22.7K | 11.2K | 24.6K |

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax VOHspec)/I(WEAK PULL-UP MIN).

Table 46 LVCMOS 2.5 V Transmitter Characteristics fo r DDRIO Bank (Output and Tristate Buffers) (continued)

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | |
| 4 mA | Slow | 3.095 | 3.641 | 2.705 | 3.182 | 3.088 | 3.633 | 4.738 | 5.575 | 4.348 | 5.116 | ns |
| | Medium | 2.825 | 3.324 | 2.488 | 2.927 | 2.823 | 3.321 | 4.492 | 5.285 | 4.063 | 4.781 | ns |
| | Medium fast | 2.701 | 3.178 | 2.384 | 2.804 | 2.698 | 3.173 | 4.364 | 5.135 | 3.945 | 4.642 | ns |
| | Fast | 2.69 | 3.165 | 2.377 | 2.796 | 2.687 | 3.161 | 4.359 | 5.129 | 3.94 | 4.636 | ns |
| 6 mA | Slow | 2.919 | 3.434 | 2.491 | 2.93 | 2.902 | 3.414 | 5.085 | 5.983 | 4.674 | 5.5 | ns |
| | Medium | 2.65 | 3.118 | 2.279 | 2.681 | 2.642 | 3.108 | 4.845 | 5.701 | 4.375 | 5.148 | ns |
| | Medium fast | 2.529 | 2.975 | 2.176 | 2.56 | 2.521 | 2.965 | 4.724 | 5.558 | 4.259 | 5.011 | ns |
| | Fast | 2.516 | 2.96 | 2.168 | 2.551 | 2.508 | 2.95 | 4.717 | 5.55 | 4.251 | 5.002 | ns |
| 8 mA | Slow | 2.863 | 3.368 | 2.427 | 2.855 | 2.844 | 3.346 | 5.196 | 6.114 | 4.769 | 5.612 | ns |
| | Medium | 2.599 | 3.058 | 2.217 | 2.608 | 2.59 | 3.047 | 4.952 | 5.827 | 4.471 | 5.261 | ns |
| | Medium fast | 2.483 | 2.921 | 2.114 | 2.487 | 2.473 | 2.91 | 4.832 | 5.685 | 4.364 | 5.134 | ns |
| | Fast | 2.467 | 2.902 | 2.106 | 2.478 | 2.457 | 2.89 | 4.826 | 5.678 | 4.348 | 5.116 | ns |
| 12 mA | Slow | 2.747 | 3.232 | 2.296 | 2.701 | 2.724 | 3.204 | 5.39 | 6.342 | 4.938 | 5.81 | ns |
| | Medium | 2.493 | 2.934 | 2.102 | 2.473 | 2.483 | 2.921 | 5.166 | 6.078 | 4.65 | 5.471 | ns |
| | Medium fast | 2.382 | 2.803 | 2.006 | 2.36 | 2.371 | 2.789 | 5.067 | 5.962 | 4.546 | 5.349 | ns |
| | Fast | 2.369 | 2.787 | 1.999 | 2.352 | 2.357 | 2.773 | 5.063 | 5.958 | 4.538 | 5.339 | ns |
| 16 mA | Slow | 2.677 | 3.149 | 2.213 | 2.604 | 2.649 | 3.116 | 5.575 | 6.56 | 5.08 | 5.977 | ns |
| | Medium | 2.432 | 2.862 | 2.028 | 2.386 | 2.421 | 2.848 | 5.372 | 6.32 | 4.801 | 5.649 | ns |
| | Medium fast | 2.324 | 2.734 | 1.937 | 2.278 | 2.311 | 2.718 | 5.297 | 6.233 | 4.7 | 5.531 | ns |
| | Fast | 2.313 | 2.721 | 1.929 | 2.269 | 2.3 | 2.706 | 5.296 | 6.231 | 4.699 | 5.529 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 47 LVCMOS 2.5 V Transmitter Characteristics fo r MSIO Bank (Output and Tristate Buffers)

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | |
| 2 mA | Slow | 3.48 | 4.095 | 3.855 | 4.534 | 3.785 | 4.453 | 2.12 | 2.494 | 3.45 | 4.059 | ns |
| 4 mA | Slow | 2.583 | 3.039 | 3.042 | 3.579 | 3.138 | 3.691 | 4.143 | 4.874 | 4.687 | 5.513 | ns |
| 6 mA | Slow | 2.392 | 2.815 | 2.669 | 3.139 | 2.82 | 3.317 | 4.909 | 5.775 | 5.083 | 5.98 | ns |
| 8 mA | Slow | 2.309 | 2.717 | 2.565 | 3.017 | 2.74 | 3.223 | 5.812 | 6.837 | 5.523 | 6.497 | ns |
| 12 mA | Slow | 2.333 | 2.745 | 2.437 | 2.867 | 2.626 | 3.089 | 6.131 | 7.213 | 5.712 | 6.72 | ns |
| 16 mA | Slow | 2.412 | 2.838 | 2.335 | 2.747 | 2.533 | 2.979 | 6.54 | 7.694 | 6.007 | 7.067 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 85 LVCMOS 1.2 V Transmitter Charac teristics for MSIOD I/O Bank (Output and Tris tate Buffers)

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | |
| 2 mA | Slow | 3.883 | 4.568 | 4.868 | 5.726 | 5.329 | 6.269 | 7.994 | 9.404 | 7.527 | 8.855 | ns |
| 4 mA | Slow | 3.774 | 4.44 | 4.188 | 4.926 | 4.613 | 5.426 | 8.972 | 10.555 | 8.315 | 9.782 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.11 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

Minimum and Maximum DC/AC Input and Output Leve ls Specification (Applicable to MSIO Bank Only)

Table 86 PCI/PCI-X DC Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V |

Table 87 PCI/PCI-X DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 3.45 | V |
| Input current high[1] | $I_{IH}$(DC) | | | |
| Input current low[1] | $I_{IL}$(DC) | | | |

1. See Table 24, page 22.

Table 88 PCI/PCI-X DC Output Voltage Specification

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | | Per PCI specification | | V |
| DC output logic low | $V_{OL}$ | | Per PCI specification | | V |

Table 89 PCI/PCI-X Minimum and Ma ximum AC Switching Speed

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (MSIO I/O bank) | $D_{MAX}$ | 630 | Mbps | AC Loading: per JEDEC specifications |

Table 90 PCI/PCI-X AC Test Parameter Specifications

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path (falling edge) | $V_{TRIP}$ | 0.615 ×$V_{DDI}$ | V |
| Measuring/trip point for data path (rising edge) | $V_{TRIP}$ | 0.285 ×$V_{DDI}$ | V |
| Resistance for data test path | RTT_TEST | 25 | : |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | : |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 10 | pF |

AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 ºC, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 3.0 V

Table 91 PCI/PCIX AC Switching Characteristic s for Receiver for MSIO I/O Bank (Input Buffers)

| | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|
| On-Die Termination (ODT) | 1 | Std | 1 | Std | Unit |
| None | 2.229 | 2.623 | 2.238 | 2.633 | ns |

Table 92 PCI/PCIX AC switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| 2.146 | 2.525 | 2.043 | 2.404 | 2.084 | 2.452 | 6.095 | 7.171 | 5.558 | 6.539 | ns |

## 2.3.6 Memory Interface and Vo ltage Referenced I/O Standards

This section describes High-Speed Transceiver Logic (HSTL) memory interface and voltage reference I/O standards.

### 2.3.6.1 High-Speed Tr ansceiver Logic (HSTL)

The HSTL standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 FPGA and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to DDRIO Bank Only)

Table 93 HSTL Recommended DC Op erating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.425 | 1.5 | 1.575 | V |
| Termination voltage | $V_{TT}$ | 0.698 | 0.750 | 0.803 | V |
| Input reference voltage | $V_{REF}$ | 0.698 | 0.750 | 0.803 | V |

Table 94 HSTL DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | $V_{REF}$ + 0.1 | 1.575 | V |
| DC input logic low | $V_{IL}$ (DC) | 0.3 | $V_{REF}$ 0.1 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

Table 112 SSTL2 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

| | On-Die Termination (ODT) | $T_{PY}$ | | |
|---|---|---|---|---|
| | | 1 | Std | Unit |
| Pseudo differential | None | 2.798 | 3.293 | ns |
| True differential | None | 2.733 | 3.215 | ns |

Table 113 DDR1/SSTL2 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

| | On-Die Termination (ODT) | $T_{PY}$ | | |
|---|---|---|---|---|
| | | 1 | Std | Unit |
| Pseudo differential | None | 2.476 | 2.913 | ns |
| True differential | None | 2.475 | 2.911 | ns |

Table 114 SSTL2 Class I Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| Single-ended | 2.26 | 2.66 | 1.99 | 2.341 | 1.985 | 2.335 | 2.135 | 2.512 | 2.13 | 2.505 | ns |
| Differential | 2.26 | 2.658 | 2.202 | 2.591 | 2.201 | 2.589 | 2.393 | 2.815 | 2.392 | 2.814 | ns |

Table 115 DDR1/SSTL2 Class I Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| Single-ended | 2.055 | 2.417 | 2.037 | 2.396 | 2.03 | 2.388 | 2.068 | 2.433 | 2.061 | 2.425 | ns |
| Differential | 2.192 | 2.58 | 2.434 | 2.864 | 2.425 | 2.852 | 2.164 | 2.545 | 2.156 | 2.536 | ns |

Table 116 DDR1/SSTL2 Class I Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| Single-ended | 1.512 | 1.779 | 1.462 | 1.72 | 1.462 | 1.72 | 1.676 | 1.972 | 1.676 | 1.971 | ns |
| Differential | 1.676 | 1.971 | 1.774 | 2.087 | 1.766 | 2.077 | 1.854 | 2.181 | 1.845 | 2.171 | ns |

Table 117 DDR1/SSTL2 Class II Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| Single-ended | 2.122 | 2.497 | 1.906 | 2.243 | 1.902 | 2.237 | 2.061 | 2.424 | 2.056 | 2.418 | ns |
| Differential | 2.127 | 2.501 | 2.042 | 2.402 | 2.043 | 2.403 | 2.363 | 2.78 | 2.365 | 2.781 | ns |

Table 128 DDR2/SSTL18 Transmitter Characterist ics (Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| SSTL18 Class I (for DDRIO I/O Bank) | | | | | | | | | | | |
| Single-ended | 2.383 | 2.804 | 2.23 | 2.623 | 2.229 | 2.622 | 2.202 | 2.591 | 2.201 | 2.59 | ns |
| Differential | 2.413 | 2.84 | 2.797 | 3.29 | 2.797 | 3.29 | 2.282 | 2.685 | 2.282 | 2.685 | ns |
| SSTL18 Class II (for DDRIO I/O Bank) | | | | | | | | | | | |
| Single-ended | 2.281 | 2.683 | 2.196 | 2.584 | 2.195 | 2.583 | 2.171 | 2.555 | 2.17 | 2.554 | ns |
| Differential | 2.315 | 2.724 | 2.698 | 3.173 | 2.698 | 3.173 | 2.242 | 2.639 | 2.242 | 2.639 | ns |

### 2.3.6.5 Stub-Series Termina ted Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

The following table lists the SSTL15 DC voltage specifications for DDRIO bank.

Table 129 SSTL15 DC Recommended DC Operating Cond itions (for DDRIO I/O Bank Only)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.425 | 1.5 | 1.575 | V |
| Termination voltage | $V_{TT}$ | 0.698 | 0.750 | 0.803 | V |
| Input reference voltage | $V_{REF}$ | 0.698 | 0.750 | 0.803 | V |

Table 130 SSTL15 DC Input Voltage Specificat ion (for DDRIO I/O Bank Only)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}(DC)$ | $V_{REF}$ + 0.1 | 1.575 | V |
| DC input logic low | $V_{IL}(DC)$ | 0.3 | $V_{REF}$ 0.1 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

Table 150 LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ENZL}$ | | $T_{ENZH}$ | | $T_{ENHZ}$ | | $T_{ENLZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| Single-ended | 2.281 | 2.683 | 2.196 | 2.584 | 2.195 | 2.583 | 2.171 | 2.555 | 2.17 | 2.554 | ns |
| Differential | 2.298 | 2.703 | 2.288 | 2.692 | 2.288 | 2.692 | 2.593 | 3.051 | 2.593 | 3.051 | ns |

Minimum and Maximum DC/AC Input and Output L evels Specification us ing LPDDR-LVCMOS 1.8 V Mode

Table 151 LPDDR-LVCMOS 1.8 V Mode Reco mmended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.710 | 1.8 | 1.89 | V |

Table 152 LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 0.65 ×$V_{DDI}$ | 1.89 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 0.65 ×$V_{DDI}$ | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | 0.3 | 0.35 ×$V_{DDI}$ | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

Table 153 LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | $V_{DDI}$ 0.45 | | V |
| DC output logic low | $V_{OL}$ | | 0.45 | V |

Table 154 LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 400 | Mbps | AC loading: 17pf load, 8 ma drive and above/all slew |

Table 155 LPDDR-LVCMOS 1.8 V Calibrated Impedance Option

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | RODT_CAL | 75, 60, 50, 33, 25, 20 | : |

Table 159 LPDDR-LVCMOS 1.8 V AC Switching Characteristi cs for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers) (continued)

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | medium | 3.246 | 3.819 | 2.686 | 3.16 | 3.236 | 3.807 | 5.542 | 6.52 | 4.936 | 5.807 | ns |
| | medium_fast | 3.066 | 3.607 | 2.525 | 2.971 | 3.054 | 3.593 | 5.405 | 6.359 | 4.811 | 5.66 | ns |
| | fast | 3.046 | 3.584 | 2.513 | 2.957 | 3.034 | 3.57 | 5.401 | 6.353 | 4.803 | 5.651 | ns |
| 10 mA | slow | 3.498 | 4.115 | 2.878 | 3.386 | 3.481 | 4.096 | 6.046 | 7.113 | 5.444 | 6.404 | ns |
| | medium | 3.138 | 3.692 | 2.569 | 3.023 | 3.126 | 3.678 | 5.782 | 6.803 | 5.129 | 6.034 | ns |
| | medium_fast | 2.966 | 3.489 | 2.414 | 2.841 | 2.951 | 3.472 | 5.666 | 6.665 | 5.013 | 5.897 | ns |
| | fast | 2.945 | 3.464 | 2.401 | 2.826 | 2.93 | 3.448 | 5.659 | 6.658 | 5.003 | 5.886 | ns |
| 12 mA | slow | 3.417 | 4.02 | 2.807 | 3.303 | 3.401 | 4.002 | 6.083 | 7.156 | 5.464 | 6.428 | ns |
| | medium | 3.076 | 3.618 | 2.519 | 2.964 | 3.063 | 3.604 | 5.828 | 6.856 | 5.176 | 6.089 | ns |
| | medium_fast | 2.913 | 3.427 | 2.376 | 2.795 | 2.898 | 3.41 | 5.725 | 6.736 | 5.072 | 5.966 | ns |
| | fast | 2.894 | 3.405 | 2.362 | 2.78 | 2.879 | 3.388 | 5.715 | 6.724 | 5.064 | 5.957 | ns |
| 16 mA | slow | 3.366 | 3.96 | 2.751 | 3.237 | 3.348 | 3.939 | 6.226 | 7.324 | 5.576 | 6.56 | ns |
| | medium | 3.03 | 3.565 | 2.47 | 2.906 | 3.017 | 3.55 | 5.981 | 7.036 | 5.282 | 6.214 | ns |
| | medium_fast | 2.87 | 3.377 | 2.328 | 2.739 | 2.854 | 3.358 | 5.895 | 6.935 | 5.18 | 6.094 | ns |
| | fast | 2.853 | 3.357 | 2.314 | 2.723 | 2.837 | 3.338 | 5.889 | 6.929 | 5.177 | 6.09 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management).

## 2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

### 2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

Minimum and Maximum Input and Output Levels

Table 160 LVDS Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V | 3.3 V range |

Table 161 LVDS DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| DC Input voltage | $V_I$ | 0 | 2.925 | V | 2.5 V range |
| DC input voltage | $V_I$ | 0 | 3.45 | V | 3.3 V range |
| Input current high[1] | $I_{IH}$ (DC) | | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | | |

1. See Table 24, page 22.

Table 168 LVDS25 Receiver Characteristics fo r MSIOD I/O Bank (Input Buffers)

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | 1 | Std | Unit |
| None | 2.554 | 3.004 | ns |
| 100 | 2.549 | 2.999 | ns |

Table 169 LVDS25 Transmitter Characteri stics for MSIO I/O Bank (O utput and Tristate Buffers)

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| 2.136 | 2.513 | 2.416 | 2.842 | 2.402 | 2.825 | 2.423 | 2.85 | 2.409 | 2.833 | ns |

Table 170 LVDS25 Transmitter Characteristics for MSIO D I/O Bank (Output an d Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| No pre-emphasis | 1.61 | 1.893 | 1.749 | 2.058 | 1.735 | 2.041 | 1.897 | 2.231 | 1.866 | 2.195 | ns |
| Min pre-emphasis | 1.527 | 1.796 | 1.757 | 2.067 | 1.744 | 2.052 | 1.905 | 2.241 | 1.876 | 2.207 | ns |
| Med pre-emphasis | 1.496 | 1.76 | 1.765 | 2.077 | 1.751 | 2.06 | 1.914 | 2.252 | 1.884 | 2.216 | ns |

LVDS33 AC Switching Characteristics

Table 171 LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

| | $T_{PY}$ | | |
|---|---|---|---|
| On Die Termination (ODT) | 1 | Std | Unit |
| None | 2.572 | 3.025 | ns |
| 100 | 2.569 | 3.023 | ns |

Table 172 LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| 1.942 | 2.284 | 1.98 | 2.33 | 1.97 | 2.318 | 1.953 | 2.298 | 1.96 | 2.307 | ns |

AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 ºC, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V.

Table 210 RSDS AC Switching Characteristics fo r Receiver (for MSIO I/O Bank - Input Buffers)

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | 1 | Std | Unit |
| None | 2.855 | 3.359 | ns |
| 100 | 2.85 | 3.353 | ns |

Table 211 RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)

| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | 1 | Std | Unit |
| None | 2.602 | 3.061 | ns |
| 100 | 2.597 | 3.055 | ns |

Table 212 RSDS AC Switching Characteristics for Tran smitter (for MSIO I/O Bank - Output and Tristate Buffers)

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| 2.097 | 2.467 | 2.303 | 2.709 | 2.291 | 2.695 | 1.961 | 2.307 | 1.947 | 2.29 | ns |

Table 213 RSDS AC Switching Characteristics for Transmitte r (for MSIOD I/O Bank - Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| No pre-emphasis | 1.614 | 1.899 | 1.559 | 1.834 | 1.55 | 1.823 | 1.59 | 1.87 | 1.575 | 1.852 | ns |
| Min pre-emphasis | 1.604 | 1.887 | 1.742 | 2.05 | 1.728 | 2.032 | 1.889 | 2.222 | 1.858 | 2.185 | ns |
| Med pre-emphasis | 1.521 | 1.79 | 1.753 | 2.062 | 1.737 | 2.043 | 1.9 | 2.235 | 1.868 | 2.197 | ns |
| Max pre-emphasis | 1.492 | 1.754 | 1.762 | 2.073 | 1.745 | 2.052 | 1.91 | 2.247 | 1.876 | 2.206 | ns |

### 2.3.7.6 LVPECL

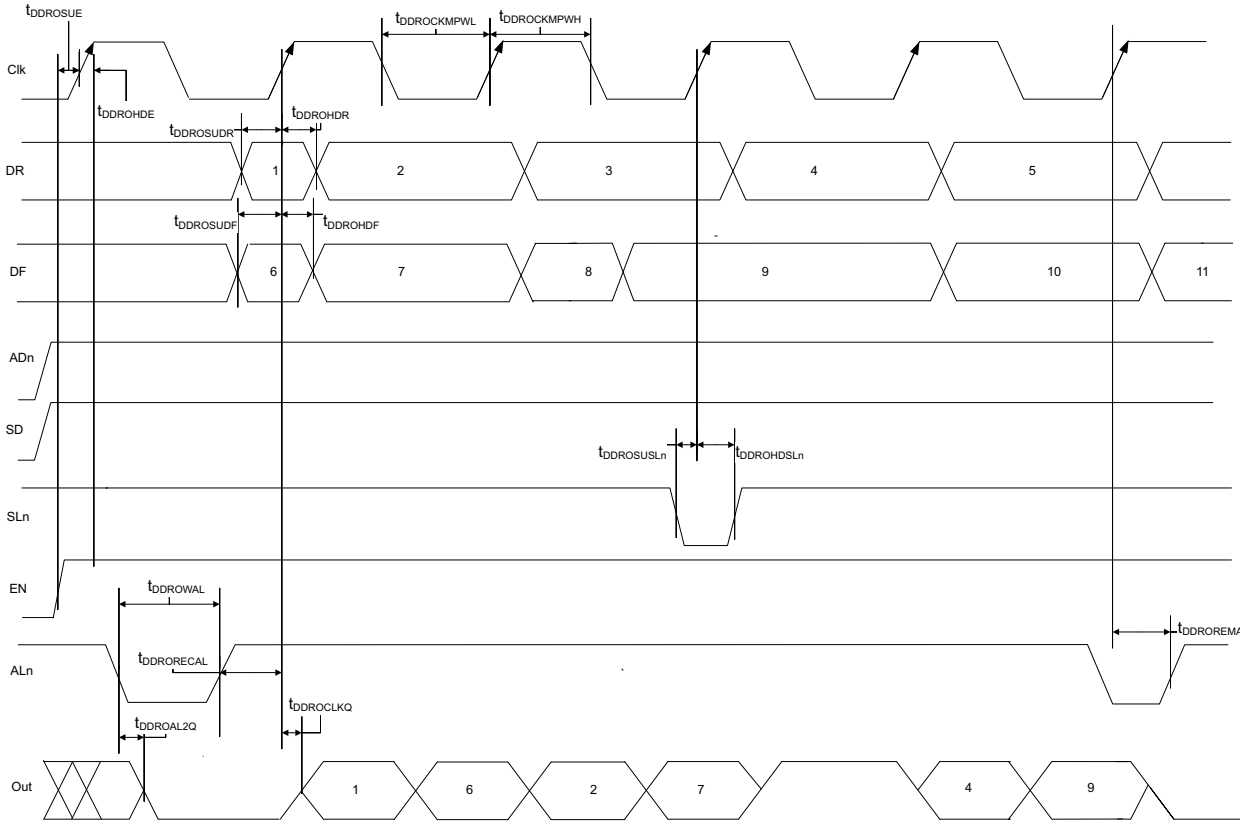
Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)

Table 214 LVPECL Recommended DC Op erating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V |

Figure 13 Output DDR Timing Diagram




### 2.3.9.5 Timing Characteristics

The following table lists the output DDR propagation delays in worst commercial-case conditions when $T_J$ = 85 ºC, $V_{DD}$ = 1.14 V.

Table 222 Output DDR Propagation Delays

| Symbol | Description | Measuring Nodes (from, to) | 1 | Std | Unit |
|---|---|---|---|---|---|
| $T_{DDROCLKQ}$ | Clock-to-out of DDR for output DDR | E, G | 0.263 | 0.309 | ns |
| $T_{DDROSUDF}$ | Data_F data setup for output DDR | F, E | 0.143 | 0.168 | ns |
| $T_{DDROSUDR}$ | Data_R data setup for output DDR | A, E | 0.19 | 0.223 | ns |
| $T_{DDROHDF}$ | Data_F data hold for output DDR | F, E | 0 | 0 | ns |
| $T_{DDROHDR}$ | Data_R data hold for output DDR | A, E | 0 | 0 | ns |
| $T_{DDROSUE}$ | Enable setup for input DDR | B, E | 0.419 | 0.493 | ns |
| $T_{DDROHE}$ | Enable hold for input DDR | B, E | 0 | 0 | ns |
| $T_{DDROSUSLN}$ | Synchronous load setup for input DDR | D, E | 0.196 | 0.231 | ns |
| $T_{DDROHSLN}$ | Synchronous load hold for input DDR | D, E | 0 | 0 | ns |
| $T_{DDROAL2Q}$ | Asynchronous load-to-out for output DDR | C, G | 0.528 | 0.621 | ns |
| $T_{DDROREMAL}$ | Asynchronous load removal time for output DDR | C, E | 0 | 0 | ns |
| $T_{DDRORECAL}$ | Asynchronous load recovery time for output DDR | C, E | 0.034 | 0.04 | ns |

## 2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when $T_J$ = 85 ℃, $V_{DD}$ = 1.14 V.

Table 225 150 Device Global Resource

| | | 1 | | Std | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Input low delay for global clock | $T_{RCKL}$ | 0.83 | 0.911 | 0.831 | 0.913 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.457 | 1.588 | 1.715 | 1.869 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.131 | | 0.154 | ns |

The following table lists the 090 device global resources in worst commercial-case conditions when $T_J$ = 85 ℃, $V_{DD}$ = 1.14 V.

Table 226 090 Device Global Resource

| | | 1 | | Std | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Input low delay for global clock | $T_{RCKL}$ | 0.835 | 0.888 | 0.833 | 0.886 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.405 | 1.489 | 1.654 | 1.752 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.084 | | 0.098 | ns |

The following table lists the 050 device global resources in worst commercial-case conditions when $T_J$ = 85 ℃, $V_{DD}$ = 1.14 V.

Table 227 050 Device Global Resource

| | | 1 | | Std | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Input low delay for global clock | $T_{RCKL}$ | 0.827 | 0.897 | 0.826 | 0.896 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.419 | 1.53 | 1.671 | 1.8 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.111 | | 0.129 | ns |

The following table lists the 025 device global resources in worst commercial-case conditions when $T_J$ = 85 ℃, $V_{DD}$ = 1.14 V.

Table 228 025 Device Global Resource

| | | 1 | | Std | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Input low delay for global clock | $T_{RCKL}$ | 0.747 | 0.799 | 0.745 | 0.797 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.294 | 1.378 | 1.522 | 1.621 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.084 | | 0.099 | ns |

Table 232 RAM1K18 Dual-Port Mode for Depth ×Width Configuration 2K ×9 (continued)

| | | 1 | | Std | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Address setup time | $T_{ADDRSU}$ | 0.475 | | 0.559 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.336 | | 0.395 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.529 | | 1.799 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.485 | | 0.57 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.514 | | 1.781 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | 0.279 | | 0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.415 | | 0.488 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 dual-port mode for depth ×width configuration 4K ×4 in worst commercial-case conditions when $T_J$ = 85 ℃, $V_{DD}$ = 1.14 V.

Table 233 RAM1K18 Dual-Port Mode for Depth ×Width Configuration 4K ×4

| | | 1 | | Std | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |

The following table lists the RAM1K18 dual-port mode for depth ×width configuration 8K ×2 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

Table 234 RAM1K18 Dual-Port Mode for Depth ×Width Configuration 8K ×2

| | | 1 | | Std | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.32 | | 0.377 | ns |
| Read access time without pipeline register | | | 2.272 | | 2.673 | ns |
| Access time with feed-through write timing | | | 1.511 | | 1.778 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.612 | | 0.72 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.33 | | 0.388 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.511 | | 1.778 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.529 | | 0.622 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.528 | | 1.797 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | 0.279 | | 0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.488 | | 0.574 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 two-port mode for depth ×width configuration 512 ×36 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

Table 236 RAM1K18 Two-Port Mode for Depth ×Width Configuration 512 ×36

| | | 1 | | Std | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.334 | | 0.393 | ns |
| Read access time without pipeline register | | | 2.25 | | 2.647 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.313 | | 0.368 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.337 | | 0.396 | | ns |
| Data hold time | $T_{DHD}$ | 0.111 | | 0.13 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.201 | | 0.237 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.25 | | 2.647 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.449 | | 0.528 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.167 | | 0.197 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.506 | | 1.772 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | 0.279 | | 0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.39 | | 0.458 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.242 | | 0.285 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

Table 239 µSRAM (RAM128x9) in 128 ×9 Mode (continued)

| | | 1 | | Std | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | 0.023 | | 0.027 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.835 | | 0.982 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.115 | | 0.135 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.15 | | 0.177 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.128 | | 0.15 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | 0.026 | | 0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 128 ×8 mode in worst commercial-case conditions when $T_J$ = 85 ℃, $V_{DD}$ = 1.14 V.

Table 240 µSRAM (RAM128x8) in 128 ×8 Mode

| | | 1 | | Std | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | 1.677 | | 1.973 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.856 | | 2.184 | | ns |

Table 265 Programming Times with 100 kHz, 25 MH z. and 12.5 MHz SPI Clock Rates (Fabric Only)

| | Auto Programming | Auto Up date | Programming Recovery | |
|---|---|---|---|---|
| M2S/M2GL Device | 100 kHz | 25 MHz | 12.5 MHz | Unit |
| 005 | 69 | 49 | 50 | Sec |
| 010 | 99 | 57 | 57 | Sec |
| 025 | 150 | 64 | 63 | Sec |
| 050 | 55[1] | Not Supported | Not Supported | Sec |
| 060 | 313 | 105 | 104 | Sec |
| 090 | 449 | 131 | 130 | Sec |
| 150 | 730 | 179 | 183 | Sec |

1. Auto programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

Table 266 Programming Times with 100 kHz, 25 MH z. and 12.5 MHz SPI Clock Rates (eNVM Only)

| | Auto Programming | Auto Up date | Programming Recovery | |
|---|---|---|---|---|
| M2S/M2GL Device | 100 kHz | 25 MHz | 12.5 MHz | Unit |
| 005 | 63 | 70 | 71 | Sec |
| 010 | 108 | 109 | 109 | Sec |
| 025 | 109 | 107 | 108 | Sec |
| 050 | 107 | Not Supported | Not Supported | Sec |
| 060 | 100 | 108 | 108 | Sec |
| 090 | 176 | 184 | 184 | Sec |
| 150 | 183 | 183 | 183 | Sec |

Table 267 Programming Times with 100 kHz, 25 MHz. and 12.5 MHz SPI Clock Rates (Fabric and eNVM)

| | Auto Programming | Auto Up date | Programming Recovery | |
|---|---|---|---|---|
| M2S/M2GL Device | 100 kHz | 25 MHz | 12.5 MHz | Unit |
| 005 | 109 | 89 | 88 | Sec |
| 010 | 183 | 135 | 135 | Sec |
| 025 | 251 | 142 | 143 | Sec |
| 050 | 134 | Not Supported | Not Supported | Sec |
| 060 | 390 | 183 | 180 | Sec |
| 090 | 604 | 283 | 282 | Sec |
| 150 | 889 | 331 | 332 | Sec |

## 2.3.22 JTAG

Table 284 JTAG 1532 for 005, 010, 025, and 050 Devices

| | | 005 | | 010 | | 025 | | 050 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | 1 | Std | 1 | Std | 1 | Std | 1 | Std | |
| Clock to Q (data out) | $T_{TCK2Q}$ | 7.47 | 8.79 | 7.73 | 9.09 | 7.75 | 9.12 | 7.89 | 9.28 | ns |
| Reset to Q (data out) | $T_{RSTB2Q}$ | 7.65 | 9 | 6.43 | 7.56 | 6.13 | 7.21 | 7.40 | 8.70 | ns |
| Test data input setup time | $T_{DISU}$ | 1.05 | 0.89 | 0.69 | 0.59 | 0.67 | 0.57 | 0.30 | 0.25 | ns |
| Test data input hold time | $T_{DIHD}$ | 2.38 | 2.8 | 2.38 | 2.8 | 2.42 | 2.85 | 2.09 | 2.45 | ns |
| Test mode select setup time | $T_{TMSSU}$ | 0.73 | 0.62 | 1.03 | 1.21 | 1.1 | 0.94 | 0.28 | 0.33 | ns |
| Test mode select hold time | $T_{TMDHD}$ | 1.36 | 1.6 | 1.43 | 1.68 | 1.93 | 2.27 | 0.16 | 0.19 | ns |
| ResetB removal time | $T_{TRSTREM}$ | 0.77 | 0.65 | 1.08 | 0.92 | 1.33 | 1.13 | 0.45 | 0.38 | ns |
| ResetB recovery time | $T_{TRSTREC}$ | 0.76 | 0.65 | 1.07 | 0.91 | 1.34 | 1.14 | 0.45 | 0.38 | ns |
| TCK maximum frequency | $F_{TCKMAX}$ | 25 | 21.25 | 25 | 21.25 | 25 | 21.25 | 25.00 | 21.25 | MHz |

Table 285 JTAG 1532 for 060, 090, and 150 Devices

| | | 060 | | 090 | | 150 | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | 1 | Std | 1 | Std | 1 | Std | Unit |
| Clock to Q (data out) | $T_{TCK2Q}$ | 8.38 | 9.86 | 8.96 | 10.54 | 8.66 | 10.19 | ns |
| Reset to Q (data out) | $T_{RSTB2Q}$ | 8.54 | 10.04 | 7.75 | 9.12 | 8.79 | 10.34 | ns |
| Test data input setup time | $T_{DISU}$ | 1.18 | 1 | 1.31 | 1.11 | 0.96 | 0.82 | ns |
| Test data input hold time | $T_{DIHD}$ | 2.52 | 2.97 | 2.68 | 3.15 | 2.57 | 3.02 | ns |
| Test mode select setup time | $T_{TMSSU}$ | 0.97 | 0.83 | 1.02 | 0.87 | 0.53 | 0.45 | ns |
| Test mode select hold time | $T_{TMDHD}$ | 1.7 | 2 | 1.67 | 1.96 | 1.02 | 1.2 | ns |
| ResetB removal time | $T_{TRSTREM}$ | 1.21 | 1.03 | 0.76 | 0.65 | 1.03 | 0.88 | ns |
| ResetB recovery time | $T_{TRSTREC}$ | 1.21 | 1.03 | 0.77 | 0.65 | 1.03 | 0.88 | ns |
| TCK maximum frequency | $F_{TCKMAX}$ | 25 | 21.25 | 25 | 21.25 | 25 | 21.25 | MHz |

## 2.3.23 System Controller SPI Characteristics

The following table lists the IGLOO2 DEVRST_N to functional times in worst-case industrial conditions when $T_J$ = 100 ºC, $V_{DD}$ = 1.14 V.

Table 292 DEVRST_N to Functional Times for IGLOO2

| | | | | Maximum Power-up to Functional Time for IGLOO2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | From | To | Description | 005 | 010 | 025 | 050 | 060 | 090 | 150 |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 114 | 116 | 113 | 113 | 115 | 115 | 114 |
| $T_{DEVRST2OUT}$ | DEVRST_N | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 314 | 353 | 314 | 307 | 343 | 341 | 341 |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 200 | 238 | 201 | 195 | 230 | 229 | 227 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |