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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 50K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-LFBGA
Supplier Device Package	400-VFBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s050t-vf400">https://www.e-xfl.com/product-detail/microchip-technology/m2s050t-vf400</a>

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- Added [Table 244](#), page 94 and [Table 256](#), page 99 (SAR 73971).
- Updated the [SerDes Electrical and Timing AC and DC Characteristics](#), page 121 (SAR 71171).
- Added the [DEVRST\\_N Characteristics](#), page 116 (SAR 64100, 72103).
- Added [Table 298](#), page 122 (SAR 71897).
- Updated [Table 25](#), page 22, [Table 26](#), page 23, and [Table 27](#), page 23 (SAR 74570).
- Added 060 devices in [Table 277](#), page 107, [Table 278](#), page 108, and [Table 279](#), page 108 (SAR 57898).
- Updated duty cycle parameter of crystal in [Table 280](#), page 109 and [Table 281](#), page 109 (SAR 57898).
- Added 32 KHz mode PLL acquisition time in [Table 282](#), page 110 (SAR 68281).
- Updated [Table 293](#), page 119 for 060 devices (SAR 57828).
- Updated [Table 297](#), page 122 for CID value (SAR 70878).

## 1.4 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated [Table 11](#), page 12 (SAR 69218).
- Updated [Table 12](#), page 13 (SAR 69218).
- Updated [Table 283](#), page 111 (SAR 69000).

## 1.5 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated [Table 1](#), page 4(SAR 68620).

## 1.6 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated [Table 5](#), page 7 (SAR 65949).
- Updated [Table 9](#), page 10 (SAR 62995).
- Updated [Table 123](#), page 47 and [Table 133](#), page 49 (SAR 67210).
- Added [Embedded NVM \(eNVM\) Characteristics](#), page 104 (SAR 52509).
- Updated [Table 277](#), page 107 (SAR 64855).
- Updated [Table 282](#), page 110 (SAR 65958 and SAR 56666).
- Added [DDR Memory Interface Characteristics](#), page 120 (SAR 66223).
- Added [SFP Transceiver Characteristics](#), page 120 (SAR 63105).
- Updated [Table 302](#), page 123 and [Table 309](#), page 129 (SAR 66314).

## 1.7 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated [Table 1](#), page 4.
- Updated [Table 4](#), page 6 for  $T_J$  symbol information.
- Updated [Table 5](#), page 7 (SAR 63109).
- Updated [Table 9](#), page 10.
- Updated [Table 282](#), page 110 (SAR 62012).
- Added [Table 290](#), page 116 (SAR 64100).
- Added [Table 306](#), page 128, [Table 307](#), page 128 (SAR 50424).

## 1.8 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Updated [Table 1](#), page 4. Changed the Status of 090 devices to "Production" (SAR 62750).
- Updated [Figure 10](#), page 70. Removed inverter bubble from DDR\_IN latch (SAR 61418).
- Updated [SerDes Electrical and Timing AC and DC Characteristics](#), page 121 (SAR 62836).

**Table 4 • Recommended Operating Conditions (continued)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
3.3 V DC supply voltage	$V_{DDIX}$	3.15	3.3	3.45	V	
LVDS differential I/O	$V_{DDIX}$	2.375	2.5	3.45	V	
B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O	$V_{DDIX}$	2.375	2.5	2.625	V	
LVPECL differential I/O	$V_{DDIX}$	3.15	3.3	3.45	V	
Reference voltage supply for FDDR (Bank0) and MDDR (Bank5)	$V_{REFX}$	0.49 × $V_{DDIX}$	0.5 × $V_{DDIX}$	0.51 × $V_{DDIX}$	V	
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$ .	$V_{PPNVM}$	2.375 3.15	2.5 3.3	2.625 3.45	V	2.5 V range 3.3 V range

1. Programming at Industrial temperature range is available only with  $V_{PP} = 3.3$  V.

**Note:** Power supply ramps must all be strictly monotonic, without plateaus.

**Table 5 • FPGA Operating Limits**

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Digest Temperature	Digest Cycles	Retention (Biased/Unbiased)
Commercial	FPGA	Min $T_J = 0$ °C Max $T_J = 85$ °C	Min $T_J = 0$ °C Max $T_J = 85$ °C	500	Min $T_J = 0$ °C Max $T_J = 85$ °C	2000	20 years
Industrial <sup>1</sup>	FPGA	Min $T_J = -40$ °C Max $T_J = 100$ °C	Min $T_J = -40$ °C Max $T_J = 100$ °C	500	Min $T_J = -40$ °C Max $T_J = 100$ °C	2000	20 years

1. Programming at Industrial temperature range is available only with  $V_{PP} = 3.3$  V.

**Note:** The retention specification is defined as the total number of programming and digest cycles. For example, 20 years of retention after 500 programming cycles.

**Note:** The digest cycle specification is 2000 digest cycles for every program cycle with a maximum of 500 programming cycles.

**Note:** If your product qualification requires accelerated programming cycles, see [Microsemi SoC Products Quality and Reliability Report](#) about recommended methodologies.

The following table lists the embedded operating flash limits.

**Table 6 • Embedded Operating Flash Limits**

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Commercial	Embedded flash	Min $T_J = 0\text{ }^\circ\text{C}$ Max $T_J = 85\text{ }^\circ\text{C}$	Min $T_J = 0\text{ }^\circ\text{C}$ Max $T_J = 85\text{ }^\circ\text{C}$	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
				< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years
Industrial	Embedded flash	Min $T_J = -40\text{ }^\circ\text{C}$ Max $T_J = 100\text{ }^\circ\text{C}$	Min $T_J = -40\text{ }^\circ\text{C}$ Max $T_J = 100\text{ }^\circ\text{C}$	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
				< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years

**Note:** If your product qualification requires accelerated programming cycles, see [Microsemi SoC Products Quality and Reliability Report](#) about recommended methodologies.

**Table 7 • Device Storage Temperature and Retention**

Product Grade	Storage Temperature ( $T_{stg}$ )	Retention
Commercial	Min $T_J = 0\text{ }^\circ\text{C}$ Max $T_J = 85\text{ }^\circ\text{C}$	20 years
Industrial	Min $T_J = -40\text{ }^\circ\text{C}$ Max $T_J = 100\text{ }^\circ\text{C}$	20 years

**Table 8 • High Temperature Data Retention (HTR) Lifetime**

$T_J$ (C)	HTR Lifetime <sup>1</sup> (yrs)
90	20.5
95	20.5
100	20.5
105	17.0
110	15.0
115	13.0
120	11.5
125	10.0
130	8.0
135	6.0
140	4.5
145	3.0
150	1.5

1. HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

### 2.3.5.5 Detailed I/O Characteristics

**Table 24 • Input Capacitance, Leakage Current, and Ramp Time**

Symbol	Description	Maximum	Unit	Conditions
$C_{IN}$	Input capacitance	10	pF	
$I_{IL}$ (dc)	Input current low (Applicable to HSTL/SSTL inputs only)	400	$\mu$ A	$V_{DDI} = 2.5$ V
		500	$\mu$ A	$V_{DDI} = 1.8$ V
		600	$\mu$ A	$V_{DDI} = 1.5$ V <sup>1</sup>
	Input current low (Applicable to all other digital inputs)	10	$\mu$ A	
$I_{IH}$ (dc)	Input current high (Applicable to HSTL/SSTL inputs only)	400	$\mu$ A	$V_{DDI} = 2.5$ V
		500	$\mu$ A	$V_{DDI} = 1.8$ V
		600	$\mu$ A	$V_{DDI} = 1.5$ V <sup>1</sup>
	Input current high (Applicable to all other digital inputs)	10	$\mu$ A	
$T_{RAMPIN}$ <sup>2</sup>	Input ramp time (Applicable to all digital inputs)	50	ns	

1. Applicable when I/O pair is programmed with an HSTL/SSTL I/O type on IOP and an un-terminated I/O type (LVCMOS, for example) on ION pad.
2. Voltage ramp must be monotonic.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of DDRIO I/O bank at  $V_{OH}/V_{OL}$  Level.

**Table 25 • I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank**

$V_{DDI}$ Domain	R(WEAK PULL-UP) at $V_{OH}$ ( $\Omega$ )		R(WEAK PULL-DOWN) at $V_{OL}$ ( $\Omega$ )	
	Min	Max	Min	Max
2.5 V <sup>1, 2</sup>	10K	17.8K	9.98K	18K
1.8 V <sup>1, 2</sup>	10.3K	19.1K	10.3K	19.5K
1.5 V <sup>1, 2</sup>	10.6K	20.2K	10.6K	21.1K
1.2 V <sup>1, 2</sup>	11.1K	22.7K	11.2K	24.6K

1.  $R(\text{WEAK PULL-DOWN}) = (V_{OLspec})/I(\text{WEAK PULL-DOWN MAX})$ .
2.  $R(\text{WEAK PULL-UP}) = (V_{DDImax} - V_{OHspec})/I(\text{WEAK PULL-UP MIN})$ .

**Table 57 • LVCMOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	Medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	Medium fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	Fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	Slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	Medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	Medium fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	Fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	Slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	Medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	Medium fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	Fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	Slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns
	Medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	Medium fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	Fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	Slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	Medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	Medium fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	Fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	Slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	Medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	Medium fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	Fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	Slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	Medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	Medium fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	Fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.



**Table 58 • LVCMOS 1.8 V Transmitter Characteristics for MSIO I/O Bank**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.441	4.047	4.165	4.9	4.413	5.192	4.891	5.755	5.138	6.044	ns
4 mA	Slow	3.218	3.786	3.642	4.284	3.941	4.636	5.665	6.665	5.568	6.551	ns
6 mA	Slow	3.141	3.694	3.501	4.118	3.823	4.498	6.587	7.75	6.032	7.096	ns
8 mA	Slow	3.165	3.723	3.319	3.904	3.654	4.298	6.898	8.115	6.216	7.313	ns
10 mA	Slow	3.202	3.767	3.278	3.857	3.616	4.254	7.25	8.529	6.435	7.571	ns
12 mA	Slow	3.277	3.855	3.175	3.736	3.519	4.139	7.392	8.697	6.538	7.692	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 59 • LVCMOS 1.8 V Transmitter Characteristics for MSIOD I/O Bank**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.725	3.206	3.316	3.901	3.484	4.099	5.204	6.123	4.997	5.88	ns
4 mA	Slow	2.242	2.638	2.777	3.267	2.947	3.466	5.729	6.74	5.448	6.41	ns
6 mA	Slow	1.995	2.347	2.466	2.901	2.63	3.094	6.372	7.496	5.987	7.043	ns
8 mA	Slow	2.001	2.354	2.44	2.87	2.6	3.058	6.633	7.804	6.193	7.286	ns
10 mA	Slow	2.025	2.382	2.312	2.719	2.47	2.906	6.94	8.165	6.412	7.544	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.9 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

#### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 60 • LVCMOS 1.5 V DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>DDI</sub>	1.425	1.5	1.575	V

**Table 61 • LVCMOS 1.5 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high for (MSIOD and DDRIO I/O banks)	V <sub>IH</sub> (DC)	0.65 × V <sub>DDI</sub>	1.575	V
DC input logic high (for MSIO I/O bank)	V <sub>IH</sub> (DC)	0.65 × V <sub>DDI</sub>	3.45	V
DC input logic low	V <sub>IL</sub> (DC)	-0.3	0.35 × V <sub>DDI</sub>	V
Input current high <sup>1</sup>	I <sub>IH</sub> (DC)			-
Input current low <sup>1</sup>	I <sub>IL</sub> (DC)			-

1. See Table 24, page 22.

**Table 82 • LVCMOS 1.2 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
	-1	-Std	-1	-Std	
None	4.154	4.887	4.114	4.84	ns
50	6.918	8.139	6.806	8.008	ns
75	5.613	6.603	5.533	6.509	ns
150	4.716	5.549	4.657	5.479	ns

**Table 83 • LVCMOS 1.2 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	6.713	7.897	5.362	6.308	6.723	7.909	7.233	8.51	6.375	7.499	ns
	Medium	5.912	6.955	4.616	5.43	5.915	6.959	6.887	8.102	6.009	7.069	ns
	Medium fast	5.5	6.469	4.231	4.978	5.5	6.471	6.672	7.849	5.835	6.865	ns
	Fast	5.462	6.426	4.194	4.935	5.463	6.427	6.646	7.819	5.828	6.857	ns
4 mA	Slow	6.109	7.186	4.708	5.539	6.098	7.174	8.005	9.418	7.033	8.274	ns
	Medium	5.355	6.299	4.034	4.746	5.338	6.28	7.637	8.985	6.672	7.849	ns
	Medium fast	4.953	5.826	3.685	4.336	4.932	5.802	7.44	8.752	6.499	7.646	ns
	Fast	4.911	5.777	3.658	4.303	4.89	5.754	7.427	8.737	6.488	7.632	ns
6 mA	Slow	5.89	6.929	4.506	5.301	5.874	6.911	8.337	9.808	7.315	8.605	ns
	Medium	5.176	6.089	3.862	4.543	5.155	6.065	7.986	9.394	6.943	8.168	ns
	Medium fast	4.792	5.637	3.523	4.145	4.765	5.606	7.808	9.186	6.775	7.97	ns
	Fast	4.754	5.593	3.486	4.101	4.728	5.563	7.777	9.149	6.769	7.963	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 84 • LVCMOS 1.2 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	6.746	7.937	7.458	8.774	8.172	9.614	9.867	11.608	8.393	9.874	ns
4 mA	Slow	7.068	8.315	6.678	7.857	7.474	8.793	10.986	12.924	9.043	10.638	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 144 • LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	$V_{DIFF}$	$0.6 \times V_{DDI}$		V
AC differential cross point voltage	$V_x$	$0.4 \times V_{DDI}$	$0.6 \times V_{DDI}$	V

**Table 145 • LPDDR AC Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	$D_{MAX}$	400	Mbps	AC loading: per JEDEC specifications

**Table 146 • LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	$R_{REF}$	20, 42	$\Omega$	Reference resistor = 150 $\Omega$
Effective impedance value (ODT)	$R_{TT}$	50, 70, 150	$\Omega$	Reference resistor = 150 $\Omega$

**Table 147 • LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	0.9	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Reference resistance for data test path for LPDDR ( $T_{DP}$ )	$R_{TT\_TEST}$	50	$\Omega$
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	$\Omega$

**AC Switching Characteristics**

Worst-case commercial conditions:  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ , worst-case  $V_{DDI}$ .

**Table 148 • LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes**

	On-Die Termination (ODT)	$T_{PY}$		Unit
		-1	-Std	
Pseudo differential	None	1.568	1.845	ns
True differential	None	1.588	1.869	ns

**Table 149 • LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ENZL}$		$T_{ENZH}$		$T_{ENHZ}$		$T_{ENLZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns
Differential	2.396	2.819	2.764	3.252	2.764	3.252	2.255	2.653	2.255	2.653	ns

**Table 150 • LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

	$T_{DP}$		$T_{ENZL}$		$T_{ENZH}$		$T_{ENHZ}$		$T_{ENLZ}$		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns
Differential	2.298	2.703	2.288	2.692	2.288	2.692	2.593	3.051	2.593	3.051	ns

**Minimum and Maximum DC/AC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode**

**Table 151 • LPDDR-LVCMOS 1.8 V Mode Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DDI}$	1.710	1.8	1.89	V

**Table 152 • LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	$V_{IH}$ (DC)	$0.65 \times V_{DDI}$	1.89	V
DC input logic high (for MSIO I/O bank)	$V_{IH}$ (DC)	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	$V_{IL}$ (DC)	-0.3	$0.35 \times V_{DDI}$	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>1</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

**Table 153 • LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	$V_{OH}$	$V_{DDI} - 0.45$		V
DC output logic low	$V_{OL}$		0.45	V

**Table 154 • LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	400	Mbps	AC loading: 17pf load, 8 ma drive and above/all slew

**Table 155 • LPDDR-LVCMOS 1.8 V Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 33, 25, 20	$\Omega$

**Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers) (continued)**

	medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	medium_fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	medium_fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	medium_fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	medium_fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO management).

### 2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

#### 2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

##### Minimum and Maximum Input and Output Levels

**Table 160 • LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V	2.5 V range
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V	3.3 V range

**Table 161 • LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit	Conditions
DC Input voltage	$V_I$	0	2.925	V	2.5 V range
DC input voltage	$V_I$	0	3.45	V	3.3 V range
Input current high <sup>1</sup>	$I_{IH}$ (DC)				
Input current low <sup>1</sup>	$I_{IL}$ (DC)				

1. See Table 24, page 22.

**Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 (continued)**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Address setup time	$T_{ADDRSU}$	0.475		0.559		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.336		0.395		ns
Data hold time	$T_{DHD}$	0.082		0.096		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		1.529		1.799	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.485		0.57		ns
Read enable hold time	$T_{RDEHD}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$		1.514		1.781	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.415		0.488		ns
Write enable hold time	$T_{WEHD}$	0.048		0.057		ns
Maximum frequency	$F_{MAX}$		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 233 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 8K × 2 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 234 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register				0.32	0.377	ns
Read access time without pipeline register	$T_{CLK2Q}$			2.272	2.673	ns
Access time with feed-through write timing				1.511	1.778	ns
Address setup time	$T_{ADDRSU}$	0.612		0.72		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.33		0.388		ns
Data hold time	$T_{DHD}$	0.082		0.096		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$			1.511	1.778	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.529		0.622		ns
Read enable hold time	$T_{RDEHD}$	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$			1.528	1.797	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.488		0.574		ns
Write enable hold time	$T_{WEHD}$	0.048		0.057		ns
Maximum frequency	$F_{MAX}$			400	340	MHz

The following table lists the RAM1K18 – two-port mode for depth × width configuration 512 × 36 in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 236 • RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36**

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	$T_{CY}$	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	$T_{PLCY}$	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.334		0.393	ns
Read access time without pipeline register			2.25		2.647	ns
Address setup time	$T_{ADDRSU}$	0.313		0.368		ns
Address hold time	$T_{ADDRHD}$	0.274		0.322		ns
Data setup time	$T_{DSU}$	0.337		0.396		ns
Data hold time	$T_{DHD}$	0.111		0.13		ns
Block select setup time	$T_{BLKSU}$	0.207		0.244		ns
Block select hold time	$T_{BLKHD}$	0.201		0.237		ns
Block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.25		2.647	ns
Block select minimum pulse width	$T_{BLKMPW}$	0.186		0.219		ns
Read enable setup time	$T_{RDESU}$	0.449		0.528		ns
Read enable hold time	$T_{RDEHD}$	0.167		0.197		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	$T_{R2Q}$		1.506		1.772	ns
Asynchronous reset removal time	$T_{RSTREM}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTREC}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	$T_{RSTMPW}$	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTSU}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTHD}$	0.036		0.043		ns
Write enable setup time	$T_{WESU}$	0.39		0.458		ns
Write enable hold time	$T_{WEHD}$	0.242		0.285		ns
Maximum frequency	$F_{MAX}$		400		340	MHz



**Table 248 • 2 Step IAP Programming (eNVM Only)**

<b>M2S/M2GL</b>					
<b>Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	137536	2	37	5	Sec
010	274816	4	76	11	Sec
025	274816	4	78	10	Sec
050	278528	3	85	9	Sec
060	268480	5	76	22	Sec
090	544496	10	152	43	Sec
150	544496	10	153	44	Sec

**Table 249 • 2 Step IAP Programming (Fabric and eNVM)**

<b>M2S/M2GL</b>					
<b>Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	439296	6	56	11	Sec
010	842688	11	100	21	Sec
025	1497408	19	113	32	Sec
050	2695168	32	136	48	Sec
060	2686464	43	137	70	Sec
090	4190208	68	236	115	Sec
150	6682768	109	286	162	Sec

**Table 250 • SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

<b>M2S/M2GL</b>					
<b>Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	302672	6	19	8	Sec
010	568784	10	26	14	Sec
025	1223504	21	39	29	Sec
050	2424832	39	60	50	Sec
060	2418896	44	65	54	Sec
090	3645968	66	90	79	Sec
150	6139184	108	140	128	Sec

**Table 251 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

<b>M2S/M2GL</b>					
<b>Device</b>	<b>Image size Bytes</b>	<b>Authenticate</b>	<b>Program</b>	<b>Verify</b>	<b>Unit</b>
005	137536	3	42	4	Sec
010	274816	4	82	7	Sec
025	274816	4	82	8	Sec
050	278528	4	80	8	Sec
060	268480	6	80	8	Sec
090	544496	10	157	15	Sec

**Table 259 • 2 Step IAP Programming (Fabric Only)**

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	302672	4	39	6	Sec	
010	568784	7	45	12	Sec	
025	1223504	14	55	23	Sec	
050	2424832	29	74	40	Sec	
060	2418896	39	83	50	Sec	
090	3645968	60	106	73	Sec	
150	6139184	100	154	120	Sec	

**Table 260 • 2 Step IAP Programming (eNVM Only)**

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	137536	2	59	5	Sec	
010	274816	4	98	11	Sec	
025	274816	4	100	10	Sec	
050	2,78,528	3	107	9	Sec	
060	268480	5	98	22	Sec	
090	544496	10	174	43	Sec	
150	544496	10	175	44	Sec	

**Table 261 • 2 Step IAP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	439296	6	78	11	Sec	
010	842688	11	122	21	Sec	
025	1497408	19	135	32	Sec	
050	2695168	32	158	48	Sec	
060	2686464	43	159	70	Sec	
090	4190208	68	258	115	Sec	
150	6682768	109	308	162	Sec	

**Table 265 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	69	49	50	Sec
010	99	57	57	Sec
025	150	64	63	Sec
050	55 <sup>1</sup>	Not Supported	Not Supported	Sec
060	313	105	104	Sec
090	449	131	130	Sec
150	730	179	183	Sec

1. Auto programming in 050 device is done through SC\_SPI, and SPI CLK is set to 6.25 MHz.

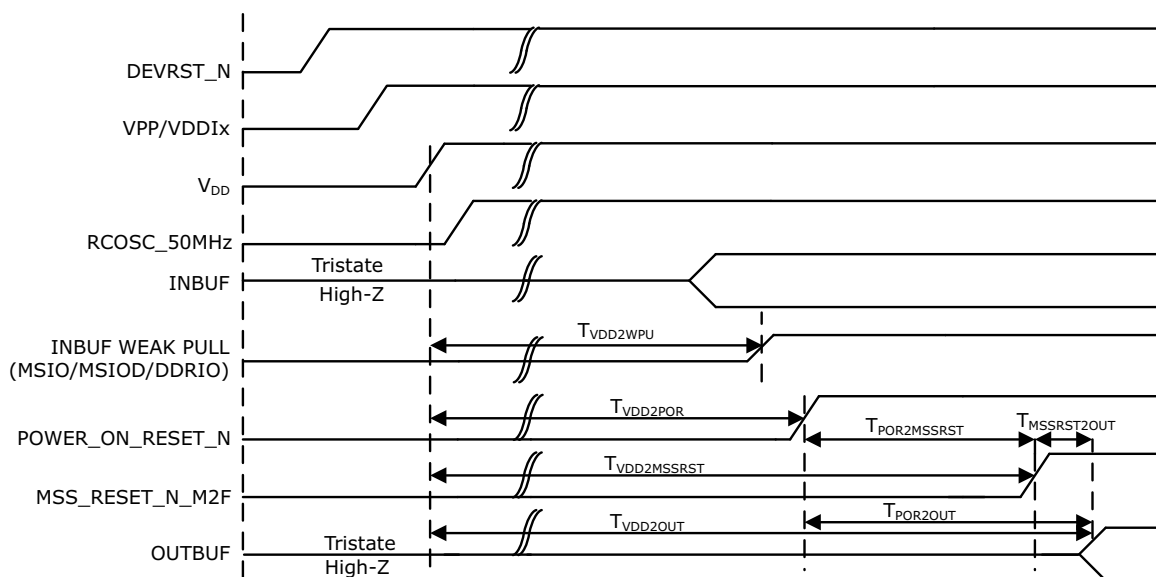
**Table 266 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	63	70	71	Sec
010	108	109	109	Sec
025	109	107	108	Sec
050	107	Not Supported	Not Supported	Sec
060	100	108	108	Sec
090	176	184	184	Sec
150	183	183	183	Sec

**Table 267 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	109	89	88	Sec
010	183	135	135	Sec
025	251	142	143	Sec
050	134	Not Supported	Not Supported	Sec
060	390	183	180	Sec
090	604	283	282	Sec
150	889	331	332	Sec

Figure 17 • Power-up to Functional Timing Diagram for SmartFusion2



The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 289 • Power-up to Functional Times for IGLOO2

Symbol	From	To	Description	Maximum Power-up to Functional Time for IGLOO2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	114	114	113	114	114	114
$T_{VDD2OUT}$	$V_{DD}$	Output available at I/O	$V_{DD}$ at its minimum threshold level to output	2587	2600	2607	2558	2591	2600	2699
$T_{VDD2POR}$	$V_{DD}$	POWER_ON_RESET_N	$V_{DD}$ at its minimum threshold level to fabric	2474	2486	2493	2445	2477	2486	2585
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

**Note:** For more information about power-up times, see [UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide](#).

## 2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 308 • MMUART Characteristics**

Parameter	Description	-1	-Std	Unit
FMMUART_REF_CLK	Internally sourced MMUART reference clock frequency.	166	142	MHz
BAUDMMUARTTx	Maximum transmit baud rate	10.375	8.875	Mbps
BAUDMMUARTRx	Maximum receive baud rate	10.375	8.875	Mbps

## 2.3.35 IGLOO2 Specifications

### 2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 309 • Maximum Frequency for HPMS Main Clock**

Symbol	Description	-1	-Std	Unit
HPMS_CLK	Maximum frequency for the HPMS main clock	166	142	MHz

### 2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI\_0\_CLK. For timing parameter definitions, see [Figure 23](#), page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 310 • SPI Characteristics for All Devices**

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12			ns	
	SPI_[0 1]_CLK = PCLK/4	24.1			ns	
	SPI_[0 1]_CLK = PCLK/8	48.2			ns	
	SPI_[0 1]_CLK = PCLK/16	0.1			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/32	0.19			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/64	0.39			$\mu\text{s}$	
SPI_[0 1]_CLK = PCLK/128	0.77			$\mu\text{s}$		