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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 90K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s090t-1fg676">https://www.e-xfl.com/product-detail/microchip-technology/m2s090t-1fg676</a>

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**Table 15 • Inrush Currents at Power up,  $-40\text{ }^{\circ}\text{C} \leq T_J \leq 100\text{ }^{\circ}\text{C}$  – Typical Process**

Power Supplies	Voltage (V)	005	010	025	050	060	090	150	Unit
$V_{DD}$	1.26	25	32	38	48	45	77	109	mA
$V_{PP}$	3.46	33	49	36	180	13	36	51	mA
$V_{DDI}$	2.62	134	141	161	187	93	272	388	mA
Number of banks		7	8	8	10	10	9	19	

### 2.3.3 Average Fabric Temperature and Voltage Derating Factors

The following table lists the average temperature and voltage derating factors for fabric timing delays normalized to  $T_J = 85\text{ }^{\circ}\text{C}$ , in worst-case  $V_{DD} = 1.14\text{ V}$ .

**Table 16 • Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays**

Array Voltage $V_{DD}$ (V)	$-40\text{ }^{\circ}\text{C}$	$0\text{ }^{\circ}\text{C}$	$25\text{ }^{\circ}\text{C}$	$70\text{ }^{\circ}\text{C}$	$85\text{ }^{\circ}\text{C}$	$100\text{ }^{\circ}\text{C}$
1.14	0.83	0.89	0.92	0.98	<b>1.00</b>	1.02
1.2	0.75	0.80	0.83	0.89	0.91	0.93
1.26	0.69	0.73	0.76	0.81	0.83	0.85

**Table 22 • Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			200	MHz
HSTL1.5 V			200	MHz
SSTL 2.5 V	255	350	200	MHz
SSTL 1.8 V			334	MHz
SSTL 1.5 V			334	MHz

**Table 23 • Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	450		MHz
LVDS 3.3 V	267.5		MHz
LVDS 2.5 V	267.5	350	MHz
RSDS	260	350	MHz
BLVDS	250		MHz
MLVDS	250		MHz
Mini-LVDS	260	350	MHz

**Table 43 • LVCMOS 2.5 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	$V_{TRIP}$	1.2	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega\sigma$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**Table 44 • LVCMOS 2.5 V Transmitter Drive Strength Specifications**

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} - 0.4$	0.4	2	2
4 mA	4 mA	4 mA	$V_{DDI} - 0.4$	0.4	4	4
6 mA	6 mA	6 mA	$V_{DDI} - 0.4$	0.4	6	6
8 mA	8 mA	8 mA	$V_{DDI} - 0.4$	0.4	8	8
12 mA	12 mA	12 mA	$V_{DDI} - 0.4$	0.4	12	12
16 mA		16 mA	$V_{DDI} - 0.4$	0.4	16	16

**Note:** For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at:  
[www.microsemi.com/soc/download/ibis/default.aspx](http://www.microsemi.com/soc/download/ibis/default.aspx).

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

**Table 45 • LVCMOS 2.5 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	$T_{PY}$		$T_{PYS}$		Unit
		-1	-Std	-1	-Std	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.29	2.694	2.305	2.712	ns

**Table 46 • LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}^1$		$T_{LZ}^1$		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns

**Table 53 • LVCMOS 1.8 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	Ω

**Table 54 • LVCMOS 1.8 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V <sub>TRIP</sub>	0.9	V
Resistance for enable path (T <sub>ZH</sub> , T <sub>ZL</sub> , T <sub>HZ</sub> , T <sub>LZ</sub> )	R <sub>ENT</sub>	2k	Ω
Capacitive loading for enable path (T <sub>ZH</sub> , T <sub>ZL</sub> , T <sub>HZ</sub> , T <sub>LZ</sub> )	C <sub>ENT</sub>	5	pF
Capacitive loading for data path (T <sub>DP</sub> )	C <sub>LOAD</sub>	5	pF

**Table 55 • LVCMOS 1.8 V Transmitter Drive Strength Specifications**

Output Drive Selection			V <sub>OH</sub> (V)	V <sub>OL</sub> (V)	IOH (at V <sub>OH</sub> )	IOL (at V <sub>OL</sub> )
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max	mA	mA
2 mA	2 mA	2 mA	V <sub>DDI</sub> - 0.45	0.45	2	2
4 mA	4 mA	4 mA	V <sub>DDI</sub> - 0.45	0.45	4	4
6 mA	6 mA	6 mA	V <sub>DDI</sub> - 0.45	0.45	6	6
8 mA	8 mA	8 mA	V <sub>DDI</sub> - 0.45	0.45	8	8
10 mA	10 mA	10 mA	V <sub>DDI</sub> - 0.45	0.45	10	10
12 mA		12 mA	V <sub>DDI</sub> - 0.45	0.45	12	12
		16 mA <sup>1</sup>	V <sub>DDI</sub> - 0.45	0.45	16	16

1. 16 mA drive strengths, all slews, meets LPDDR JEDEC electrical compliance.

**AC Switching Characteristics**

Worst commercial-case conditions: T<sub>J</sub> = 85 °C, V<sub>DD</sub> = 1.14 V, V<sub>DDI</sub> = 1.71 V

**Table 56 • LVCMOS 1.8 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	T <sub>PY</sub>		T <sub>PYS</sub>		Unit
		-1	-Std	-1	-Std	
<b>LVCMOS 1.8 V (for DDRIO I/O bank with Fixed Codes)</b>	None	1.968	2.315	2.099	2.47	ns
	None	2.898	3.411	2.883	3.393	ns
	50	3.05	3.59	3.044	3.583	ns
	75	2.999	3.53	2.987	3.516	ns
<b>LVCMOS 1.8 V (for MSIO I/O bank)</b>	150	2.947	3.469	2.933	3.452	ns
	None	2.611	3.071	2.598	3.057	ns
	50	2.775	3.264	2.775	3.265	ns
	75	2.72	3.2	2.712	3.19	ns
<b>LVCMOS 1.8 V (for MSIOD I/O bank)</b>	150	2.666	3.137	2.655	3.123	ns

**Table 58 • LVCMOS 1.8 V Transmitter Characteristics for MSIO I/O Bank**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.441	4.047	4.165	4.9	4.413	5.192	4.891	5.755	5.138	6.044	ns
4 mA	Slow	3.218	3.786	3.642	4.284	3.941	4.636	5.665	6.665	5.568	6.551	ns
6 mA	Slow	3.141	3.694	3.501	4.118	3.823	4.498	6.587	7.75	6.032	7.096	ns
8 mA	Slow	3.165	3.723	3.319	3.904	3.654	4.298	6.898	8.115	6.216	7.313	ns
10 mA	Slow	3.202	3.767	3.278	3.857	3.616	4.254	7.25	8.529	6.435	7.571	ns
12 mA	Slow	3.277	3.855	3.175	3.736	3.519	4.139	7.392	8.697	6.538	7.692	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 59 • LVCMOS 1.8 V Transmitter Characteristics for MSIOD I/O Bank**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.725	3.206	3.316	3.901	3.484	4.099	5.204	6.123	4.997	5.88	ns
4 mA	Slow	2.242	2.638	2.777	3.267	2.947	3.466	5.729	6.74	5.448	6.41	ns
6 mA	Slow	1.995	2.347	2.466	2.901	2.63	3.094	6.372	7.496	5.987	7.043	ns
8 mA	Slow	2.001	2.354	2.44	2.87	2.6	3.058	6.633	7.804	6.193	7.286	ns
10 mA	Slow	2.025	2.382	2.312	2.719	2.47	2.906	6.94	8.165	6.412	7.544	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**2.3.5.9 1.5 V LVCMOS**

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

**Table 60 • LVCMOS 1.5 V DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>DDI</sub>	1.425	1.5	1.575	V

**Table 61 • LVCMOS 1.5 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high for (MSIOD and DDRIO I/O banks)	V <sub>IH</sub> (DC)	0.65 × V <sub>DDI</sub>	1.575	V
DC input logic high (for MSIO I/O bank)	V <sub>IH</sub> (DC)	0.65 × V <sub>DDI</sub>	3.45	V
DC input logic low	V <sub>IL</sub> (DC)	-0.3	0.35 × V <sub>DDI</sub>	V
Input current high <sup>1</sup>	I <sub>IH</sub> (DC)			-
Input current low <sup>1</sup>	I <sub>IL</sub> (DC)			-

1. See Table 24, page 22.



**Table 62 • LVCMOS 1.5 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	VOH	$V_{DDI} \times 0.75$		V
DC output logic low	VOL		$V_{DDI} \times 0.25$	V

**Table 63 • LVCMOS 1.5 V AC Minimum and Maximum Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	$D_{MAX}$	235	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	$D_{MAX}$	160	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	$D_{MAX}$	220	Mbps	AC loading: 17 pF load, maximum drive/slew

**Table 64 • LVCMOS 1.5 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CA L	75, 60, 50, 40	$\Omega$

**Table 65 • LVCMOS 1.5 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point	$V_{TRIP}$	0.75	V
Resistance for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$R_{ENT}$	2K	$\Omega$
Capacitive loading for enable path ( $T_{ZH}$ , $T_{ZL}$ , $T_{HZ}$ , $T_{LZ}$ )	$C_{ENT}$	5	pF
Capacitive loading for data path ( $T_{DP}$ )	$C_{LOAD}$	5	pF

**Table 66 • LVCMOS 1.5 V Transmitter Drive Strength Specifications**

Output Drive Selection			$V_{OH}$ (V)	$V_{OL}$ (V)	IOH (at $V_{OH}$ ) mA	IOL (at $V_{OL}$ ) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	2	2
4 mA	4 mA	4 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	4	4
6 mA	6 mA	6 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	6	6
8 mA		8 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	8	8
		10 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	10	10
		12 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	12	12

**Note:** For a detailed I/V curve, use the corresponding IBIS models:  
[www.microsemi.com/soc/download/ibis/default.aspx](http://www.microsemi.com/soc/download/ibis/default.aspx).

**Table 70 • LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**  
(continued)

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
6 mA	Slow	4.244	4.993	3.465	4.076	4.233	4.979	6.39	7.518	5.736	6.748	ns
	Medium	3.774	4.44	3.05	3.587	3.762	4.426	6.114	7.193	5.397	6.35	ns
	Medium fast	3.544	4.17	2.839	3.339	3.529	4.152	5.978	7.033	5.27	6.2	ns
	Fast	3.519	4.14	2.82	3.317	3.504	4.122	5.965	7.017	5.259	6.187	ns
8 mA	Slow	4.099	4.823	3.311	3.894	4.087	4.807	6.584	7.746	5.854	6.888	ns
	Medium	3.656	4.301	2.927	3.443	3.642	4.284	6.311	7.425	5.553	6.533	ns
	Medium fast	3.437	4.044	2.731	3.213	3.42	4.023	6.182	7.273	5.435	6.394	ns
	Fast	3.41	4.012	2.715	3.193	3.393	3.991	6.178	7.269	5.425	6.383	ns
10 mA	Slow	4.029	4.74	3.238	3.809	4.015	4.723	6.732	7.921	5.965	7.018	ns
	Medium	3.601	4.237	2.867	3.372	3.586	4.218	6.473	7.615	5.669	6.669	ns
	Medium fast	3.384	3.981	2.672	3.143	3.365	3.958	6.351	7.471	5.55	6.529	ns
	Fast	3.357	3.949	2.655	3.123	3.338	3.927	6.345	7.464	5.54	6.518	ns
12 mA	Slow	3.974	4.675	3.196	3.759	3.958	4.656	6.842	8.049	6.068	7.139	ns
	Medium	3.55	4.176	2.827	3.326	3.534	4.157	6.584	7.746	5.751	6.766	ns
	Medium fast	3.345	3.935	2.638	3.103	3.325	3.911	6.488	7.633	5.641	6.637	ns
	Fast	3.316	3.902	2.621	3.083	3.297	3.878	6.486	7.63	5.626	6.619	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 71 • LVCMOS 1.5 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	4.423	5.203	5.397	6.35	5.686	6.69	5.609	6.599	5.561	6.542	ns
4 mA	Slow	4.05	4.765	4.503	5.298	4.92	5.788	7.358	8.657	6.525	7.677	ns
6 mA	Slow	4.081	4.801	4.259	5.012	4.699	5.528	7.659	9.011	6.709	7.893	ns
8 mA	Slow	4.234	4.98	4.068	4.786	4.521	5.319	8.218	9.668	7.05	8.294	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 156 • LPDDR-LVCMOS 1.8 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V <sub>TRIP</sub>	0.9	V
Resistance for enable path (T <sub>ZH</sub> , T <sub>ZL</sub> , T <sub>HZ</sub> , T <sub>LZ</sub> )	R <sub>ENT</sub>	2K	Ω
Capacitive loading for enable path (T <sub>ZH</sub> , T <sub>ZL</sub> , T <sub>HZ</sub> , T <sub>LZ</sub> )	C <sub>ENT</sub>	5	pF
Capacitive loading for data path (T <sub>DP</sub> )	C <sub>LOAD</sub>	5	pF

**Table 157 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification for DDRIO Bank**

Output Drive Selection	V <sub>OH</sub> (V) Min	V <sub>OL</sub> (V) Max	I <sub>OH</sub> (at V <sub>OH</sub> ) mA	I <sub>OL</sub> (at V <sub>OL</sub> ) mA
2 mA	V <sub>DDI</sub> - 0.45	0.45	2	2
4 mA	V <sub>DDI</sub> - 0.45	0.45	4	4
6 mA	V <sub>DDI</sub> - 0.45	0.45	6	6
8 mA	V <sub>DDI</sub> - 0.45	0.45	8	8
10 mA	V <sub>DDI</sub> - 0.45	0.45	10	10
12 mA	V <sub>DDI</sub> - 0.45	0.45	12	12
16 mA <sup>1</sup>	V <sub>DDI</sub> - 0.45	0.45	16	16

1. 16 mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance.

**Table 158 • LPDDR-LVCMOS 1.8V AC Switching Characteristics for Receiver (for DDRIO I/O Bank with Fixed Code - Input Buffers)**

ODT (On Die Termination)	-1	-Std	-1	-Std	Unit
None	1.968	2.315	2.099	2.47	ns

**Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T <sub>DP</sub>		T <sub>ZL</sub>		T <sub>ZH</sub>		T <sub>HZ</sub> <sup>1</sup>		T <sub>LZ</sub> <sup>1</sup>		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	medium_fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	medium_fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	medium_fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns

**Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers) (continued)**

	medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	medium_fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	medium_fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	medium_fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	medium_fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO management).

### 2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

#### 2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

##### Minimum and Maximum Input and Output Levels

**Table 160 • LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	$V_{DDI}$	2.375	2.5	2.625	V	2.5 V range
Supply voltage	$V_{DDI}$	3.15	3.3	3.45	V	3.3 V range

**Table 161 • LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit	Conditions
DC Input voltage	$V_I$	0	2.925	V	2.5 V range
DC input voltage	$V_I$	0	3.45	V	3.3 V range
Input current high <sup>1</sup>	$I_{IH}$ (DC)				
Input current low <sup>1</sup>	$I_{IL}$ (DC)				

1. See Table 24, page 22.

**AC Switching Characteristics**

Worst commercial-case conditions:  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$ .

**Table 180 • B-LVDS AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

**Table 181 • B-LVDS AC Switching Characteristics for Receiver for MSIOD I/O Bank (Input Buffers)**

On-Die Termination (ODT)	$T_{PY}$		Unit
	-1	-Std	
None	2.495	2.934	ns
100	2.495	2.935	ns

**Table 182 • B-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

$T_{DP}$		$T_{ZL}$		$T_{ZH}$		$T_{HZ}$		$T_{LZ}$		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.258	2.656	2.343	2.756	2.329	2.74	2.12	2.494	2.123	2.497	ns

**2.3.7.3 M-LVDS**

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

**Minimum and Maximum Input and Output Levels**

**Table 183 • M-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage <sup>1</sup>	$V_{DDI}$	2.375	2.5	2.625	V

1. Only M-LVDS TYPE I is supported.

**Table 184 • M-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	$V_I$	0	2.925	V
Input current high <sup>1</sup>	$I_{IH}$ (DC)			
Input current low <sup>2</sup>	$I_{IL}$ (DC)			

1. See Table 24, page 22.

The following table lists the input data register propagation delays in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

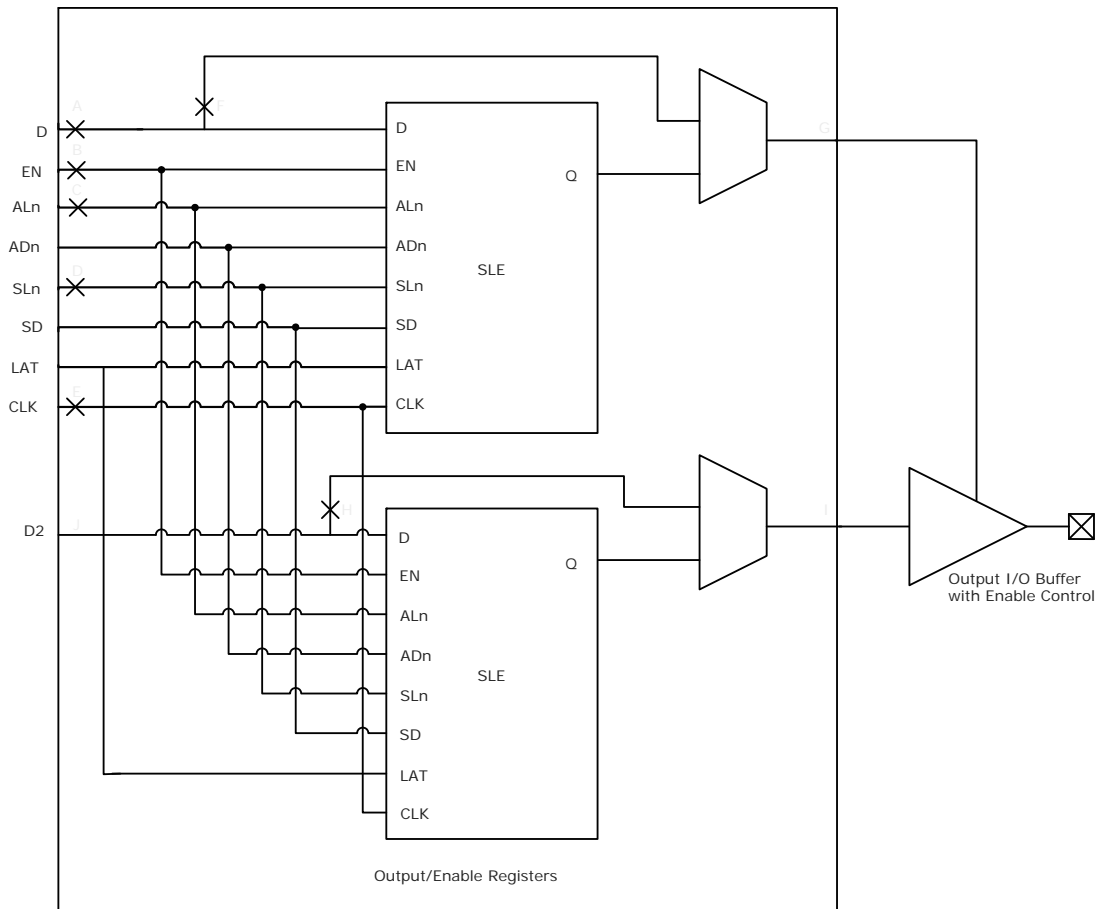
**Table 219 • Input Data Register Propagation Delays**

Parameter	Symbol	Measuring Nodes (from, to) <sup>1</sup>	-1		Unit
			-1	-Std	
Bypass delay of the input register	$T_{IBYP}$	F, G	0.353	0.415	ns
Clock-to-Q of the input register	$T_{ICLKQ}$	E, G	0.16	0.188	ns
Data setup time for the input register	$T_{ISUD}$	A, E	0.357	0.421	ns
Data hold time for the input register	$T_{IHD}$	A, E	0	0	ns
Enable setup time for the input register	$T_{ISUE}$	B, E	0.46	0.542	ns
Enable hold time for the input register	$T_{IHE}$	B, E	0	0	ns
Synchronous load setup time for the input register	$T_{ISUSL}$	D, E	0.46	0.542	ns
Synchronous load hold time for the input register	$T_{IHSL}$	D, E	0	0	ns
Asynchronous clear-to-Q of the input register (ADn=1)	$T_{IALN2Q}$	C, G	0.625	0.735	ns
Asynchronous preset-to-Q of the input register (ADn=0)		C, G	0.587	0.69	ns
Asynchronous load removal time for the input register	$T_{IREMALN}$	C, E	0	0	ns
Asynchronous load recovery time for the input register	$T_{IRECALN}$	C, E	0.074	0.087	ns
Asynchronous load minimum pulse width for the input register	$T_{IWALN}$	C, C	0.304	0.357	ns
Clock minimum pulse width high for the input register	$T_{ICKMPWH}$	E, E	0.075	0.088	ns
Clock minimum pulse width low for the input register	$T_{ICKMPWL}$	E, E	0.159	0.187	ns

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

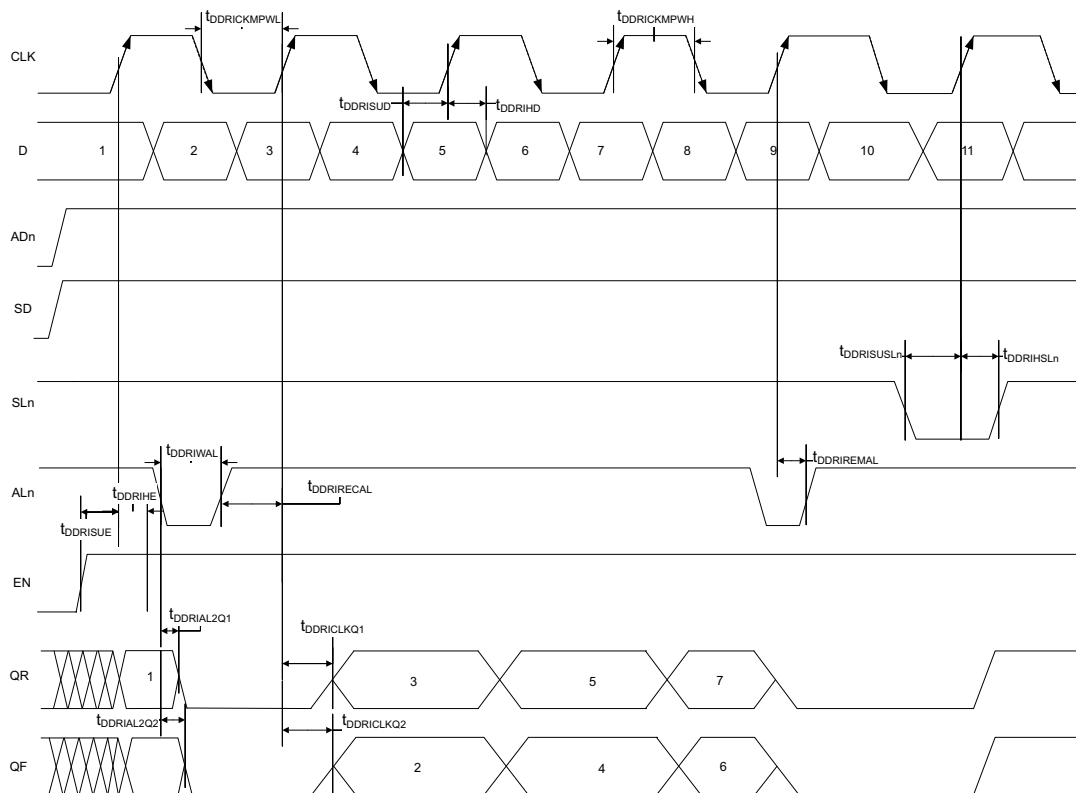
### 2.3.8.2 Output/Enable Register

Figure 8 • Timing Model for Output/Enable Register



### 2.3.9.2 Input DDR Timing Diagram

Figure 11 • Input DDR Timing Diagram



### 2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 221 • Input DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDRICKLKQ1}$	Clock-to-Out Out_QR for input DDR	B, C	0.16	0.188	ns
$T_{DDRICKLKQ2}$	Clock-to-Out Out_QF for input DDR	B, D	0.166	0.195	ns
$T_{DDRISUD}$	Data setup for input DDR	A, B	0.357	0.421	ns
$T_{DDRIHD}$	Data hold for input DDR	A, B	0	0	ns
$T_{DDRISUE}$	Enable setup for input DDR	E, B	0.46	0.542	ns
$T_{DDRIHE}$	Enable hold for input DDR	E, B	0	0	ns
$T_{DDRISUSL}$	Synchronous load setup for input DDR	G, B	0.46	0.542	ns
$T_{DDRIHSL}$	Synchronous load hold for input DDR	G, B	0	0	ns
$T_{DDRIR2Q1}$	Asynchronous load-to-out QR for input DDR	F, C	0.587	0.69	ns
$T_{DDRIR2Q2}$	Asynchronous load-to-out QF for input DDR	F, D	0.541	0.636	ns
$T_{DDRIREMAL}$	Asynchronous load removal time for input DDR	F, B	0	0	ns
$T_{DDRIRECAL}$	Asynchronous load recovery time for input DDR	F, B	0.074	0.087	ns



**Table 241 •  $\mu$ SRAM (RAM256x4) in 256 x 4 Mode (continued)**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Write address hold time	$T_{ADDRCHD}$	0.245		0.288		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.03		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 512 x 2 mode in worst commercial-case conditions when  $T_J = 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 242 •  $\mu$ SRAM (RAM512x2) in 512 x 2 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.27		0.31	ns
Read access time without pipeline register				1.76		2.08
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.96		2.306	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.137		0.161		ns
Read address hold time in asynchronous mode			-0.58		-0.68	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHD}$	-0.65		-0.77		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.14		2.52	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$	-0.02		-0.03		ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	
Read asynchronous reset recovery time (pipelined clock)	$T_{RSTREC}$	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)			0.236		0.278	
Read asynchronous reset to output propagation delay (with pipelined register enabled)	$T_{R2Q}$		0.83		0.98	ns
Read synchronous reset setup time	$T_{SRSTSU}$	0.271		0.319		ns
Read synchronous reset hold time	$T_{SRSTHD}$	0.061		0.071		ns

**Table 242 •  $\mu$ SRAM (RAM512x2) in 512 x 2 Mode (continued)**

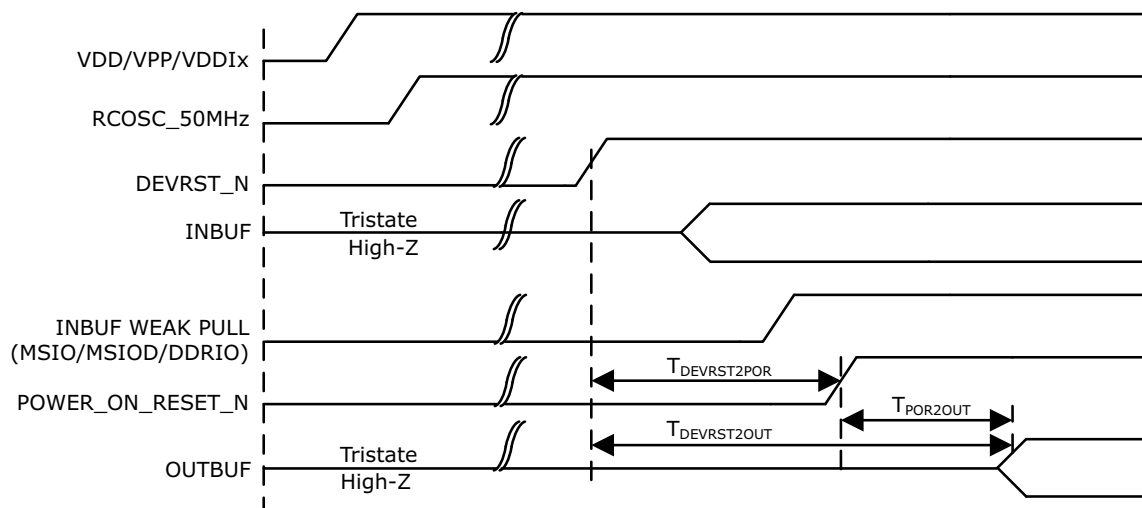
Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Write clock period	$T_{CCY}$	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	$T_{BLKCSU}$	0.404		0.476		ns
Write block hold time	$T_{BLKCHD}$	0.007		0.008		ns
Write input data setup time	$T_{DINCSU}$	0.101		0.118		ns
Write input data hold time	$T_{DINCHD}$	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.247		0.29		ns
Write enable setup time	$T_{WECSU}$	0.397		0.467		ns
Write enable hold time	$T_{WECHD}$	-0.03		-0.03		ns
Maximum frequency	$F_{MAX}$		250		250	MHz

The following table lists the  $\mu$ SRAM in 1024 x 1 mode in worst commercial-case conditions when  $T_J = 85^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 243 •  $\mu$ SRAM (RAM1024x1) in 1024 x 1 Mode**

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	$T_{CY}$	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	$T_{PLCY}$	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	$T_{CLK2Q}$		0.27		0.31	ns
Read access time without pipeline register				1.78		2.1
Read address setup time in synchronous mode	$T_{ADDRSU}$	0.301		0.354		ns
Read address setup time in asynchronous mode			1.978		2.327	
Read address hold time in synchronous mode	$T_{ADDRHD}$	0.137		0.161		ns
Read address hold time in asynchronous mode			-0.6		-0.71	
Read enable setup time	$T_{RDENSU}$	0.278		0.327		ns
Read enable hold time	$T_{RDENHD}$	0.057		0.067		ns
Read block select setup time	$T_{BLKSU}$	1.839		2.163		ns
Read block select hold time	$T_{BLKHHD}$	-0.65		-0.77		ns
Read block select to out disable time (when pipelined register is disabled)	$T_{BLK2Q}$		2.16		2.54	ns
Read asynchronous reset removal time (pipelined clock)	$T_{RSTREM}$		-0.02		-0.03	ns
Read asynchronous reset removal time (non-pipelined clock)			0.046		0.054	

Figure 20 • DEVRST\_N to Functional Timing Diagram for IGLOO2



### 2.3.27 Flash\*Freeze Timing Characteristics

The following table lists the Flash\*Freeze entry and exit times in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

Table 293 • Flash\*Freeze Entry and Exit Times

Parameter	Symbol	Entry/Exit Timing			Unit	Conditions
		FCLK = 100MHz		FCLK = 3 MHz		
		005, 010, 025, 060, 090, and 150	050	All Devices		
Entry time	TFF_ENTRY	160	150	320	$\mu\text{s}$	eNVM and MSS/HPMS PLL = ON
		215	200	430	$\mu\text{s}$	eNVM and MSS/HPMS PLL= OFF
Exit time with respect to the MSS PLL Lock	TFF_EXIT	100	100	140	$\mu\text{s}$	eNVM and MSS/HPMS PLL = ON during F*F
		136	120	190	$\mu\text{s}$	eNVM = ON and MSS/HPMS PLL = OFF during F*F and MSS/HPMS PLL turned back on at exit
		200	200	285	$\mu\text{s}$	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit
		200	200	285	$\mu\text{s}$	eNVM = OFF and MSS/HPMS PLL = ON during F*F and eNVM turned back on at exit

## 2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 308 • MMUART Characteristics**

Parameter	Description	-1	-Std	Unit
FMMUART_REF_CLK	Internally sourced MMUART reference clock frequency.	166	142	MHz
BAUDMMUARTTx	Maximum transmit baud rate	10.375	8.875	Mbps
BAUDMMUARTRx	Maximum receive baud rate	10.375	8.875	Mbps

## 2.3.35 IGLOO2 Specifications

### 2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 309 • Maximum Frequency for HPMS Main Clock**

Symbol	Description	-1	-Std	Unit
HPMS_CLK	Maximum frequency for the HPMS main clock	166	142	MHz

### 2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI\_0\_CLK. For timing parameter definitions, see Figure 23, page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when  $T_J = 100\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ .

**Table 310 • SPI Characteristics for All Devices**

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12			ns	
	SPI_[0 1]_CLK = PCLK/4	24.1			ns	
	SPI_[0 1]_CLK = PCLK/8	48.2			ns	
	SPI_[0 1]_CLK = PCLK/16	0.1			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/32	0.19			$\mu\text{s}$	
	SPI_[0 1]_CLK = PCLK/64	0.39			$\mu\text{s}$	
SPI_[0 1]_CLK = PCLK/128	0.77			$\mu\text{s}$		

**Table 310 • SPI Characteristics for All Devices (continued)**

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) <sup>1</sup>		2.77		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) <sup>1</sup>		2.906		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time <sup>2</sup>	12			ns	
sp9m	SPI_[0 1]_DI hold time <sup>2</sup>	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time <sup>2</sup>	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time <sup>2</sup>	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time <sup>2</sup>	2			ns	
sp9s	SPI_[0 1]_DI hold time <sup>2</sup>	7			ns	