Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 90K Logic Modules
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s090t-1fgg676i

Table 4 • **Recommended Operating Conditions** *(continued)*

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
3.3 V DC supply voltage	V_{DDIx}	3.15	3.3	3.45	V	
LVDS differential I/O	V_{DDIx}	2.375	2.5	3.45	V	
B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O	V_{DDIx}	2.375	2.5	2.625	V	
LVPECL differential I/O	V_{DDIx}	3.15	3.3	3.45	V	
Reference voltage supply for FDDR (Bank0) and MDDR (Bank5)	V_{REFx}	0.49 × V_{DDIx}	0.5 × V_{DDIx}	0.51 × V_{DDIx}	V	
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V_{PP}.	V_{PPNVM}	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range

1. Programming at Industrial temperature range is available only with V_{PP} = 3.3 V.

Note: Power supply ramps must all be strictly monotonic, without plateaus.

Table 5 • **FPGA Operating Limits**

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Digest Temperature	Digest Cycles	Retention (Biased/ Unbiased)
Commercial	FPGA	Min T_J = 0 °C Max T_J = 85 °C	Min T_J = 0 °C Max T_J = 85 °C	500	Min T_J = 0 °C Max T_J = 85 °C	2000	20 years
Industrial[1]	FPGA	Min T_J = –40 °C Max T_J = 100 °C	Min T_J = –40 °C Max T_J = 100 °C	500	Min T_J = –40 °C Max T_J = 100 °C	2000	20 years

1. Programming at Industrial temperature range is available only with VPP = 3.3 V.

Note: The retention specification is defined as the total number of programing and digest cycles. For example, 20 years of retention after 500 programming cycles.

Note: The digest cycle specification is 2000 digest cycles for every program cycle with a maximum of 500 programming cycles.

Note: If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

Table 9 • **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices** *(continued)*

Device	Still Air	1.0 m/s	2.5 m/s	θ_{JB}	θ_{JC}	Unit
		θ_{JA}				
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W
FCS536	15.01	12.06	10.76	3.69	1.55	°C/W
FCV484	16.21	13.11	11.84	6.73	0.10	°C/W

2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

θ_{JA} = 14.7 °C/W (taken from Table 9, page 10).

T_A = 85 °C

$$\text{Maximum power allowed} = \frac{100\ °C - 85\ °C}{14.7\ °C/W} = 1.088\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

2.3.1.3 ESD Performance

See *RT0001: Microsemi Corporation - SoC Products Reliability Report* for information about ESD.

2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 38 • **LVCMOS 2.5 V DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 39 • **LVCMOS 2.5 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	1.7	2.625	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	1.7	3.45	V
DC input logic low	V_{IL} (DC)	−0.3	0.7	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 40 • **LVCMOS 2.5 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}[1]	$V_{DDI} - 0.4$	–	V
DC output logic low	V_{OL}[2]		0.4	V

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

Table 41 • **LVCMOS 2.5 V AC Minimum and Maximum Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	410	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	420	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 42 • **LVCMOS 2.5 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	Ω

Table 48 •   **LVCMOS 2.5 V Transmitter Characteristics for MSIOD Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		Unit
		−1	−Std	−1	−Std	−1	−Std	−1	−Std	−1	−Std	
2 mA	Slow	2.206	2.596	2.678	3.15	2.64	3.106	4.935	5.805	4.74	5.576	ns
4 mA	Slow	1.835	2.159	2.242	2.637	2.256	2.654	5.413	6.368	5.15	6.059	ns
6 mA	Slow	1.709	2.01	2.132	2.508	2.167	2.549	5.813	6.838	5.499	6.469	ns
8 mA	Slow	1.63	1.918	1.958	2.303	2.012	2.367	6.226	7.324	5.816	6.842	ns
12 mA	Slow	1.648	1.939	1.86	2.187	1.921	2.259	6.519	7.669	6.027	7.09	ns

1.   Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.8 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 49 •   **LVCMOS 1.8 V DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ Max	Unit
LVCMOS 1.8 V DC Recommended Operating Conditions				
Supply voltage	V_{DDI}	1.710	1.8 1.89	V

Table 50 •   **LVCMOS 1.8 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	$0.65 \times V_{DDI}$	1.89	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	V_{IL} (DC)	−0.3	$0.35 \times V_{DDI}$	V
Input current high[1]	I_{IH} (DC)		−	
Input current low[1]	I_{IL} (DC)		−	

1.   See Table 24, page 22.

Table 51 •   **LVCMOS 1.8 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	$V_{DDI} - 0.45$		V
DC output logic low	V_{OL}		0.45	V

Table 52 •   **LVCMOS 1.8 V Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)[1]	D_{MAX}	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	295	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)[1]	D_{MAX}	400	Mbps	AC loading: 17 pF load, maximum drive/slew

1.   Maximum Data Rate applies for Drive Strength 8 mA and above, All Slews.

Table 62 • **LVCMOS 1.5 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	VOH	V_{DDI} × 0.75		V
DC output logic low	VOL		V_{DDI} × 0.25	V

Table 63 • **LVCMOS 1.5 V AC Minimum and Maximum Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	235	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	160	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	220	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 64 • **LVCMOS 1.5 V AC Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 40	Ω

Table 65 • **LVCMOS 1.5 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 66 • **LVCMOS 1.5 V Transmitter Drive Strength Specifications**

Output Drive Selection			V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH})	IOL (at V_{OL})
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max	mA	mA
2 mA	2 mA	2 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	2	2
4 mA	4 mA	4 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	4	4
6 mA	6 mA	6 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	6	6
8 mA		8 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	8	8
		10 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	10	10
		12 mA	V_{DDI} × 0.75	V_{DDI} × 0.25	12	12

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

Table 95 • **HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only**

Parameter	Symbol	Min	Max	Unit
HSTL Class I				
DC output logic high	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current (MSIO and DDRIO I/O banks)	I_{OH} at V_{OH}	−8.0		mA
Output minimum sink current (MSIO and DDRIO I/O banks)	I_{OL} at V_{OL}	8.0		mA
HSTL Class II				
DC output logic high	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current	I_{OH} at V_{OH}	−16.0		mA
Output minimum sink current	I_{OL} at V_{OL}	16.0		mA

Table 96 • **HSTL DC Differential Voltage Specification**

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.2	V

Table 97 • **HSTL AC Differential Voltage Specifications**

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF}	0.4		V
AC differential cross point voltage	V_x	0.68	0.9	V

Table 98 • **HSTL Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications

Table 99 • **HSTL Impedance Specification**

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	R_{REF}	25.5, 47.8	Ω	Reference resistance = 191 Ω
Effective impedance value (ODT for DDRIO I/O bank only)	R_{TT}	47.8	Ω	Reference resistance = 191 Ω

Table 100 • **HSTL AC Test Parameter Specification**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for HSTL15 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for HSTL15 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst-case commercial conditions: T_J = 85 °C, V_{DD} = 1.14 V, worst-case V_{DDI}.

Table 101 • **HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)**

		T_{PY}		
	On-Die Termination (ODT)	−1	−Std	Unit
Pseudo differential	None	1.605	1.888	ns
	47.8	1.614	1.898	ns
True differential	None	1.622	1.909	ns
	47.8	1.628	1.916	ns

Table 102 • **HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	−1	−Std	−1	−Std	−1	−Std	−1	−Std	−1	−Std	Unit
HSTL Class I											
Single-ended	2.6	3.059	2.514	2.958	2.514	2.958	2.431	2.86	2.431	2.86	ns
Differential	2.621	3.083	2.648	3.115	2.647	3.113	2.925	3.442	2.923	3.44	ns
HSTL Class II											
Single-ended	2.511	2.954	2.488	2.927	2.49	2.93	2.409	2.833	2.411	2.836	ns
Differential	2.528	2.974	2.552	3.003	2.551	3.001	2.897	3.409	2.896	3.408	ns

2.3.6.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

Table 136 • **SSTL15 AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for SSTL15 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for SSTL15 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 1.425 V

Table 137 • **DDR3/SSTL15 Receiver Characteristics for DDRIO I/O Bank – with Calibration Only**

		T_{PY}		
	On-Die Termination (ODT)	–1	–Std	Unit
Pseudo differential	None	1.605	1.888	ns
	20	1.616	1.901	ns
	30	1.613	1.897	ns
	40	1.611	1.895	ns
	60	1.609	1.893	ns
	120	1.607	1.89	ns
True differential	None	1.623	1.91	ns
	20	1.637	1.926	ns
	30	1.63	1.918	ns
	40	1.626	1.914	ns
	60	1.622	1.91	ns
	120	1.619	1.905	ns

Table 138 • **DDR3/SSTL15 Transmitter Characteristics (Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)											
Single-ended	2.533	2.98	2.522	2.967	2.523	2.968	2.427	2.855	2.428	2.856	ns
Differential	2.555	3.005	3.073	3.615	3.073	3.615	2.416	2.843	2.416	2.843	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)											
Single-ended	2.53	2.977	2.514	2.958	2.516	2.96	2.422	2.849	2.425	2.852	ns
Differential	2.552	3.002	2.591	3.048	2.59	3.047	2.882	3.391	2.881	3.39	ns

Table 150 • **LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

	T_{DP}		T_{ENZL}		T_{ENZH}		T_{ENHZ}		T_{ENLZ}		
	−1	−Std	−1	−Std	−1	−Std	−1	−Std	−1	−Std	Unit
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns
Differential	2.298	2.703	2.288	2.692	2.288	2.692	2.593	3.051	2.593	3.051	ns

Minimum and Maximum DC/AC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode

Table 151 • **LPDDR-LVCMOS 1.8 V Mode Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.710	1.8	1.89	V

Table 152 • **LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	$0.65 \times V_{DDI}$	1.89	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	V_{IL} (DC)	−0.3	$0.35 \times V_{DDI}$	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 153 • **LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	$V_{DDI} - 0.45$		V
DC output logic low	V_{OL}		0.45	V

Table 154 • **LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: 17pf load, 8 ma drive and above/all slew

Table 155 • **LPDDR-LVCMOS 1.8 V Calibrated Impedance Option**

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 33, 25, 20	Ω

Table 168 • **LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

| On-Die Termination (ODT) | T_{PY} | | Unit |
	−1	−Std	
None	2.554	3.004	ns
100	2.549	2.999	ns

Table 169 • **LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| T_{DP} | | T_{ZL} | | T_{ZH} | | T_{HZ} | | T_{LZ} | | |
−1	−Std	−1	−Std	−1	−Std	−1	−Std	−1	−Std	Unit
2.136	2.513	2.416	2.842	2.402	2.825	2.423	2.85	2.409	2.833	ns

Table 170 • **LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

| | T_{DP} | | T_{ZL} | | T_{ZH} | | T_{HZ} | | T_{LZ} | | |
	−1	−Std	−1	−Std	−1	−Std	−1	−Std	−1	−Std	Unit
No pre-emphasis	1.61	1.893	1.749	2.058	1.735	2.041	1.897	2.231	1.866	2.195	ns
Min pre-emphasis	1.527	1.796	1.757	2.067	1.744	2.052	1.905	2.241	1.876	2.207	ns
Med pre-emphasis	1.496	1.76	1.765	2.077	1.751	2.06	1.914	2.252	1.884	2.216	ns

LVDS33 AC Switching Characteristics

Table 171 • **LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| On Die Termination (ODT) | T_{PY} | | Unit |
	−1	−Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

Table 172 • **LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| T_{DP} | | T_{ZL} | | T_{ZH} | | T_{HZ} | | T_{LZ} | | |
−1	−Std	−1	−Std	−1	−Std	−1	−Std	−1	−Std	Unit
1.942	2.284	1.98	2.33	1.97	2.318	1.953	2.298	1.96	2.307	ns

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V.

Table 180 • **B-LVDS AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

On-Die Termination (ODT)	T_{PY}		Unit
	−1	−Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

Table 181 • **B-LVDS AC Switching Characteristics for Receiver for MSIOD I/O Bank (Input Buffers)**

On-Die Termination (ODT)	T_{PY}		Unit
	−1	−Std	
None	2.495	2.934	ns
100	2.495	2.935	ns

Table 182 • **B-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
−1	−Std	−1	−Std	−1	−Std	−1	−Std	−1	−Std	Unit
2.258	2.656	2.343	2.756	2.329	2.74	2.12	2.494	2.123	2.497	ns

2.3.7.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum Input and Output Levels

Table 183 • **M-LVDS Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage[1]	V_{DDI}	2.375	2.5	2.625	V

1. Only M-LVDS TYPE I is supported.

Table 184 • **M-LVDS DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	2.925	V
Input current high[1]	I_{IH} (DC)			
Input current low[2]	I_{IL} (DC)			

1. See Table 24, page 22.

The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

Figure 16 • **Sequential Module Timing Diagram**
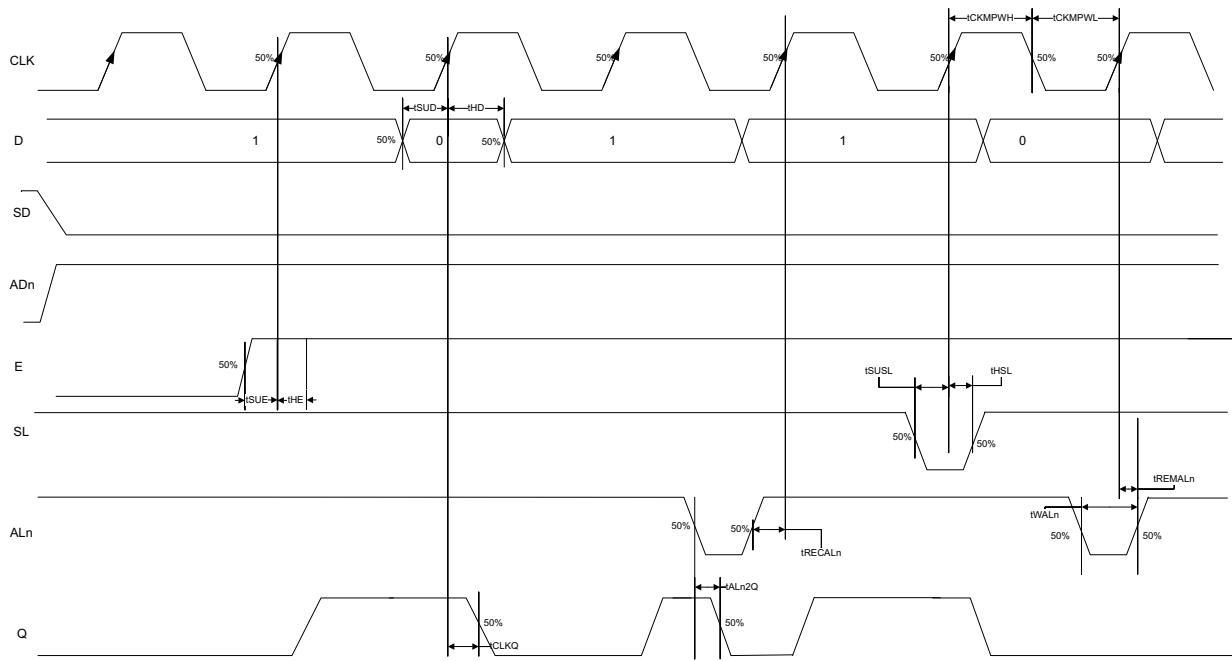
2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 224 • **Register Delays**

Parameter	Symbol	–1	–Std	Unit
Clock-to-Q of the core register	T_{CLKQ}	0.108	0.127	ns
Data setup time for the core register	T_{SUD}	0.254	0.298	ns
Data hold time for the core register	T_{HD}	0	0	ns
Enable setup time for the core register	T_{SUE}	0.335	0.394	ns
Enable hold time for the core register	T_{HE}	0	0	ns
Synchronous load setup time for the core register	T_{SUSL}	0.335	0.394	ns
Synchronous load hold time for the core register	T_{HSL}	0	0	ns
Asynchronous Clear-to-Q of the core register (ADn = 1)	T_{ALN2Q}	0.473	0.556	ns
Asynchronous preset-to-Q of the core register (ADn = 0)		0.451	0.531	ns
Asynchronous load removal time for the core register	T_{REMALN}	0	0	ns
Asynchronous load recovery time for the core register	T_{RECALN}	0.353	0.415	ns
Asynchronous load minimum pulse width for the core register	T_{WALN}	0.266	0.313	ns
Clock minimum pulse width high for the core register	T_{CKMPWH}	0.065	0.077	ns
Clock minimum pulse width low for the core register	T_{CKMPWL}	0.139	0.164	ns

2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 225 • **150 Device Global Resource**

Parameter	Symbol	−1		−Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.83	0.911	0.831	0.913	ns
Input high delay for global clock	T_{RCKH}	1.457	1.588	1.715	1.869	ns
Maximum skew for global clock	T_{RCKSW}		0.131		0.154	ns

The following table lists the 090 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 226 • **090 Device Global Resource**

Parameter	Symbol	−1		−Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.835	0.888	0.833	0.886	ns
Input high delay for global clock	T_{RCKH}	1.405	1.489	1.654	1.752	ns
Maximum skew for global clock	T_{RCKSW}		0.084		0.098	ns

The following table lists the 050 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 227 • **050 Device Global Resource**

Parameter	Symbol	−1		−Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.827	0.897	0.826	0.896	ns
Input high delay for global clock	T_{RCKH}	1.419	1.53	1.671	1.8	ns
Maximum skew for global clock	T_{RCKSW}		0.111		0.129	ns

The following table lists the 025 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 228 • **025 Device Global Resource**

Parameter	Symbol	−1		−Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.747	0.799	0.745	0.797	ns
Input high delay for global clock	T_{RCKH}	1.294	1.378	1.522	1.621	ns
Maximum skew for global clock	T_{RCKSW}		0.084		0.099	ns

Table 259 • **2 Step IAP Programming (Fabric Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	4	39	6	Sec
010	568784	7	45	12	Sec
025	1223504	14	55	23	Sec
050	2424832	29	74	40	Sec
060	2418896	39	83	50	Sec
090	3645968	60	106	73	Sec
150	6139184	100	154	120	Sec

Table 260 • **2 Step IAP Programming (eNVM Only)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	2	59	5	Sec
010	274816	4	98	11	Sec
025	274816	4	100	10	Sec
050	2,78,528	3	107	9	Sec
060	268480	5	98	22	Sec
090	544496	10	174	43	Sec
150	544496	10	175	44	Sec

Table 261 • **2 Step IAP Programming (Fabric and eNVM)**

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	6	78	11	Sec
010	842688	11	122	21	Sec
025	1497408	19	135	32	Sec
050	2695168	32	158	48	Sec
060	2686464	43	159	70	Sec
090	4190208	68	258	115	Sec
150	6682768	109	308	162	Sec

1. The minimum output clock frequency is limited by the PLL. For more information, see *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide.*
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.

The following table lists the CCC/PLL jitter specifications in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 283 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**

CCC Output Maximum Peak-to-Peak Period Jitter F_{OUT_CCC}

Parameter	Conditions/Package Combinations					Unit
10 FG484, 050 FG896/FG484/FCS325 Packages[1]	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16	
20 MHz to 100 MHz	Max(110, ± 1% x (1/F_{OUT_CCC}))	Max(150, ± 1% x (1/F_{OUT_CCC}))				ps
100 MHz to 400 MHz	Max(120, ± 1% x (1/F_{OUT_CCC}))	Max(150, ± 1% x (1/F_{OUT_CCC}))			Max(170, ± 1% x (1/F_{OUT_CCC}))	ps
025 FG484/FCS325 Package[1]	0 < SSO <=16					
20 MHz to 74 MHz	± 1% x (1/F_{OUT_CCC}))					ps
74 MHz to 400 MHz	210					ps
005 FG484 Package[1]	0 < SSO <=16					
20 MHz to 53 MHz	± 1% x (1/F_{OUT_CCC}))					ps
53 MHz to 400 MHz	270					ps
090 FG676 and FC325 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F_{OUT_CCC}))					ps
100 MHz to 400 MHz	150					ps
060 FG676 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F_{OUT_CCC})					ps
100 MHz to 400 MHz	150					
150 FC1152 Package[1]	0 < SSO <=16					
20 MHz to 100 MHz	± 1% x (1/F_{OUT_CCC}))					ps
100 MHz to 400 MHz	120					ps

1. SSO data is based on LVCMOS 2.5 V MSIO and/or MSIOD bank I/Os.

Figure 18 • **Power-up to Functional Timing Diagram for IGLOO2**
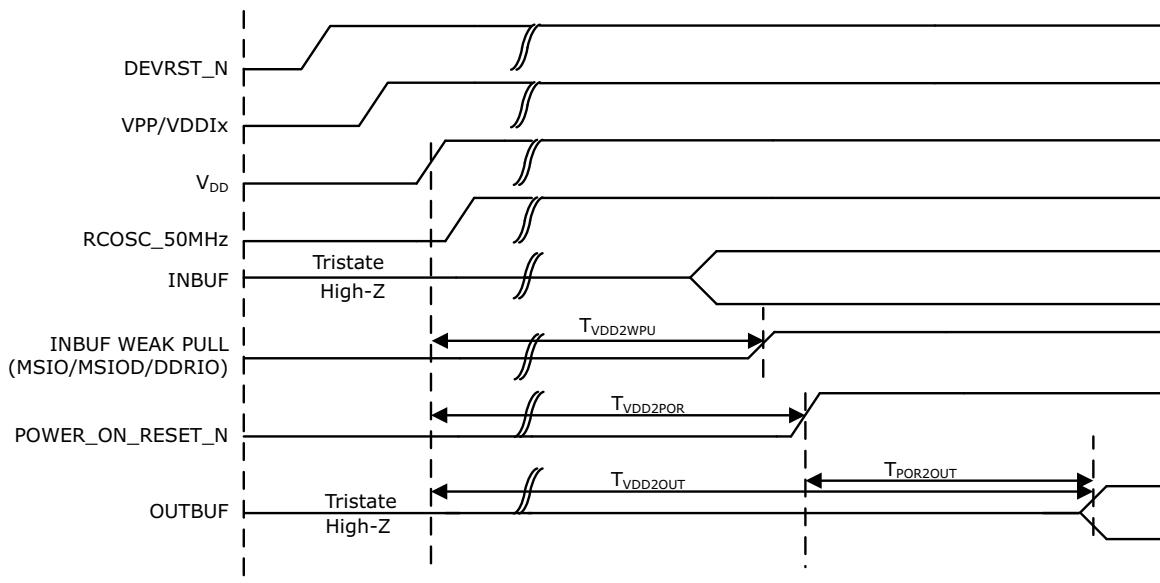
2.3.25 DEVRST_N Characteristics

Table 290 • **DEVRST_N Characteristics for All Devices**

Parameter	Symbol	Max	Unit
DEVRST_N ramp rate	$T_{RAMPDEVRSTN}$	1	us
DEVRST_N cycling rate	$F_{MAXPDEVRSTN}$	100	kHz

2.3.26 DEVRST_N to Functional Times

The following table lists the SmartFusion2 DEVRST_N to functional times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 291 • **DEVRST_N to Functional Times for SmartFusion2**

Symbol	From	To	Description	Maximum Power-up to Functional Time for SmartFusion2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON _RESET_N	Output available at I/O	Fabric to output	518	501	527	521	422	419	694
$T_{POR2MSSRST}$	POWER_ON _RESET_N	MSS_RESE T_N_M2F	Fabric to MSS	515	497	524	518	417	414	689
$T_{MSSRST2OUT}$	MSS_RESET _N_M2F	Output available at I/O	MSS to output	3.5	3.5	3.5	3.3	4.8	4.8	4.8
$T_{DEVRST2OUT}$	DEVRST_N	Output available at I/O	V_{DD} at its minimum threshold level to output	706	768	715	691	641	635	871

The following table lists the SerDes reference clock AC specifications in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 299 • **SerDes Reference Clock AC Specifications**

Parameter	Symbol	Min	Max	Unit
Reference clock frequency	F_{REFCLK}	100	160	MHz
Reference clock rise time	T_{RISE}	0.6	4	V/ns
Reference clock fall time	T_{FALL}	0.6	4	V/ns
Reference clock duty cycle	T_{CYC}	40	60	%
Reference clock mismatch	$M_{MREFCLK}$	−300	300	ppm
Reference spread spectrum clock	SSCref	0	5000	ppm

Table 300 • **HCSL Minimum and Maximum DC Input Levels (Applicable to SerDes REFCLK Only)**

Parameter	Symbol	Min	Typ	Max	Unit
Recommended DC Operating Conditions					
Supply voltage	V_{DDI}	2.375	2.5	2.625	V
HCSL DC Input Voltage Specification					
DC Input voltage	V_I	0		2.625	V
HCSL Differential Voltage Specification					
Input common mode voltage	V_{ICM}	0.05		2.4	V
Input differential voltage	V_{IDIFF}	100		1100	mV

Table 301 • **HCSL Minimum and Maximum AC Switching Speeds (Applicable to SerDes REFCLK Only)**

Parameter	Symbol	Min	Typ	Max	Unit
HCSL AC Specifications					
Maximum data rate (for MSIO I/O bank)	F_{MAX}			350	Mbps
HCSL Impedance Specifications					
Termination resistance	Rt		100		Ω

2.3.31 SmartFusion2 Specifications

2.3.31.1 MSS Clock Frequency

The following table lists the maximum frequency for MSS main clock in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 302 • **Maximum Frequency for MSS Main Clock**

Symbol	Description	−1	−Std	Unit
M3_CLK	Maximum frequency for the MSS main clock	166	142	MHz

2.3.31.3   Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, see Figure 22, page 128.

The following table lists the SPI characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V

Table 305 •   **SPI Characteristics for All Devices**

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0|1]_CLK minimum period					
	SPI_[0|1]_CLK = PCLK/2	12			ns	
	SPI_[0|1]_CLK = PCLK/4	24.1			ns	
	SPI_[0|1]_CLK = PCLK/8	48.2			ns	
	SPI_[0|1]_CLK = PCLK/16	0.1			μs	
	SPI_[0|1]_CLK = PCLK/32	0.19			μs	
	SPI_[0|1]_CLK = PCLK/64	0.39			μs	
	SPI_[0|1]_CLK = PCLK/128	0.77			μs	
sp2	SPI_[0|1]_CLK minimum pulse width high					
	SPI_[0|1]_CLK = PCLK/2	6			ns	
	SPI_[0|1]_CLK = PCLK/4	12.05			ns	
	SPI_[0|1]_CLK = PCLK/8	24.1			ns	
	SPI_[0|1]_CLK = PCLK/16	0.05			μs	
	SPI_[0|1]_CLK = PCLK/32	0.095			μs	
	SPI_[0|1]_CLK = PCLK/64	0.195			μs	
	SPI_[0|1]_CLK = PCLK/128	0.385			μs	
sp3	SPI_[0|1]_CLK minimum pulse width low					
	SPI_[0|1]_CLK = PCLK/2	6			ns	
	SPI_[0|1]_CLK = PCLK/4	12.05			ns	
	SPI_[0|1]_CLK = PCLK/8	24.1			ns	
	SPI_[0|1]_CLK = PCLK/16	0.05			μs	
	SPI_[0|1]_CLK = PCLK/32	0.095			μs	
	SPI_[0|1]_CLK = PCLK/64	0.195			μs	
	SPI_[0|1]_CLK = PCLK/128	0.385			μs	
sp4	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS rise time (10%–90%)[1]		2.77		ns	I/O Configuration: LVCMOS 2.5 V–8 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C

Table 305 • **SPI Characteristics for All Devices** *(continued)*

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp5	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS fall time (10%–90%)[1]		2.906		ns	IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0|1]_DI setup time[2]	12			ns	
sp9m	SPI_[0|1]_DI hold time[2]	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0|1]_DI setup time[2]	2			ns	
sp9s	SPI_[0|1]_DI hold time[2]	7			ns	
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0|1]_DI setup time[2]	15			ns	
sp9m	SPI_[0|1]_DI hold time[2]	−2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) - 3.5			ns	
sp8s	SPI_[0|1]_DI setup time[2]	3			ns	
sp9s	SPI_[0|1]_DI hold time[2]	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

Figure 22 • **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**
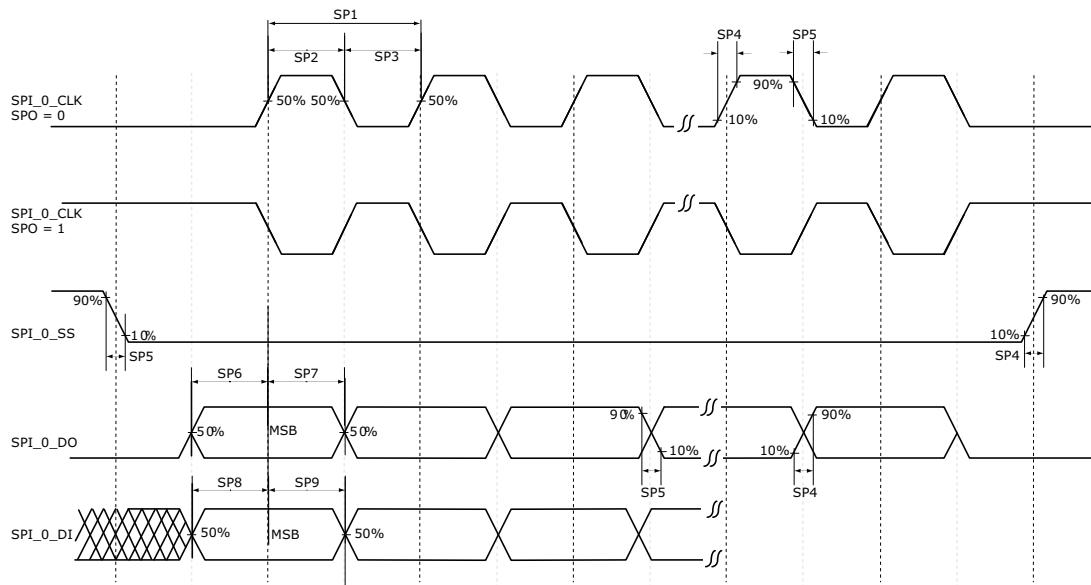
2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 306 • **CAN Controller Characteristics**

Parameter	Description	−1	−Std	Unit
FCANREFCLK[1]	Internally sourced CAN reference clock frequency	160	136	MHz
BAUDCANMAX	Maximum CAN performance baud rate	1	1	Mbps
BAUDCANMIN	Minimum CAN performance baud rate	0.05	0.05	Mbps

1.   PCLK to CAN controller must be a multiple of 8 MHz.

2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 307 • **USB Characteristics**

Parameter	Description	−1	−Std	Unit
FUSBREFCLK	Internally sourced USB reference clock frequency	166	142	MHz
TUSBCLK	USB clock period	16.66	16.66	ns
TUSBPD	Clock to USB data propagation delay	9.0	9.0	ns
TUSBSU	Setup time for USB data	6.0	6.0	ns
TUSBHD	Hold time for USB data	0	0	ns