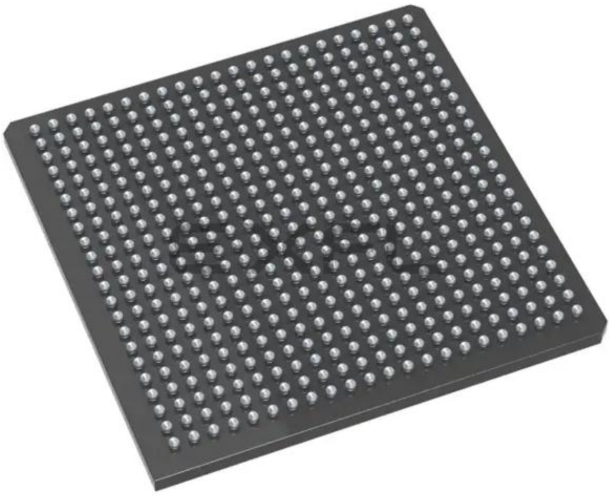
# Microchip Technology - M2S090T-FG484 Datasheet



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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| **Details** | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 512KB |
| RAM Size | 64KB |
| Peripherals | DDR, PCIe, SERDES |
| Connectivity | CANbus, Ethernet, I²C, SPI, UART/USART, USB |
| Speed | 166MHz |
| Primary Attributes | FPGA - 90K Logic Modules |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2s090t-fg484 |

# Contents

# 2 IGLOO2 FPGA and SmartFusion2 SoC FPGA

Microsemi's mainstream SmartFusion®2 SoC and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated math blocks, multiple embedded memory blocks, and high-performance SerDes communication interfaces on a single chip. Both families benefit from low-power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to 5 MBs of embedded RAM, up to 16 SerDes lanes, and up to four PCI Express Gen 2 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 devices integrate an entire low-power, real-time microcontroller subsystem (MSS) with a rich set of industry-standard peripherals including Ethernet, USB, and CAN, while IGLOO2 devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

## 2.1 Device Status

The following table shows the design security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

***Table 1 •*** **IGLOO2 and SmartFusion2 Design Security Densities**

| Design Security Device Densities | Status |
|---|---|
| 005 | Production |
| 010, 010T | Production |
| 025, 025T | Production |
| 050, 050T | Production |
| 060, 060T | Production |
| 090, 090T | Production |
| 150, 150T | Production |

The following table shows the data security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

***Table 2 •*** **IGLOO2 and SmartFusion2 Data Security Densities**

| Data Security Device Densities | Status |
|---|---|
| 005S | Production |
| 010TS | Production |
| 025TS | Production |
| 050TS | Production |
| 060TS | Production |
| 090TS | Production |
| 150TS | Production |

The following table lists the embedded operating flash limits.

**Table 6 • Embedded Operating Flash Limits**

| Product Grade | Element | Programming Temperature | Maximum Operating Temperature | Programming Cycles | Retention (Biased/Unbiased) |
|---|---|---|---|---|---|
| Commercial | Embedded flash | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | < 1000 cycles per page, up to two million cycles per eNVM array | 20 years |
| | | | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | < 10000 cycles per page, up to 20 million cycles per eNVM array | 10 years |
| Industrial | Embedded flash | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | < 1000 cycles per page, up to two million cycles per eNVM array | 20 years |
| | | | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | < 10000 cycles per page, up to 20 million cycles per eNVM array | 10 years |

**Note:** If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

**Table 7 • Device Storage Temperature and Retention**

| Product Grade | Storage Temperature (Tstg) | Retention |
|---|---|---|
| Commercial | Min $T_J$ = 0 °C<br>Max $T_J$ = 85 °C | 20 years |
| Industrial | Min $T_J$ = –40 °C<br>Max $T_J$ = 100 °C | 20 years |

**Table 8 • High Temperature Data Retention (HTR) Lifetime**

| $T_J$ (C) | HTR Lifetime[1] (yrs) |
|---|---|
| 90 | 20.5 |
| 95 | 20.5 |
| 100 | 20.5 |
| 105 | 17.0 |
| 110 | 15.0 |
| 115 | 13.0 |
| 120 | 11.5 |
| 125 | 10.0 |
| 130 | 8.0 |
| 135 | 6.0 |
| 140 | 4.5 |
| 145 | 3.0 |
| 150 | 1.5 |

[1] HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

## 2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

### 2.3.2.1 Quiescent Supply Current

***Table 10 •*** **Quiescent Supply Current Characteristics**

| | Modes and Configurations | |
|---|---|---|
| **Power Supplies/Blocks** | **Non-Flash*Freeze** | **Flash*Freeze** |
| FPGA Core | On | Off |
| $V_{DD}$/SERDES_[01]_VDD[1] | On | On |
| $V_{PP}$/$V_{PPNVM}$ | On | On |
| HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDDA | 0 V | 0 V |
| SERDES_[01]_PLL_VDDA[2] | 0 V | 0 V |
| SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5[2] | On | On |
| SERDES_[01]_L[0123]_VDDAIIO[2] | On | On |
| $V_{DDIx}$[3, 4] | On | On |
| $V_{REFx}$ | On | On |
| MSSDDR CLK | 32 kHz | 32 kHz |
| RAM | On | Sleep state |
| System controller | 50 MHz | 50 MHz |
| 50 MHz oscillator (enable/disable) | Enable | Disabled |
| 1 MHz oscillator (enable/disable) | Disabled | Disabled |
| Crystal oscillator (enable/disable) | Disabled | Disabled |

1. SERDES_[01]_VDD Power Supply is shorted to $V_{DD}$.
2. SerDes and DDR blocks to be unused.
3. $V_{DDIx}$ has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate $V_{DDI}$ bank supplies. For details on bank power supplies, see “Recommendation for Unused Bank Supplies” table in the *AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

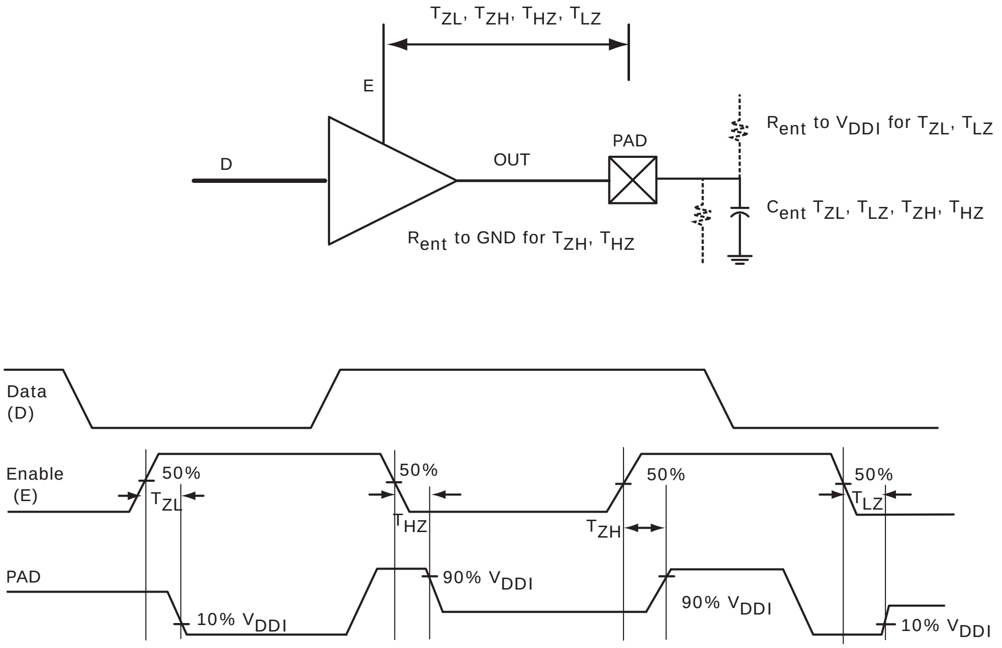
***Table 11 •*** **SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD}$ = 1.2 V) – Typical Process**

| Symbol | Modes | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| IDC1 | Non-Flash*Freeze | 6.2 | 6.9 | 8.9 | 13.1 | 15.3 | 15.4 | 27.5 | mA | Typical ($T_J$ = 25 °C) |
| | | 24.0 | 28.4 | 40.6 | 67.8 | 80.6 | 81.4 | 144.7 | mA | Commercial ($T_J$ = 85 °C) |
| | | 35.2 | 41.9 | 60.5 | 102.1 | 121.4 | 122.6 | 219.1 | mA | Industrial ($T_J$ = 100 °C) |

### 2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

***Figure 5 •*** **Tristate Buffer for Enable Path Test Point**



### 2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

***Table 18 •*** **Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| PCI 3.3 V | 630 | | | Mbps |
| LVTTL 3.3 V | 600 | | | Mbps |
| LVCMOS 3.3 V | 600 | | | Mbps |
| LVCMOS 2.5 V | 410 | 420 | 400 | Mbps |
| LVCMOS 1.8 V | 295 | 400 | 400 | Mbps |
| LVCMOS 1.5 V | 160 | 220 | 235 | Mbps |
| LVCMOS 1.2 V | 120 | 160 | 200 | Mbps |
| LPDDR-LVCMOS 1.8 V mode | | | 400 | Mbps |

***Table 43 •*** **LVCMOS 2.5 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 1.2 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ωσ |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

***Table 44 •*** **LVCMOS 2.5 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|---|---|---|---|---|---|---|
| **MSIO I/O Bank** | **MSIOD I/O Bank** | **DDRIO I/O Bank (With Software Default Fixed Code)** | **Min** | **Max** | | |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ – 0.4 | 0.4 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ – 0.4 | 0.4 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI}$ – 0.4 | 0.4 | 6 | 6 |
| 8 mA | 8 mA | 8 mA | $V_{DDI}$ – 0.4 | 0.4 | 8 | 8 |
| 12 mA | 12 mA | 12 mA | $V_{DDI}$ – 0.4 | 0.4 | 12 | 12 |
| 16 mA | | 16 mA | $V_{DDI}$ – 0.4 | 0.4 | 16 | 16 |

**Note:** For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at: www.microsemi.com/soc/download/ibis/default.aspx.

### AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

***Table 45 •*** **LVCMOS 2.5 V Receiver Characteristics (Input Buffers)**

| | On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | Unit |
|---|---|---|---|---|---|---|
| | | **–1** | **–Std** | **–1** | **–Std** | |
| **LVCMOS 2.5 V (for DDRIO I/O bank)** | None | 1.823 | 2.145 | 1.932 | 2.274 | ns |
| **LVCMOS 2.5 V (for MSIO I/O bank)** | None | 2.486 | 2.925 | 2.495 | 2.935 | ns |
| **LVCMOS 2.5 V (for MSIOD I/O bank)** | None | 2.29 | 2.694 | 2.305 | 2.712 | ns |

***Table 46 •*** **LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | |
| 2 mA | Slow | 3.657 | 4.302 | 3.393 | 3.991 | 3.675 | 4.323 | 3.894 | 4.582 | 3.552 | 4.18 | ns |
| | Medium | 3.374 | 3.97 | 3.139 | 3.693 | 3.396 | 3.995 | 3.635 | 4.277 | 3.253 | 3.828 | ns |
| | Medium fast | 3.239 | 3.811 | 3.036 | 3.572 | 3.261 | 3.836 | 3.519 | 4.141 | 3.128 | 3.681 | ns |
| | Fast | 3.224 | 3.793 | 3.029 | 3.563 | 3.246 | 3.818 | 3.512 | 4.132 | 3.119 | 3.67 | ns |

**Table 57 • LVCMOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 4.234 | 4.981 | 3.646 | 4.29 | 4.245 | 4.995 | 4.908 | 5.774 | 4.434 | 5.216 | ns |
| | Medium | 3.824 | 4.498 | 3.282 | 3.861 | 3.834 | 4.511 | 4.625 | 5.441 | 4.116 | 4.843 | ns |
| | Medium fast | 3.627 | 4.267 | 3.111 | 3.66 | 3.637 | 4.279 | 4.481 | 5.272 | 3.984 | 4.687 | ns |
| | Fast | 3.605 | 4.241 | 3.097 | 3.644 | 3.615 | 4.253 | 4.472 | 5.262 | 3.973 | 4.674 | ns |
| 4 mA | Slow | 3.923 | 4.615 | 3.314 | 3.9 | 3.918 | 4.61 | 5.403 | 6.356 | 4.894 | 5.757 | ns |
| | Medium | 3.518 | 4.138 | 2.961 | 3.484 | 3.515 | 4.135 | 5.121 | 6.025 | 4.561 | 5.366 | ns |
| | Medium fast | 3.321 | 3.907 | 2.783 | 3.275 | 3.317 | 3.903 | 4.966 | 5.843 | 4.426 | 5.206 | ns |
| | Fast | 3.301 | 3.883 | 2.77 | 3.259 | 3.296 | 3.878 | 4.957 | 5.831 | 4.417 | 5.196 | ns |
| 6 mA | Slow | 3.71 | 4.364 | 3.104 | 3.652 | 3.702 | 4.355 | 5.62 | 6.612 | 5.08 | 5.977 | ns |
| | Medium | 3.333 | 3.921 | 2.779 | 3.27 | 3.325 | 3.913 | 5.346 | 6.289 | 4.777 | 5.62 | ns |
| | Medium fast | 3.155 | 3.712 | 2.62 | 3.083 | 3.146 | 3.702 | 5.21 | 6.13 | 4.657 | 5.479 | ns |
| | Fast | 3.134 | 3.688 | 2.608 | 3.068 | 3.125 | 3.677 | 5.202 | 6.12 | 4.648 | 5.468 | ns |
| 8 mA | Slow | 3.619 | 4.258 | 3.007 | 3.538 | 3.607 | 4.244 | 5.815 | 6.841 | 5.249 | 6.175 | ns |
| | Medium | 3.246 | 3.819 | 2.686 | 3.16 | 3.236 | 3.807 | 5.542 | 6.52 | 4.936 | 5.807 | ns |
| | Medium fast | 3.066 | 3.607 | 2.525 | 2.971 | 3.054 | 3.593 | 5.405 | 6.359 | 4.811 | 5.66 | ns |
| | Fast | 3.046 | 3.584 | 2.513 | 2.957 | 3.034 | 3.57 | 5.401 | 6.353 | 4.803 | 5.651 | ns |
| 10 mA | Slow | 3.498 | 4.115 | 2.878 | 3.386 | 3.481 | 4.096 | 6.046 | 7.113 | 5.444 | 6.404 | ns |
| | Medium | 3.138 | 3.692 | 2.569 | 3.023 | 3.126 | 3.678 | 5.782 | 6.803 | 5.129 | 6.034 | ns |
| | Medium fast | 2.966 | 3.489 | 2.414 | 2.841 | 2.951 | 3.472 | 5.666 | 6.665 | 5.013 | 5.897 | ns |
| | Fast | 2.945 | 3.464 | 2.401 | 2.826 | 2.93 | 3.448 | 5.659 | 6.658 | 5.003 | 5.886 | ns |
| 12 mA | Slow | 3.417 | 4.02 | 2.807 | 3.303 | 3.401 | 4.002 | 6.083 | 7.156 | 5.464 | 6.428 | ns |
| | Medium | 3.076 | 3.618 | 2.519 | 2.964 | 3.063 | 3.604 | 5.828 | 6.856 | 5.176 | 6.089 | ns |
| | Medium fast | 2.913 | 3.427 | 2.376 | 2.795 | 2.898 | 3.41 | 5.725 | 6.736 | 5.072 | 5.966 | ns |
| | Fast | 2.894 | 3.405 | 2.362 | 2.78 | 2.879 | 3.388 | 5.715 | 6.724 | 5.064 | 5.957 | ns |
| 16 mA | Slow | 3.366 | 3.96 | 2.751 | 3.237 | 3.348 | 3.939 | 6.226 | 7.324 | 5.576 | 6.56 | ns |
| | Medium | 3.03 | 3.565 | 2.47 | 2.906 | 3.017 | 3.55 | 5.981 | 7.036 | 5.282 | 6.214 | ns |
| | Medium fast | 2.87 | 3.377 | 2.328 | 2.739 | 2.854 | 3.358 | 5.895 | 6.935 | 5.18 | 6.094 | ns |
| | Fast | 2.853 | 3.357 | 2.314 | 2.723 | 2.837 | 3.338 | 5.889 | 6.929 | 5.177 | 6.09 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 58 • LVCMOS 1.8 V Transmitter Characteristics for MSIO I/O Bank**

| Output Drive Selection | Slew Control | $T_{DP}$ –1 | $T_{DP}$ –Std | $T_{ZL}$ –1 | $T_{ZL}$ –Std | $T_{ZH}$ –1 | $T_{ZH}$ –Std | $T_{HZ}$[1] –1 | $T_{HZ}$[1] –Std | $T_{LZ}$[1] –1 | $T_{LZ}$[1] –Std | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Slow | 3.441 | 4.047 | 4.165 | 4.9 | 4.413 | 5.192 | 4.891 | 5.755 | 5.138 | 6.044 | ns |
| 4 mA | Slow | 3.218 | 3.786 | 3.642 | 4.284 | 3.941 | 4.636 | 5.665 | 6.665 | 5.568 | 6.551 | ns |
| 6 mA | Slow | 3.141 | 3.694 | 3.501 | 4.118 | 3.823 | 4.498 | 6.587 | 7.75 | 6.032 | 7.096 | ns |
| 8 mA | Slow | 3.165 | 3.723 | 3.319 | 3.904 | 3.654 | 4.298 | 6.898 | 8.115 | 6.216 | 7.313 | ns |
| 10 mA | Slow | 3.202 | 3.767 | 3.278 | 3.857 | 3.616 | 4.254 | 7.25 | 8.529 | 6.435 | 7.571 | ns |
| 12 mA | Slow | 3.277 | 3.855 | 3.175 | 3.736 | 3.519 | 4.139 | 7.392 | 8.697 | 6.538 | 7.692 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**Table 59 • LVCMOS 1.8 V Transmitter Characteristics for MSIOD I/O Bank**

| Output Drive Selection | Slew Control | $T_{DP}$ –1 | $T_{DP}$ –Std | $T_{ZL}$ –1 | $T_{ZL}$ –Std | $T_{ZH}$ –1 | $T_{ZH}$ –Std | $T_{HZ}$[1] –1 | $T_{HZ}$[1] –Std | $T_{LZ}$[1] –1 | $T_{LZ}$[1] –Std | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Slow | 2.725 | 3.206 | 3.316 | 3.901 | 3.484 | 4.099 | 5.204 | 6.123 | 4.997 | 5.88 | ns |
| 4 mA | Slow | 2.242 | 2.638 | 2.777 | 3.267 | 2.947 | 3.466 | 5.729 | 6.74 | 5.448 | 6.41 | ns |
| 6 mA | Slow | 1.995 | 2.347 | 2.466 | 2.901 | 2.63 | 3.094 | 6.372 | 7.496 | 5.987 | 7.043 | ns |
| 8 mA | Slow | 2.001 | 2.354 | 2.44 | 2.87 | 2.6 | 3.058 | 6.633 | 7.804 | 6.193 | 7.286 | ns |
| 10 mA | Slow | 2.025 | 2.382 | 2.312 | 2.719 | 2.47 | 2.906 | 6.94 | 8.165 | 6.412 | 7.544 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.9 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

**Table 60 • LVCMOS 1.5 V DC Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.425 | 1.5 | 1.575 | V |

**Table 61 • LVCMOS 1.5 V DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high for (MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 1.575 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.35 × $V_{DDI}$ | V |
| Input current high[1] | $I_{IH}$ (DC) | | | – |
| Input current low[1] | $I_{IL}$ (DC | | | – |

1. See Table 24, page 22.

***Table 100 •*** **HSTL AC Test Parameter Specification**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for HSTL15 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for HSTL15 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**AC Switching Characteristics**

Worst-case commercial conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, worst-case $V_{DDI}$.

***Table 101 •*** **HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)**

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| Pseudo differential | None | 1.605 | 1.888 | ns |
| | 47.8 | 1.614 | 1.898 | ns |
| True differential | None | 1.622 | 1.909 | ns |
| | 47.8 | 1.628 | 1.916 | ns |

***Table 102 •*** **HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| **HSTL Class I** | | | | | | | | | | | |
| Single-ended | 2.6 | 3.059 | 2.514 | 2.958 | 2.514 | 2.958 | 2.431 | 2.86 | 2.431 | 2.86 | ns |
| Differential | 2.621 | 3.083 | 2.648 | 3.115 | 2.647 | 3.113 | 2.925 | 3.442 | 2.923 | 3.44 | ns |
| **HSTL Class II** | | | | | | | | | | | |
| Single-ended | 2.511 | 2.954 | 2.488 | 2.927 | 2.49 | 2.93 | 2.409 | 2.833 | 2.411 | 2.836 | ns |
| Differential | 2.528 | 2.974 | 2.552 | 3.003 | 2.551 | 3.001 | 2.897 | 3.409 | 2.896 | 3.408 | ns |

### 2.3.6.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V.

***Table 180 •*** **B-LVDS AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.738 | 3.221 | ns |
| 100 | 2.735 | 3.218 | ns |

***Table 181 •*** **B-LVDS AC Switching Characteristics for Receiver for MSIOD I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.495 | 2.934 | ns |
| 100 | 2.495 | 2.935 | ns |

***Table 182 •*** **B-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2.258 | 2.656 | 2.343 | 2.756 | 2.329 | 2.74 | 2.12 | 2.494 | 2.123 | 2.497 | ns |

### 2.3.7.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

**Minimum and Maximum Input and Output Levels**

***Table 183 •*** **M-LVDS Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage[1] | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

1. Only M-LVDS TYPE I is supported.

***Table 184 •*** **M-LVDS DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 2.925 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[2] | $I_{IL}$ (DC) | | | |

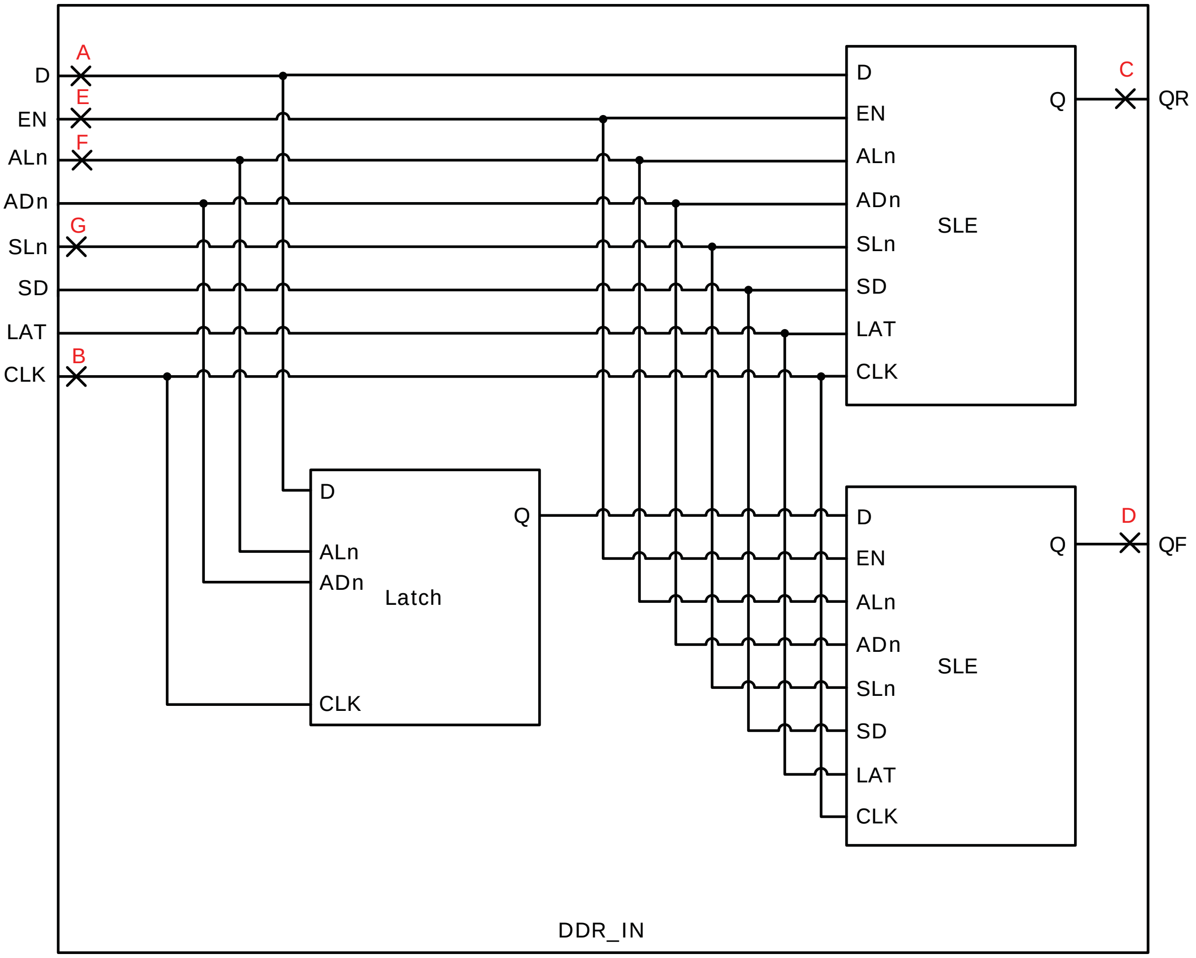
1. See Table 24, page 22.

## 2.3.9 DDR Module Specification

This section describes input and output DDR module and timing specifications.

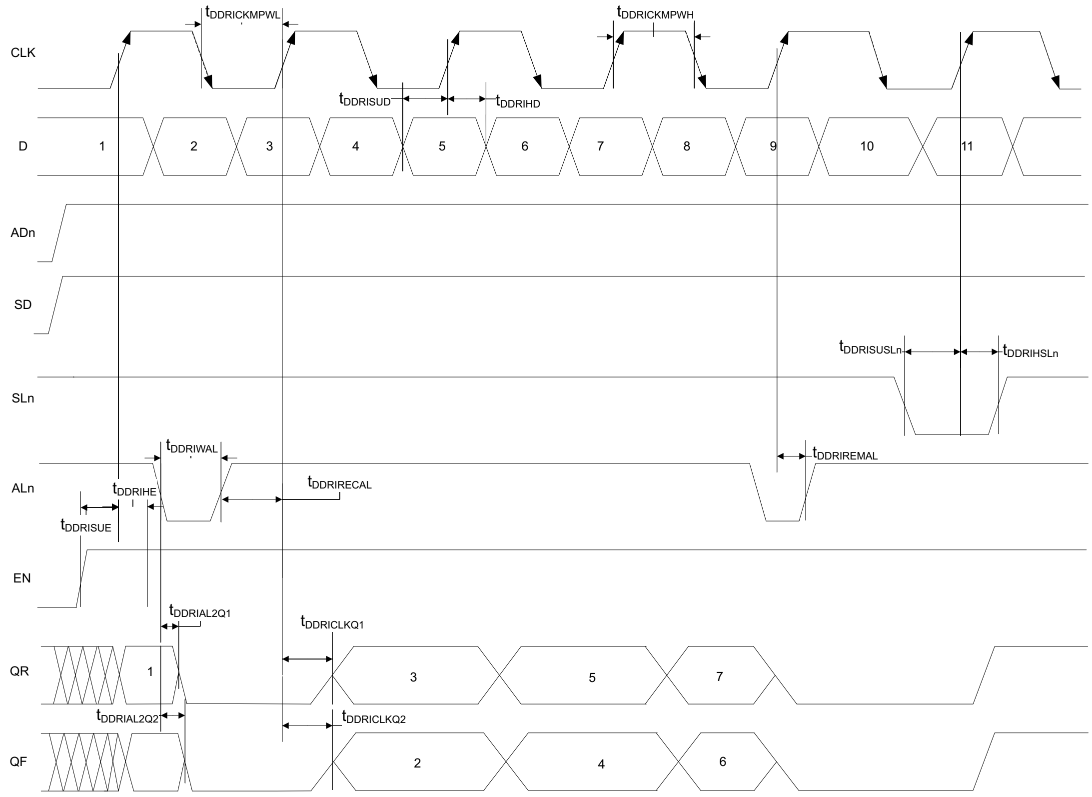
### 2.3.9.1 Input DDR Module

***Figure 10 •*** **Input DDR Module**



### 2.3.9.2 Input DDR Timing Diagram

***Figure 11 •*** **Input DDR Timing Diagram**



### 2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 221 •*** **Input DDR Propagation Delays**

| Symbol | Description | Measuring Nodes (from, to) | –1 | –Std | Unit |
|---|---|---|---|---|---|
| $T_{DDRICLKQ1}$ | Clock-to-Out Out_QR for input DDR | B, C | 0.16 | 0.188 | ns |
| $T_{DDRICLKQ2}$ | Clock-to-Out Out_QF for input DDR | B, D | 0.166 | 0.195 | ns |
| $T_{DDRISUD}$ | Data setup for input DDR | A, B | 0.357 | 0.421 | ns |
| $T_{DDRIHD}$ | Data hold for input DDR | A, B | 0 | 0 | ns |
| $T_{DDRISUE}$ | Enable setup for input DDR | E, B | 0.46 | 0.542 | ns |
| $T_{DDRIHE}$ | Enable hold for input DDR | E, B | 0 | 0 | ns |
| $T_{DDRISUSLN}$ | Synchronous load setup for input DDR | G, B | 0.46 | 0.542 | ns |
| $T_{DDRIHSLN}$ | Synchronous load hold for input DDR | G, B | 0 | 0 | ns |
| $T_{DDRIAL2Q1}$ | Asynchronous load-to-out QR for input DDR | F, C | 0.587 | 0.69 | ns |
| $T_{DDRIAL2Q2}$ | Asynchronous load-to-out QF for input DDR | F, D | 0.541 | 0.636 | ns |
| $T_{DDRIREMAL}$ | Asynchronous load removal time for input DDR | F, B | 0 | 0 | ns |
| $T_{DDRIRECAL}$ | Asynchronous load recovery time for input DDR | F, B | 0.074 | 0.087 | ns |

**Table 232 •** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Address setup time | $T_{ADDRSU}$ | 0.475 | | 0.559 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.336 | | 0.395 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.529 | | 1.799 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.485 | | 0.57 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.514 | | 1.781 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.415 | | 0.488 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

**Table 233 •** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |

The following table lists the RAM1K18 – two-port mode for depth × width configuration 512 × 36 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 236 •*** **RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.334 | | 0.393 | ns |
| Read access time without pipeline register | | | 2.25 | | 2.647 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.313 | | 0.368 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.337 | | 0.396 | | ns |
| Data hold time | $T_{DHD}$ | 0.111 | | 0.13 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.201 | | 0.237 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.25 | | 2.647 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.449 | | 0.528 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.167 | | 0.197 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.506 | | 1.772 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.39 | | 0.458 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.242 | | 0.285 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

***Table 243* • μSRAM (RAM1024x1) in 1024 × 1 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.83 | | 0.98 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.003 | | 0.004 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.137 | | 0.161 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.247 | | 0.29 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.03 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

## 2.3.13 Programming Times

The following tables list the programming times in typical conditions when $T_J$ = 25 °C, $V_{DD}$ = 1.2 V. External SPI flash part# AT25DF641-s3H is used during this measurement.

***Table 244* • JTAG Programming (Fabric Only)**

| **M2S/M2GL Device** | **Image size Bytes** | **Program** | **Verify** | **Unit** |
|---|---|---|---|---|
| 005 | 302672 | 22 | 10 | Sec |
| 010 | 568784 | 28 | 18 | Sec |
| 025 | 1223504 | 51 | 26 | Sec |
| 050 | 2424832 | 66 | 54 | Sec |
| 060 | 2418896 | 77 | 54 | Sec |
| 090 | 3645968 | 113 | 126 | Sec |
| 150 | 6139184 | 155 | 193 | Sec |

**Table 248 •** **2 Step IAP Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 137536 | 2 | 37 | 5 | Sec |
| 010 | 274816 | 4 | 76 | 11 | Sec |
| 025 | 274816 | 4 | 78 | 10 | Sec |
| 050 | 278528 | 3 | 85 | 9 | Sec |
| 060 | 268480 | 5 | 76 | 22 | Sec |
| 090 | 544496 | 10 | 152 | 43 | Sec |
| 150 | 544496 | 10 | 153 | 44 | Sec |

**Table 249 •** **2 Step IAP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 439296 | 6 | 56 | 11 | Sec |
| 010 | 842688 | 11 | 100 | 21 | Sec |
| 025 | 1497408 | 19 | 113 | 32 | Sec |
| 050 | 2695168 | 32 | 136 | 48 | Sec |
| 060 | 2686464 | 43 | 137 | 70 | Sec |
| 090 | 4190208 | 68 | 236 | 115 | Sec |
| 150 | 6682768 | 109 | 286 | 162 | Sec |

**Table 250 •** **SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 302672 | 6 | 19 | 8 | Sec |
| 010 | 568784 | 10 | 26 | 14 | Sec |
| 025 | 1223504 | 21 | 39 | 29 | Sec |
| 050 | 2424832 | 39 | 60 | 50 | Sec |
| 060 | 2418896 | 44 | 65 | 54 | Sec |
| 090 | 3645968 | 66 | 90 | 79 | Sec |
| 150 | 6139184 | 108 | 140 | 128 | Sec |

**Table 251 •** **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 137536 | 3 | 42 | 4 | Sec |
| 010 | 274816 | 4 | 82 | 7 | Sec |
| 025 | 274816 | 4 | 82 | 8 | Sec |
| 050 | 278528 | 4 | 80 | 8 | Sec |
| 060 | 268480 | 6 | 80 | 8 | Sec |
| 090 | 544496 | 10 | 157 | 15 | Sec |

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

*Table 270 •* **Math Block with Input Register Used and Output in Bypass Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input register setup time | $T_{MISU}$ | 0.149 | | 0.176 | | ns |
| Input register hold time | $T_{MIHD}$ | 0.185 | | 0.218 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | 0.08 | | 0.094 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | –0.012 | | –0.014 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | –0.005 | | –0.005 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.088 | | 0.104 | | ns |
| Input register clock to output delay | $T_{MICQ}$ | | 2.52 | | 2.964 | ns |
| CDIN to output delay | $T_{MCDIN2Q}$ | | 1.951 | | 2.295 | ns |

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

*Table 271 •* **Math Block with Input and Output in Bypass Mode**

| | | –1 | –Std | |
|---|---|---|---|---|
| **Parameter** | **Symbol** | **Max** | **Max** | **Unit** |
| Input to output delay | $T_{MIQ}$ | 2.568 | 3.022 | ns |
| CDIN to output delay | $T_{MCDIN2Q}$ | 1.951 | 2.295 | ns |

## 2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when $V_{DD}$ = 1.14 V, $V_{PPNVM}$ = $V_{PP}$ = 2.375 V.

*Table 272 •* **eNVM Read Performance**

| | | Operating Temperature Range | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Description** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| $T_J$ | Junction temperature range | –55 °C to 125 °C | | –40 °C to 100 °C | | 0 °C to 85 °C | | °C |
| $F_{MAXREAD}$ | eNVM maximum read frequency | 25 | 25 | 25 | 25 | 25 | 25 | MHz |

The following table lists the eNVM page programming in worst-case conditions when $V_{DD}$ = 1.14 V, $V_{PPNVM}$ = $V_{PP}$ = 2.375 V.

*Table 273 •* **eNVM Page Programming**

| | | Operating Temperature Range | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Description** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| $T_J$ | Junction temperature range | –55 °C to 125 °C | | –40 °C to 100 °C | | 0 °C to 85 °C | | °C |
| $T_{PAGEPGM}$ | eNVM page programming time | 40 | 40 | 40 | 40 | 40 | 40 | ms |

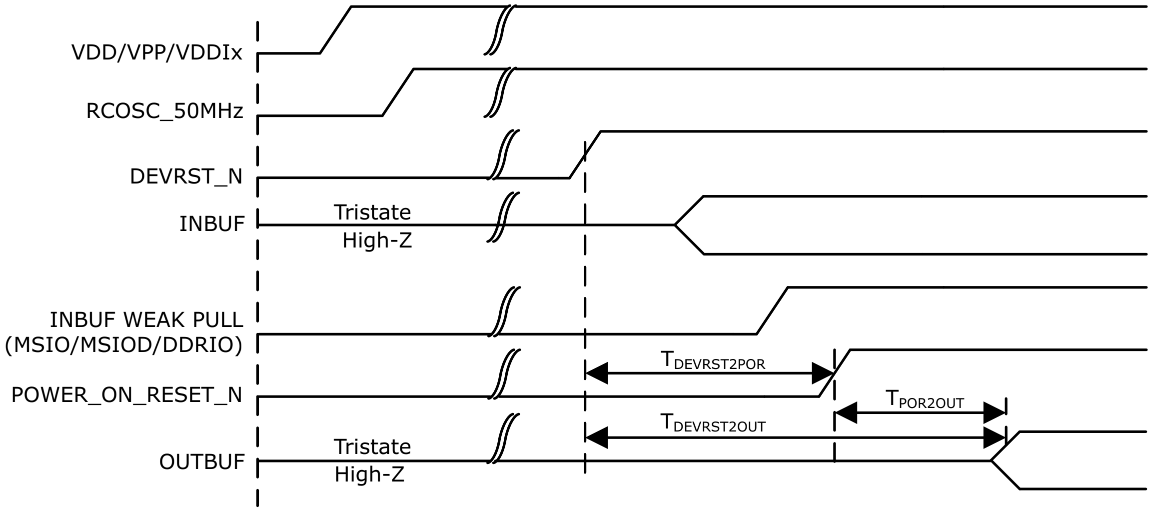
## 2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 282 •*** **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Clock conditioning circuitry input frequency $F_{IN\_CCC}$ | 1 | | 200 | MHz | All CCC |
| | 0.032 | | 200 | MHz | 32 kHz capable CCC |
| Clock conditioning circuitry output frequency $F_{OUT\_CCC}{}^1$ | 0.078 | | 400 | MHz | |
| PLL VCO frequency$^2$ | 500 | | 1000 | MHz | |
| Delay increments in programmable delay blocks | | 75 | 100 | ps | |
| Number of programmable values in each programmable delay block | | | 64 | | |
| Acquisition time | | 70 | 100 | µs | $F_{IN}$ >= 1 MHz |
| | | 1 | 16 | ms | $F_{IN}$ = 32 kHz |
| Input duty cycle (reference clock) | | | | | Internal Feedback |
| | 10 | | 90 | % | 1 MHz ≤ $F_{IN\_CCC}$ ≤ 25 MHz |
| | 25 | | 75 | % | 25 MHz ≤ $F_{IN\_CCC}$≤ 100 MHz |
| | 35 | | 65 | % | 100 MHz ≤ $F_{IN\_CCC}$ ≤ 150 MHz |
| | 45 | | 55 | % | 150 MHz ≤ $F_{IN\_CCC}$ ≤ 200 MHz |
| | | | | | External Feedback (CCC, FPGA, Off-chip) |
| | 25 | | 75 | % | 1 MHz ≤ $F_{IN\_CCC}$ ≤ 25 MHz |
| | 35 | | 65 | % | 25 MHz ≤ $F_{IN\_CCC}$ ≤ 35 MHz |
| | 45 | | 55 | % | 35 MHz ≤ $F_{IN\_CCC}$ ≤ 50 MHz |
| Output duty cycle | 48 | | 52 | % | 050 devices $F_{OUT}$ ≤ 400 MHz |
| | 48 | | 52 | % | 005, 010, and 025 devices<br>$F_{OUT}$ < 350 MHz |
| | 46 | | 54 | % | 005, 010, and 025 devices<br>350 MHz ≤ $F_{out}$ ≤ 400 MHz |
| | 48 | | 52 | % | 060 and 090 devices<br>$F_{OUT}$ ≤ 100 MHz |
| | 44 | | 52 | % | 060 and 090 devices<br>100 MHz ≤ $F_{OUT}$ ≤ 400 MHz |
| | 48 | | 52 | % | 150 devices<br>$F_{OUT}$ ≤ 120 MHz |
| | 45 | | 52 | % | 150 devices<br>120 MHz ≤ $F_{OUT}$ ≤ 400 MHz |
| **Spread Spectrum Characteristics** | | | | | |
| Modulation frequency range | 25 | 35 | 50 | k | |
| Modulation depth range | 0 | | 1.5 | % | |
| Modulation depth control | | 0.5 | | % | |

***Figure 20 •*** **DEVRST_N to Functional Timing Diagram for IGLOO2**



## 2.3.27 Flash*Freeze Timing Characteristics

The following table lists the Flash*Freeze entry and exit times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 293 •*** **Flash*Freeze Entry and Exit Times**

| | | **Entry/Exit Timing FCLK = 100MHz** | | **Entry/Exit Timing FCLK = 3 MHz** | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **005, 010, 025, 060, 090, and 150** | **050** | **All Devices** | **Unit** | **Conditions** |
| Entry time | TFF_ENTRY | 160 | 150 | 320 | µs | eNVM and MSS/HPMS PLL = ON |
| | | 215 | 200 | 430 | µs | eNVM and MSS/HPMS PLL= OFF |
| Exit time with respect to the MSS PLL Lock | TFF_EXIT | 100 | 100 | 140 | µs | eNVM and MSS/HPMS PLL = ON during F*F |
| | | 136 | 120 | 190 | µs | eNVM = ON and MSS/HPMS PLL = OFF during F*F and MSS/HPMS PLL turned back on at exit |
| | | 200 | 200 | 285 | µs | eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit |
| | | 200 | 200 | 285 | µs | eNVM = OFF and MSS/HPMS PLL = ON during F*F and eNVM turned back on at exit |

**Table 305 • SPI Characteristics for All Devices *(continued)***

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| sp5 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS fall time (10%–90%)[1] | | 2.906 | | ns | IO Configuration: LVCMOS 2.5 V-8 mA<br>AC Loading: 35 pF<br>Test Conditions: Typical Voltage, 25 °C |
| SPI master configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 8.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 2.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 12 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |
| SPI slave configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 17.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) + 3.0 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 2 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 7 | | | ns | |
| SPI master configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 7.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 9.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 15 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | —2.5 | | | ns | |
| SPI slave configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 16.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) - 3.5 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 3 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |

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1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.