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Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f26k83-e-ss

TABLE 1: **PIC18(L)FXXK83 FAMILY TYPES**

Device	Data Sheet Index	Program Flash Memory (KB)	Data EEPROM (B)	Data SRAM (bytes)	I/O Pins	12-bit ADC^2 (ch)	5-bit DAC	Comparator	8-bit/ (with HLT)/16-bit Timer	Window Watchdog Timer (WWDT)	Signal Measurement Timer (SMT)	CCP/10-bit PWM	CWG	NCO	CLC	Zero-Cross Detect	Direct Memory Access (DMA)	Memory Access Partition	Vectored Interrupts	CAN	UART with Protocols	I^{2}C/SPI	Peripheral Pin Select	Peripheral Module Disable	Debug$^{(1)}$
PIC18(L)F25K83	(A)	32	1024	2048	25	24	1	2	3/3	Y	Y	4/4	1	1	4	Y	2	Y	Y	Y	2	1/1	Y	Y	I
PIC18(L)F26K83	(A)	64	1024	4096	25	24	1	2	3/3	Y	Y	4/4	1	1	4	Y	2	Y	Y	Y	2	1/1	Y	Y	I

Note 1: I - Debugging integrated on chip.

Data Sheet Index:

  A: DS40001943 PIC18(L)F25/26K83 Data Sheet, 28-Pin

Note: For other small form-factor package availability and marking information, visit
http://www.microchip.com/packaging or contact your local sales office.

REGISTER 5-5: **CONFIGURATION WORD 3L (30 0004h)**

U-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	WDTE<1:0>		WDTCPS<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **Unimplemented:** Read as '1'

bit 6-5   **WDTE<1:0>:** WDT Operating Mode bits

00 = WDT is disabled, SWDTEN is ignored
01 = WDT is enabled/disabled by the SWDTEN bit in WDTCON0
10 = WDT is enabled while Sleep = 0, suspended when Sleep = 1; SWDTEN is ignored
11 = WDT is enabled regardless of Sleep; SWDTEN is ignored

bit 4-0   **WDTCPS<4:0>:** WDT Period Select bits

| WDTCPS<4:0>	WDTPS at POR			Software Control of WDTPS?
	Value	Divider Ratio		Typical Time-out (F_{IN} = 31 kHz)	
00000	00000	1:32	2^5	1 ms	
00001	00001	1:64	2^6	2 ms	
00010	00010	1:128	2^7	4 ms	
00011	00011	1:256	2^8	8 ms	
00100	00100	1:512	2^9	16 ms	
00101	00101	1:1024	2^{10}	32 ms	
00110	00110	1:2048	2^{11}	64 ms	
00111	00111	1:4096	2^{12}	128 ms	
01000	01000	1:8192	2^{13}	256 ms	
01001	01001	1:16384	2^{14}	512 ms	No
01010	01010	1:32768	2^{15}	1s	
01011	01011	1:65536	2^{16}	2s	
01100	01100	1:131072	2^{17}	4s	
01101	01101	1:262144	2^{18}	8s	
01110	01110	1:524299	2^{19}	16s	
01111	01111	1:1048576	2^{20}	32s	
10000	10000	1:2097152	2^{21}	64s	
10001	10001	1:4194304	2^{22}	128s	
10010	10010	1:8388608	2^{23}	256s	
10011 ... 11110	10011 ... 11110	1:32	2^5	1 ms	No
11111	01011	1:65536	2^{16}	2s	Yes

6.11 Start-up Sequence

Upon the release of a POR or BOR, the following must occur before the device will begin executing:

1. Power-up Timer runs to completion (if enabled).
2. Oscillator start-up timer runs to completion (if required for selected oscillator source).
3. $\overline{\text{MCLR}}$ must be released (if enabled).

The total time out will vary based on oscillator configuration and Power-up Timer configuration. See **Section 7.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for more information.

The Power-up Timer and oscillator start-up timer run independently of $\overline{\text{MCLR}}$ Reset. If $\overline{\text{MCLR}}$ is kept low long enough, the Power-up Timer and oscillator Start-up Timer will expire. Upon bringing $\overline{\text{MCLR}}$ high, the device will begin execution after 10 FOSC cycles (see Figure 6-4). This is useful for testing purposes or to synchronize more than one device operating in parallel.

FIGURE 6-4:   **RESET START-UP SEQUENCE**
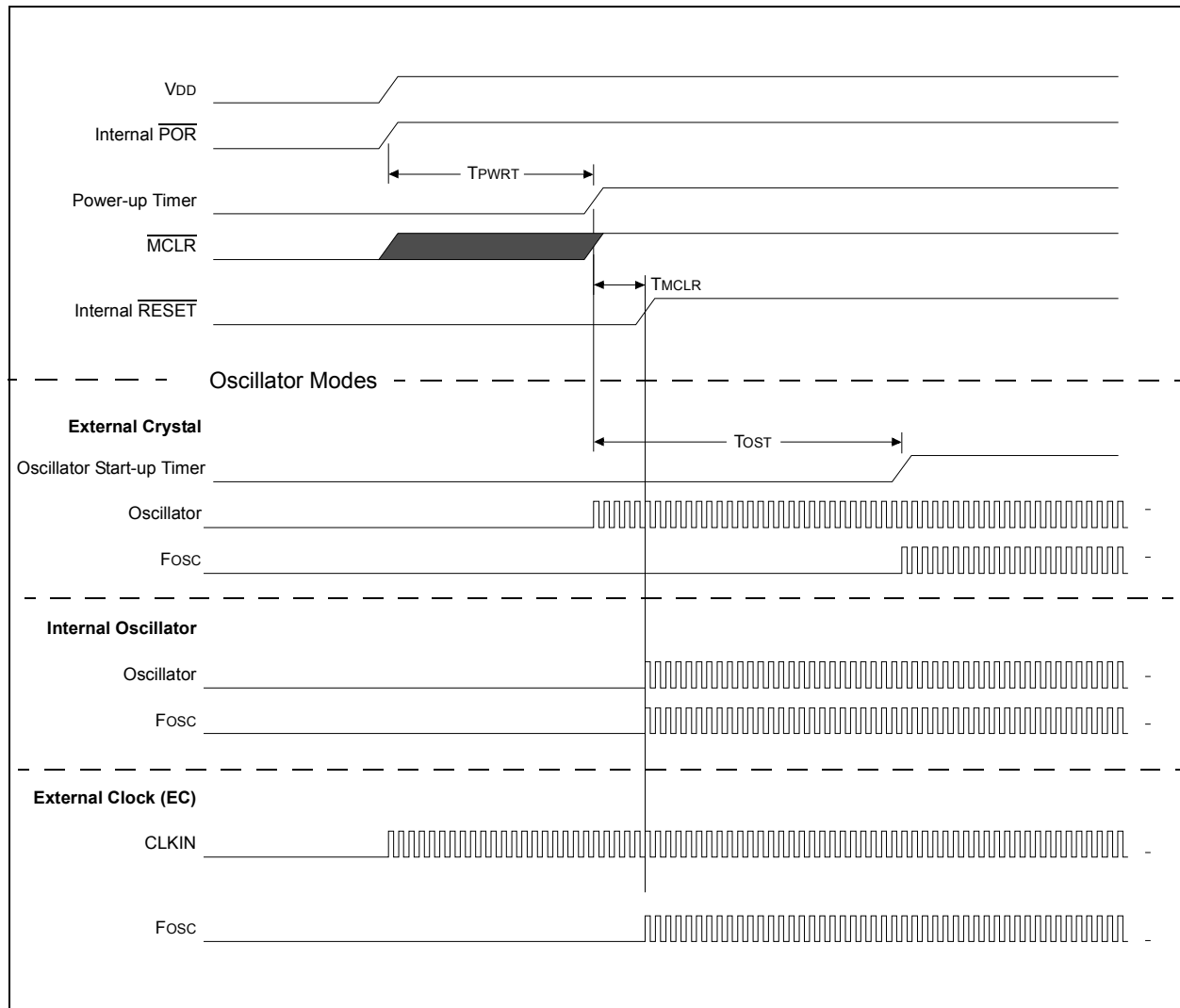
9.2   Interrupt Vector Table (IVT)

The interrupt controller supports an Interrupt Vector Table (IVT) that contains the vector address location for each interrupt request source.

The Interrupt Vector Table (IVT) resides in program memory, starting at address location determined by the IVTBASE registers; refer to Registers 9-33 through 9-35 for details. The IVT contains 68 vectors, one for each source of interrupt. Each interrupt vector location contains the starting address of the associated Interrupt Service Routine (ISR).

The MVECEN bit in Configuration Word 2L controls the availability of the vector table.

9.2.1   INTERRUPT VECTOR TABLE BASE ADDRESS (IVTBASE)

The start address of the vector table is user programmable through the IVTBASE registers. The user must ensure the start address is such that it can encompass the entire vector table inside the program memory.

Each vector address is a 16-bit word (or two address locations on PIC18 devices). So for n interrupt sources, there are 2n address locations necessary to hold the table starting from IVTBASE as the first location. So the staring address of IVTBASE should be chosen such that the address range form IVTBASE to (IVTBASE +2n-1) can be encompassed inside the program flash memory.

For example, the K42 devices have the highest vector number: 81. So IVTBASE should be chosen such that (IVTBASE + 0xA1) is less than the last memory location in program flash memory.

A programmable vector table base address is useful in situations to switch between different sets of vector tables, depending on the application. It can also be used when the application program needs to update the existing vector table (vector address values).

Note:	It is required that the user assign an even address to the IVTBASE register for correct operation.

9.2.2   INTERRUPT VECTOR TABLE CONTENTS

MVECEN = 0

When MVECEN = 0, the address location pointed by the IVTBASE registers has a GOTO instruction for a high priority interrupt. Similarly, the corresponding low priority vector location also has a GOTO instruction, which is executed in case of a low priority interrupt.

MVECEN = 1

When MVECEN = 1, the value in the vector table of each interrupt, points to the address location of the first instruction of the interrupt service routine.

ISR Location = Interrupt Vector Table entry << 2.

9.2.3   INTERRUPT VECTOR TABLE (IVT) ADDRESS CALCULATION

MVECEN = 0

When the MVECEN bit in Configuration Word 2L (Register 5-3) is cleared, the address pointed by IVTBASE registers is used as the high priority interrupt vector address. The low priority interrupt vector address is offset eight instruction words from the address in IVTBASE registers.

For PIC18 devices the IVTBASE registers default to 00 0008h, the high priority interrupt vector address will be 00 0008h and the low priority interrupt vector address will be 00 0018h.

MVECEN = 1

Each interrupt has a unique vector number associated with it as defined in Table 9-2. This vector number is used for calculating the location of the interrupt vector for a particular interrupt source.

Interrupt Vector Address = IVTBASE + (2*Vector Number).

This calculated Interrupt Vector Address value is stored in the IVTAD<20:0> registers when an interrupt is received (Registers 9-36 through 9-38).

User-assigned software priority assigned using the IPRx registers does not affect address calculation and is only used to resolve concurrent interrupts.

If for any reason the address of the ISR could not be fetched from the vector table, it will cause the system to reset and clear the memory execution violation flag (MEMV bit) in PCON1 register (Register 6-3). This occurs due to any one of the following:

- The entry for the interrupt in the vector table lies outside the executable PFM area (SAF area is non-executable when SAFEN = 1).
- ISR pointed by the vector table lies outside the executable PFM area (SAF area is non-executable when SAFEN = 1).

11.0 WINDOWED WATCHDOG TIMER (WWDT)

The Watchdog Timer (WDT) is a system timer that generates a Reset if the firmware does not issue a `CLRWDT` instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events. The Windowed Watchdog Timer (WWDT) differs in that `CLRWDT` instructions are only accepted when they are performed within a specific window during the time-out period.

The WWDT has the following features:

- Selectable clock source
- Multiple operating modes
  - WWDT is always On
  - WWDT is off when in Sleep
  - WWDT is controlled by software
  - WWDT is always Off
- Configurable time-out period is from 1 ms to 256s (nominal)
- Configurable window size from 12.5% to 100% of the time-out period
- Multiple Reset conditions

REGISTER 15-1:   DMAxCON0: DMAx CONTROL REGISTER 0

R/W-0/0	R/W/HC-0/0	R/W/HS/HC-0/0	U-0	U-0	R/W/HC-0/0	U-0	R/HS/HC-0/0
EN	SIRQEN	DGO	—	—	AIRQEN	—	XIP
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n/n = Value at POR and BOR/Value at all other Resets		0 = bit is cleared x = bit is unknown
		u = bit is unchanged

bit 7   **EN:** DMA Module Enable bit
1 =   Enables module
0 =   Disables module

bit 6   **SIRQEN:** Start of Transfer Interrupt Request Enable bits
1 =   Hardware triggers are allowed to start DMA transfers
0 =   Hardware triggers are not allowed to start DMA transfers

bit 5   **DGO:** DMA transaction bit
1 =   DMA transaction is in progress
0 =   DMA transaction is not in progress

bit 4-3   **Unimplemented:** Read as '0'

bit 2   **AIRQEN:** Abort of Transfer Interrupt Request Enable bits
1 =   Hardware triggers are allowed to abort DMA transfers
0 =   Hardware triggers are not allowed to abort DMA transfers

bit 1   **Unimplemented:** Read as '0'

bit 0   **XIP:** Transfer in Progress Status bit
1 =   The DMAxBUF register currently holds contents from a read operation and has not transferred data to the destination.
0 =   The DMAxBUF register is empty or has successfully transferred data to the destination address

16.5 Register Definitions: Port Control

REGISTER 16-1: PORTx: PORTx REGISTER[1]

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1	Rx0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets		

bit 7-0 **Rx<7:0>:** Rx7:Rx0 Port I/O Value bits

1 = Port pin is $\geq$ V$_{IH}$

0 = Port pin is $\leq$ V$_{IL}$

Note 1: Writes to PORTx are actually written to the corresponding LATx register.
Reads from PORTx register return actual I/O pin values.

TABLE 16-2: PORT REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
PORTB	RB7[1]	RB6[1]	RB5	RB4	RB3	RB2	RB1	RB0
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
PORTE	—	—	—	—	RE3[2]	—	—	—

Note 1: Bits RB6 and RB7 read '1' while in Debug mode.

2: Bit PORTE3 is read-only, and will read '1' when MCLRE = 1 (Master Clear enabled).

TABLE 17-1: PPS INPUT REGISTER DETAILS

Peripheral	PPS Input Register	Default Pin Selection at POR	Register Reset Value at POR	Input Available from Selected PORTx		
				PIC18(L)F2xK83		
Interrupt 0	INT0PPS	RB0	0b0 1000	A	B	—
Interrupt 1	INT1PPS	RB1	0b0 1001	A	B	—
Interrupt 2	INT2PPS	RB2	0b0 1010	A	B	—
Timer0 Clock	T0CKIPPS	RA4	0b0 0100	A	B	—
Timer1 Clock	T1CKIPPS	RC0	0b1 0000	A	—	C
Timer1 Gate	T1GPPS	RB5	0b0 1101	—	B	C
Timer3 Clock	T3CKIPPS	RC0	0b1 0000	—	B	C
Timer3 Gate	T3GPPS	RC0	0b1 0000	A	—	C
Timer5 Clock	T5CKIPPS	RC2	0b1 0010	A	—	C
Timer5 Gate	T5GPPS	RB4	0b0 1100	—	B	C
Timer2 Clock	T2INPPS	RC3	0b1 0011	A	—	C
Timer4 Clock	T4INPPS	RC5	0b1 0101	—	B	C
Timer6 Clock	T6INPPS	RB7	0b0 1111	—	B	C
CCP1	CCP1PPS	RC2	0b1 0010	—	B	C
CCP2	CCP2PPS	RC1	0b1 0001	—	B	C
CCP3	CCP3PPS	RB5	0b0 1101	—	B	C
CCP4	CCP4PPS	RB0	0b0 1000	—	B	C
SMT1 Window	SMT1WINPPS	RC0	0b1 0000	—	B	C
SMT1 Signal	SMT1SIGPPS	RB4	0b0 1100	—	B	C
SMT2 Window	SMT2WINPPS	RB5	0b0 1101	—	B	C
SMT2 Signal	SMT2SIGPPS	RC1	0b1 0001	—	B	C
CWG1	CWG1PPS	RB0	0b0 1000	—	B	C
CWG2	CWG2PPS	RB1	0b0 1001	—	B	C
CWG3	CWG3PPS	RB2	0b0 1010	—	B	C
DSM1 Carrier Low	MD1CARLPPS	RA3	0b0 0011	A	—	C
DSM1 Carrier High	MD1CARHPPS	RA4	0b0 0100	A	—	C
DSM1 Source	MD1SRCPPS	RA5	0b0 0101	A	—	C
CLCx Input 1	CLCIN0PPS	RA0	0b0 0000	A	—	C
CLCx Input 2	CLCIN1PPS	RA1	0b0 0001	A	—	C
CLCx Input 3	CLCIN2PPS	RB6	0b0 1110	—	B	C
CLCx Input 4	CLCIN3PPS	RB7	0b0 1111	—	B	C
ADC Conversion Trigger	ADACTPPS	RB4	0b0 1100	—	B	C
SPI1 Clock	SPI1SCKPPS	RC3	0b1 0011	—	B	C
SPI1 Data	SPI1SDIPPS	RC4	0b1 0100	—	B	C
SPI1 Slave Select	SPI1SSPPS	RA5	0b0 0101	A	—	C
I^{2}C1 Clock	I2C1SCLPPS	RC3	0b1 0011	—	B	C
I^{2}C1 Data	I2C1SDAPPS	RC4	0b1 0100	—	B	C
I^{2}C2 Clock	I2C2SCLPPS	RB1	0b0 1001	—	B	C
I^{2}C2 Data	I2C2SDAPPS	RB2	0b0 1010	—	B	C
UART1 Receive	U1RXPPS	RC7	0b1 0111	—	B	C
UART1 Clear To Send	U1CTSPPS	RC6	0b1 0110	—	B	C
UART2 Receive	U2RXPPS	RB7	0b0 1111	—	B	C
UART2 Clear To Send	U2CTSPPS	RB6	0b0 1110	—	B	C
CAN Receive	CANRXPPS	RB3	0b0 1011	—	B	C

20.1 Timer0 Operation

Timer0 can operate as either an 8-bit timer/counter or a 16-bit timer/counter. The mode is selected with the MD16 bit of the T0CON register.

20.1.1 16-BIT MODE

The register pair TMR0H:TMR0L increments on the rising edge of the clock source. A 15-bit prescaler on the clock input gives several prescale options (see prescaler control bits, CKPS<3:0> in the T0CON1 register).

20.1.1.1 Timer0 Reads and Writes in 16-Bit Mode

In 16-bit mode, in order to avoid rollover between reading high and low registers, the TMR0H register is a buffered copy of the actual high byte of Timer0, which is neither directly readable, nor writable (see Figure 20-1). TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16 bits of Timer0 without having to verify that the read of the high and low byte was valid, due to a rollover between successive reads of the high and low byte.

Similarly, a write to the high byte of Timer0 must also take place through the TMR0H Buffer register. The high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16 bits of Timer0 to be updated at once.

20.1.2 8-BIT MODE

In 8-bit mode, the value of TMR0L is compared to that of the Period buffer, a copy of TMR0H, on each clock cycle. When the two values match, the following events happen:

• TMR0_out goes high for one prescaled clock period
• TMR0L is reset
• The contents of TMR0H are copied to the period buffer

In 8-bit mode, the TMR0L and TMR0H registers are both directly readable and writable. The TMR0L register is cleared on any device Reset, while the TMR0H register initializes at FFh.

Both the prescaler and postscaler counters are cleared on the following events:

• A write to the TMR0L register
• A write to either the T0CON0 or T0CON1 registers
• Any device Reset – Power-on Reset (POR), MCLR Reset, Watchdog Timer Reset (WDTR) or
• Brown-out Reset (BOR)

20.1.3 COUNTER MODE

In Counter mode, the prescaler is normally disabled by setting the CKPS bits of the T0CON1 register to '0000'. Each rising edge of the clock input (or the output of the prescaler if the prescaler is used) increments the counter by '1'.

20.1.4 TIMER MODE

In Timer mode, the Timer0 module will increment every instruction cycle as long as there is a valid clock signal and the CKPS bits of the T0CON1 register (Register 20-2) are set to '0000'. When a prescaler is added, the timer will increment at the rate based on the prescaler value.

20.1.5 ASYNCHRONOUS MODE

When the ASYNC bit of the T0CON1 register is set (ASYNC = '1'), the counter increments with each rising edge of the input source (or output of the prescaler, if used). Asynchronous mode allows the counter to continue operation during Sleep mode provided that the clock also continues to operate during Sleep.

20.1.6 SYNCHRONOUS MODE

When the ASYNC bit of the T0CON1 register is clear (ASYNC = '0'), the counter clock is synchronized to the system clock (F_{OSC}/4). When operating in Synchronous mode, the counter clock frequency cannot exceed F_{OSC}/4.

20.2 Clock Source Selection

The CS<2:0> bits of the T0CON1 register are used to select the clock source for Timer0. Register 20-2 displays the clock source selections.

20.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, Timer0 operates as a timer and will increment on multiples of the clock source, as determined by the Timer0 prescaler.

20.2.2 EXTERNAL CLOCK SOURCE

When an external clock source is selected, Timer0 can operate as either a timer or a counter. Timer0 will increment on multiples of the rising edge of the external clock source, as determined by the Timer0 prescaler.
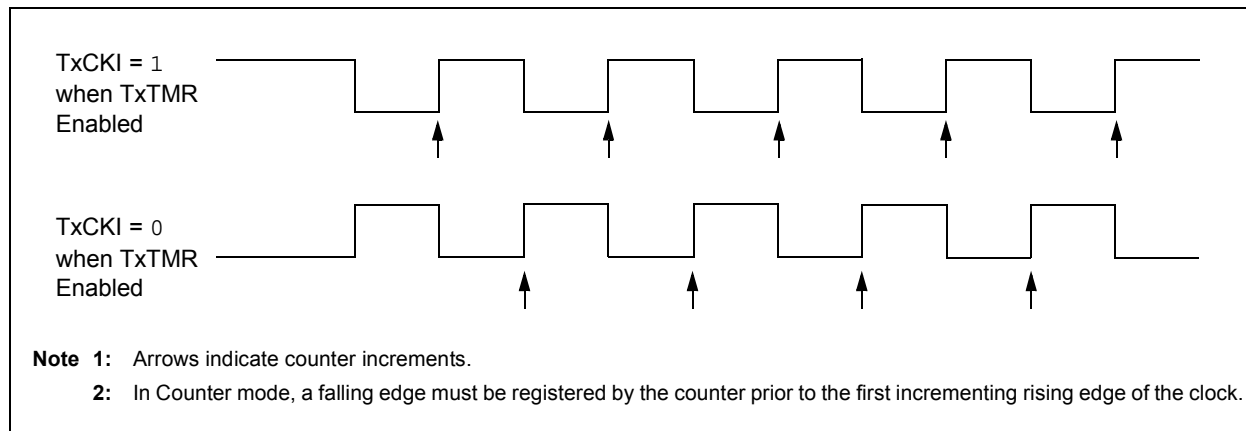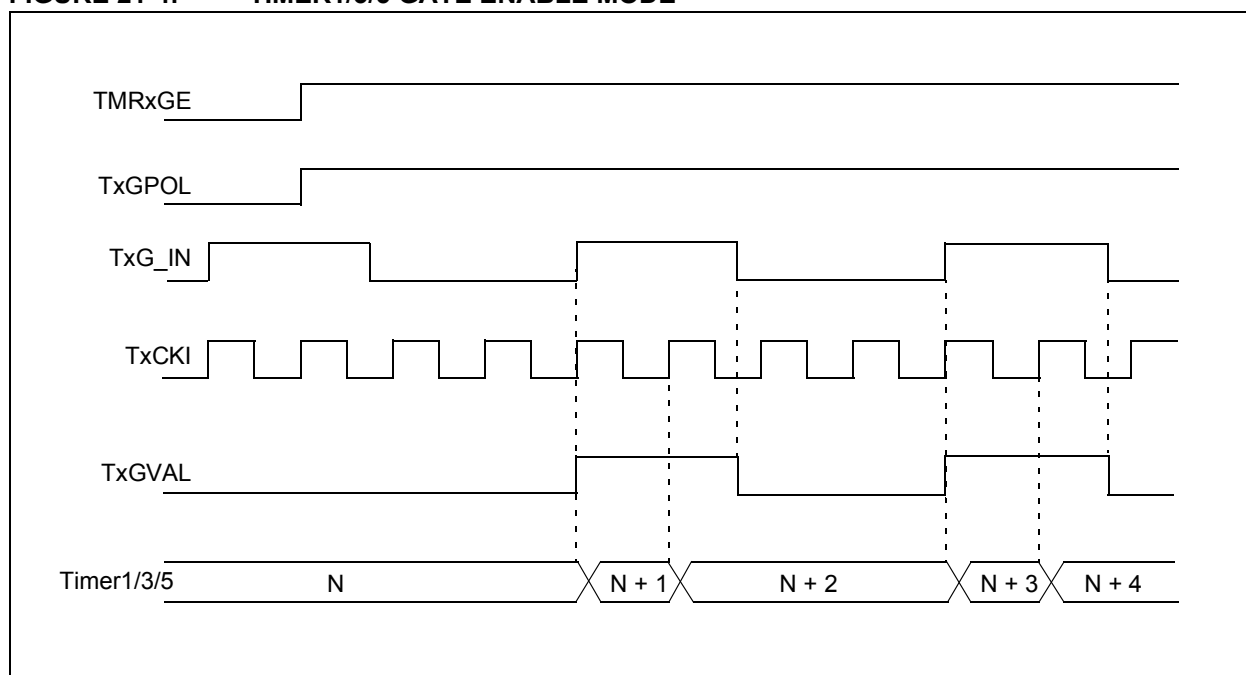
FIGURE 21-3: **TIMER1/3/5 INCREMENTING EDGE**

TxCKI = 1
when TxTMR
Enabled

TxCKI = 0
when TxTMR
Enabled

Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

FIGURE 21-4: **TIMER1/3/5 GATE ENABLE MODE**

TMRxGE

TxGPOL

TxG_IN

TxCKI

TxGVAL

Timer1/3/5   N   N + 1   N + 2   N + 3   N + 4

23.2.3   SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE Interrupt Priority bit of the respective PIE register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the respective PIR register following any change in Operating mode.

23.2.4   CAPTURE DURING SLEEP

Capture mode depends upon the Timer1 module for proper operation. There are two options for driving the Timer1 module in Capture mode. It can be driven by the instruction clock (FOSC/4), or by an external clock source.

When Timer1 is clocked by FOSC/4, Timer1 will not increment during Sleep. When the device wakes from Sleep, Timer1 will continue from its previous state.

Capture mode will operate during Sleep as long as the clock source for Timer1 is active in Sleep.

23.3   Compare Mode

Compare mode makes use of the 16-bit Timer1 resource. The 16-bit value of the CCPRxH:CCPRxL register pair is constantly compared against the 16-bit value of the TMRxH:TMRxL register pair. When a match occurs, one of the following events can occur:

• Toggle the CCPx output, clear TMRx
• Toggle the CCPx output
• Set the CCPx output
• Clear the CCPx output
• Pulse output
• Pulse output, clear TMRx

The action on the pin is based on the value of the MODE<3:0> control bits of the CCPxCON register. At the same time, the interrupt flag CCPxIF bit is set, and an ADC conversion can be triggered, if selected.

All Compare modes can generate an interrupt and trigger an ADC conversion. When MODE = 0b0001 or 0b1011, the CCP resets the TMR register pair.
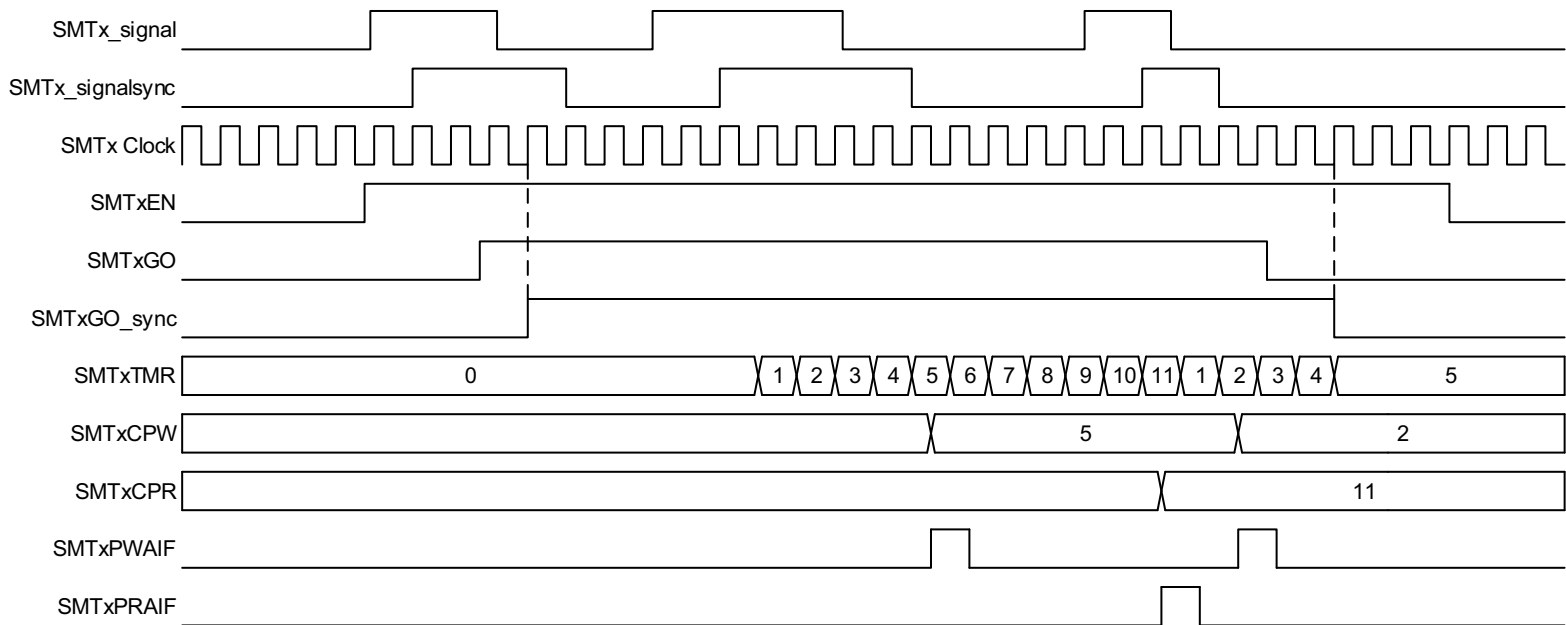
Figure 23-2 shows a simplified diagram of the compare operation.

FIGURE 23-2:   COMPARE MODE OPERATION BLOCK DIAGRAM
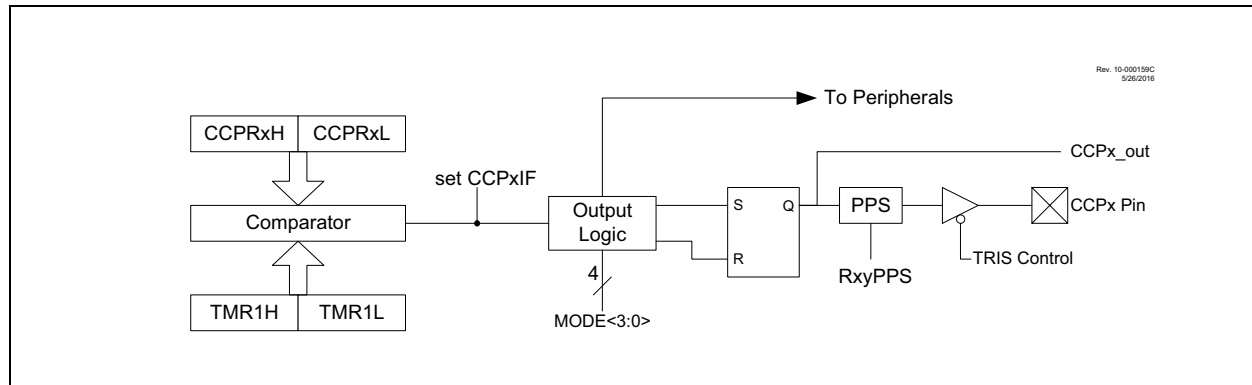
FIGURE 25-6: **PERIOD AND DUTY-CYCLE REPEAT ACQUISITION MODE TIMING DIAGRAM**

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response. As with all transmit buffers, once the TXREQ bit is set, buffer registers become read-only and any writes to them will be ignored.

34.15.5 CAN MODULE I/O CONTROL REGISTER

This register controls the operation of the CAN module's I/O pins in relation to the rest of the microcontroller.

REGISTER 34-55: CIOCON: CAN I/O CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
TX1SRC	—	—	—	—	—	—	CLKSEL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TX1SRC:** CAN_tx1 Signal Data Source bit

1 = CAN_tx1 signal will output the CAN clock
0 = CAN_tx1 signal will output CANTX

bit 6-1 **Unimplemented:** Read as '0'

bit 0 **CLKSEL:** CAN Clock Source Selection bit

1 = CAN clock is sourced by the clock selected by the FEXTOSC Configuration bit field, regardless of system clock[1]
0 = CAN clock is sourced from the system clock

Note 1: When CLKSEL = 1, the clock supplied by FEXTOSC must be less than or equal to the system clock. If the CAN clock is greater than the system clock, unexpected behavior will occur.

REGISTER 37-18: ADRESH: ADC RESULT REGISTER HIGH, FM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
			ADRES<11:4>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0   **ADRES<11:4>**: ADC Result Register bits
Upper eight bits of 12-bit conversion result.

REGISTER 37-19: ADRESL: ADC RESULT REGISTER LOW, FM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0
	ADRES<3:0>			—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4   **ADRES<3:0>**: ADC Result Register bits. Lower four bits of 12-bit conversion result.
bit 3-0   **Reserved**

39.0 COMPARATOR MODULE

> **Note:** The PIC18(L)F25/26K83 devices have two comparators. Therefore, all information in this section refers to both C1 and C2.

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution.
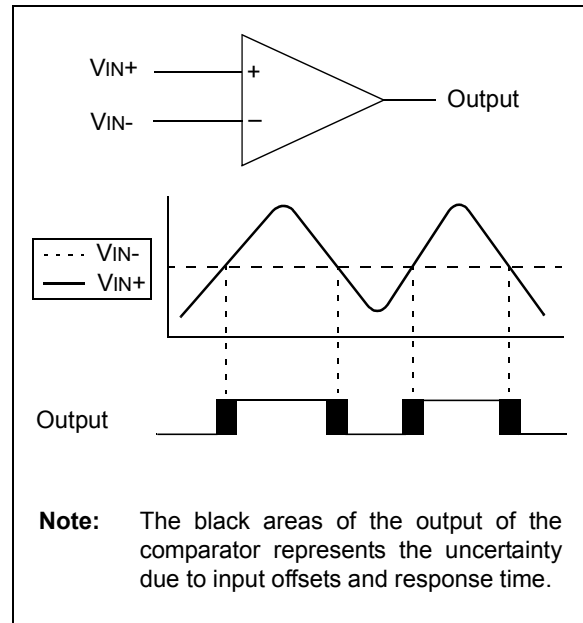
The analog comparator module includes the following features:

• Programmable input selection
• Programmable output polarity
• Rising/falling output edge interrupts

39.1 Comparator Overview

A single comparator is shown in Figure 39-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at $V_{IN}+$ is less than the analog voltage at $V_{IN}-$, the output of the comparator is a digital low level. When the analog voltage at $V_{IN}+$ is greater than the analog voltage at $V_{IN}-$, the output of the comparator is a digital high level.

FIGURE 39-1: SINGLE COMPARATOR

> **Note:** The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

BTG	Bit Toggle f

Syntax:	BTG f, b {,a}
Operands:	$0 \leq f \leq 255$ $0 \leq b < 7$ $a \in [0,1]$
Operation:	$(\overline{f<b>}) \rightarrow f<b>$
Status Affected:	None
Encoding:		0111	bbba	ffff	ffff	
Description:	Bit 'b' in data memory location 'f' is inverted. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See **Section 42.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f'

Example: BTG   PORTC, 4, 0

Before Instruction:
    PORTC = 0111 0101 [75h]
After Instruction:
    PORTC = 0110 0101 [65h]

BOV	Branch if Overflow

Syntax:	BOV n
Operands:	$-128 \leq n \leq 127$
Operation:	if OVERFLOW bit is '1' $(PC) + 2 + 2n \rightarrow PC$
Status Affected:	None
Encoding:		1110	0100	nnnn	nnnn	
Description:	If the OVERFLOW bit is '1', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.
Words:	1
Cycles:	1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE   BOV Jump

Before Instruction
    PC   =   address (HERE)
After Instruction
    If OVERFLOW =   1;
        PC   =   address (Jump)
    If OVERFLOW =   0;
        PC   =   address (HERE + 2)

TABLE 45-15: COMPARATOR SPECIFICATIONS

		Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C						
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**	
CM01	V_{IOFF}	Input Offset Voltage	—	—	±40	mV	V_{ICM} = V_{DD}/2	
CM02	V_{ICM}	Input Common Mode Range	GND	—	V_{DD}	V		
CM03	CMRR	Common Mode Input Rejection Ratio	—	50	—	dB		
CM04	V_{HYST}	Comparator Hysteresis	10	25	40	mV		
CM05	T_{RESP}[1]	Response Time, Rising Edge	—	300	600	ns		
		Response Time, Falling Edge	—	220	500	ns		

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at V_{DD}/2, while the other input transitions from V_{SS} to V_{DD}.

2: A mode change includes changing any of the control register values, including module enable.

TABLE 45-16: 5-BIT DAC SPECIFICATIONS

		Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C					
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
DSB01	V_{LSB}	Step Size	—	($V_{DACREF+}$ – $V_{DACREF-}$) / 32	—	V	
DSB01	V_{ACC}	Absolute Accuracy	—	—	± 0.5	LSb	
DSB03*	R_{UNIT}	Unit Resistor Value	—	5000	—	Ω	
DSB04*	T_{ST}	Settling Time[1]	—	—	10	μs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Settling time measured while DACR<4:0> transitions from '00000' to '01111'.

TABLE 45-17: FIXED VOLTAGE REFERENCE (FVR) SPECIFICATIONS

		Standard Operating Conditions (unless otherwise stated)					
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
FVR01	V_{FVR1}	1x Gain (1.024V)	-4	—	+4	%	$V_{DD} \geq$ 2.5V, -40°C to 85°C
FVR02	V_{FVR2}	2x Gain (2.048V)	-4	—	+4	%	$V_{DD} \geq$ 2.5V, -40°C to 85°C
FVR03	V_{FVR4}	4x Gain (4.096V)	-5	—	+5	%	$V_{DD} \geq$ 4.75V, -40°C to 85°C
FVR04	T_{FVRST}	FVR Start-up Time	—	25	—	us	

TABLE 45-18: ZERO CROSS DETECT (ZCD) SPECIFICATIONS

		Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C					
Param. No.	**Sym.**	**Characteristics**	**Min**	**Typ†**	**Max**	**Units**	**Comments**
ZC01	V_{PINZC}	Voltage on Zero Cross Pin	—	0.75	—	V	
ZC02	I_{ZCD_MAX}	Maximum source or sink current	—	—	600	μA	
ZC03	T_{RESPH}	Response Time, Rising Edge	—	1	—	μs	
	T_{RESPL}	Response Time, Falling Edge	—	1	—	μs	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
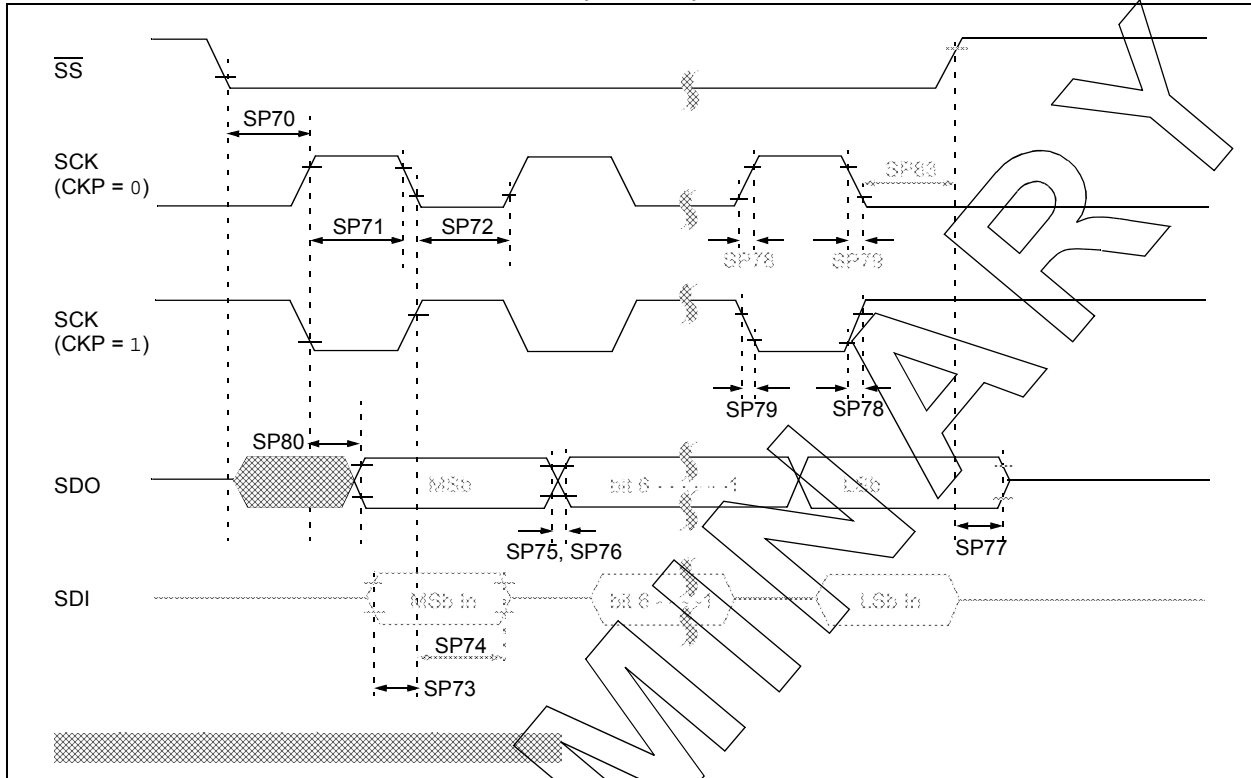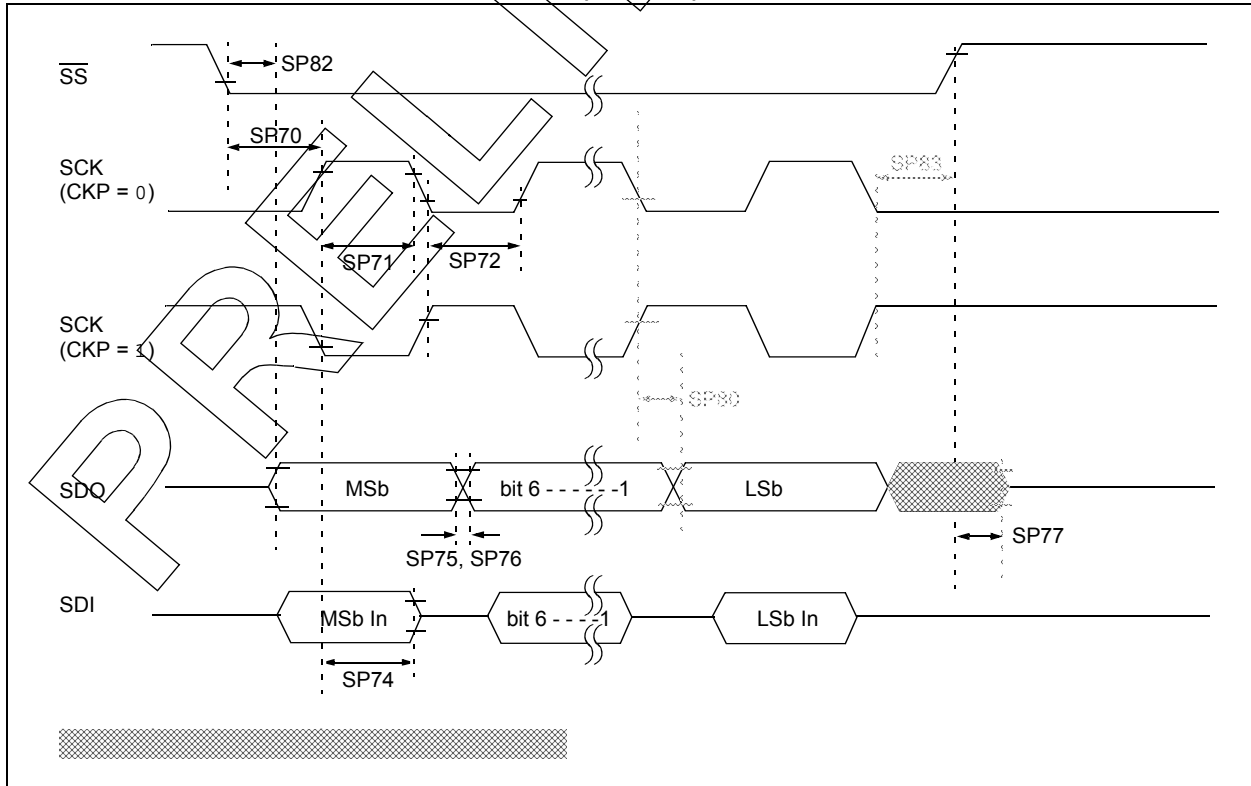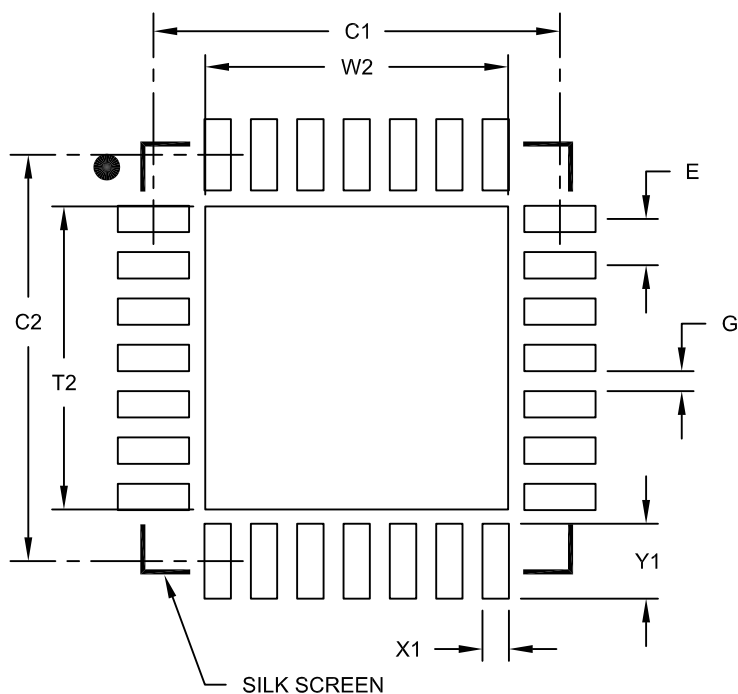
FIGURE 45-16: **SPI SLAVE MODE TIMING (CKE = 0)**

FIGURE 45-17: **SPI SLAVE MODE TIMING (CKE = 1)**

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

	Units		MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A