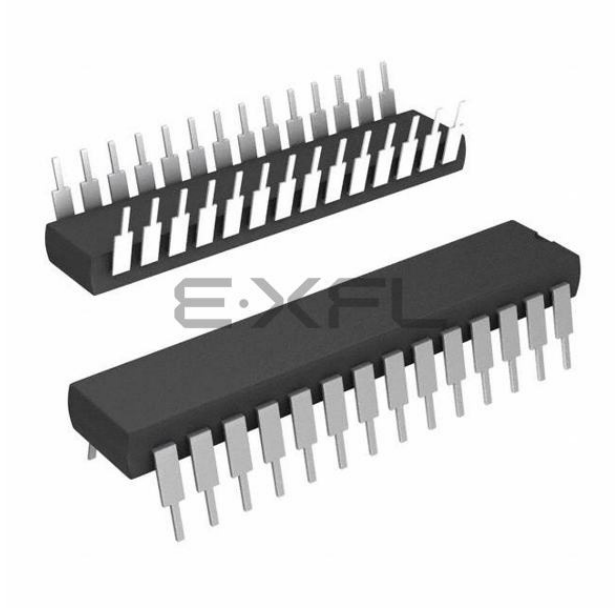

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf25k83-e-sp

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CPU

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
ISRPR	—	—	—	—	—	ISRPR2	ISRPR1	ISRPR0	20
MAINPR	—	—	—	—	—	MAINPR2	MAINPR1	MAINPR0	20
DMA1PR	—	—	—	—	—	DMA1PR2	DMA1PR1	DMA1PR0	20
DMA2PR	—	—	—	—	—	DMA2PR2	DMA2PR1	DMA2PR0	21
SCANPR	—	—	—	—	—	SCANPR2	SCANPR1	SCANPR0	21
PRLOCK	—	—	—	—	—	—	—	PRLOCKED	21

Legend: — = Unimplemented location, read as '0'.

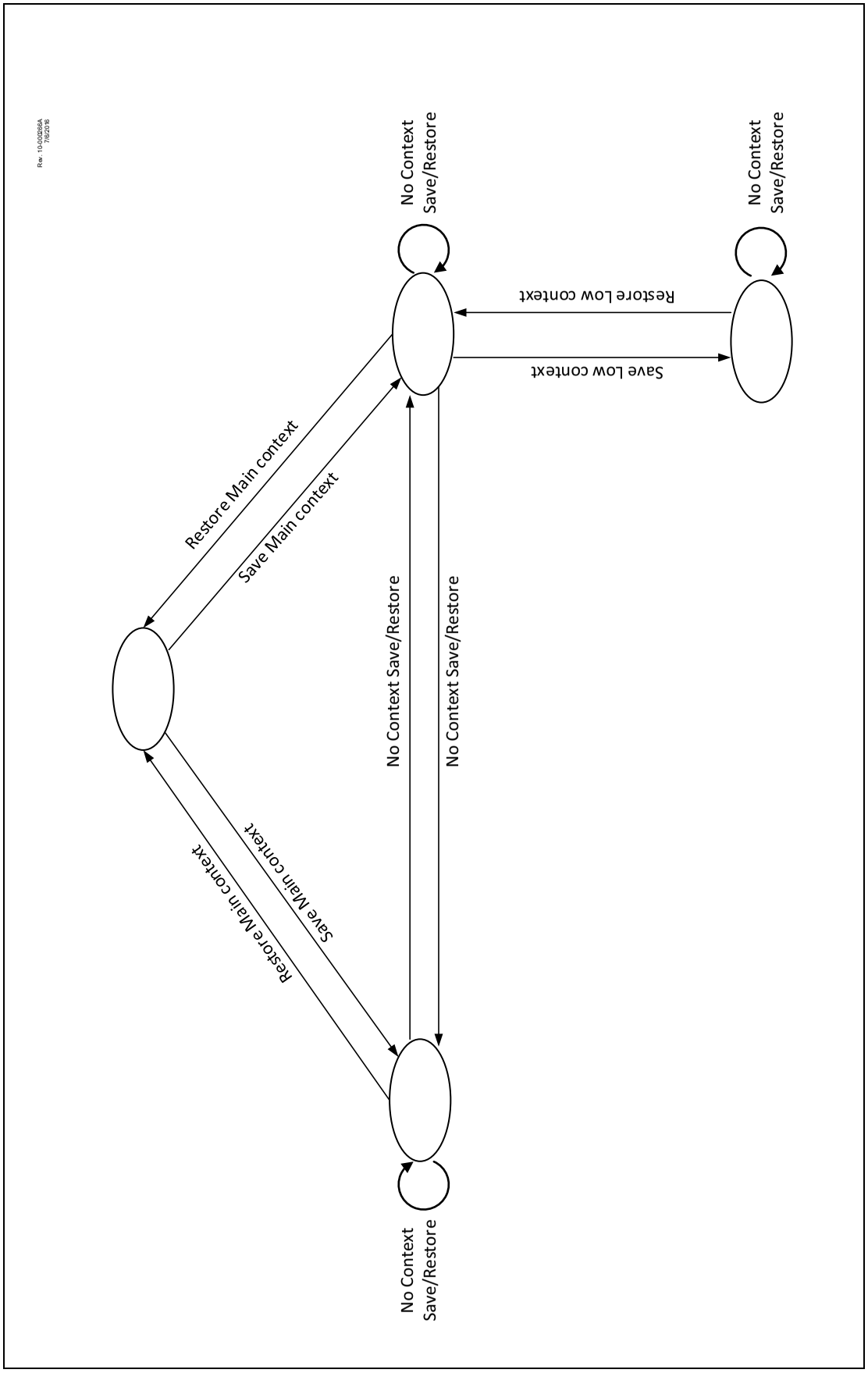
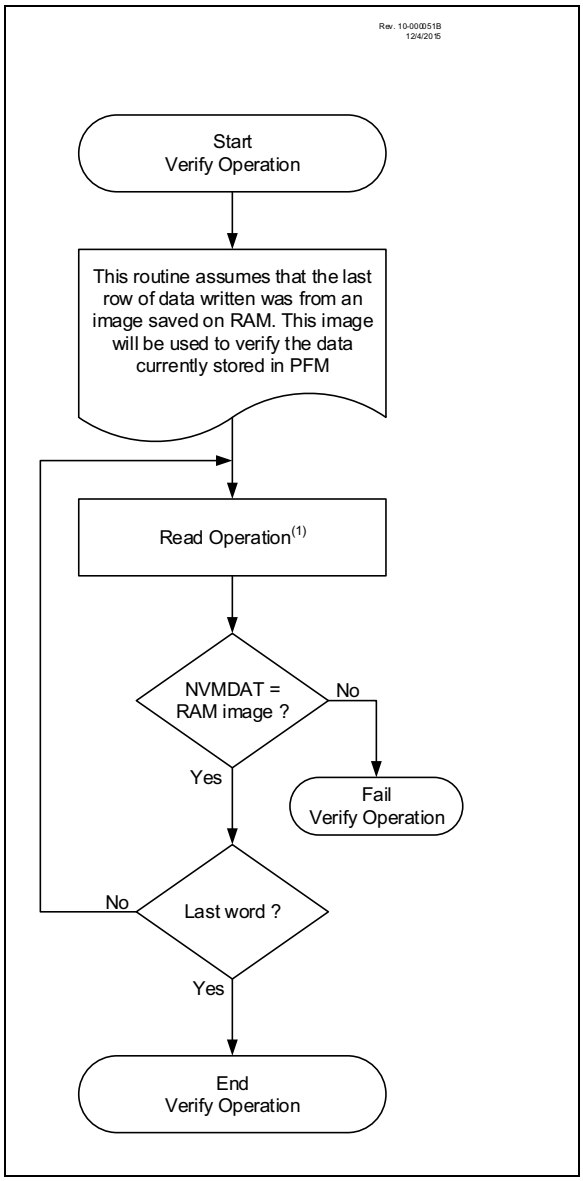


FIGURE 9-6: CONTEXT SAVE STATE MACHINE DIAGRAM

13.1.6.2 Write Verify

Depending on the application, good programming practice may dictate that the value written to the memory should be verified against the original value. This should be used in applications where excessive writes can stress bits near the specification limit. Since program memory is stored as a full page, the stored program memory contents are compared with the intended data stored in RAM after the last write is complete.

FIGURE 13-10: PROGRAM FLASH MEMORY VERIFY FLOWCHART



13.1.6.3 Unexpected Termination of Write Operation

If a write is terminated by an unplanned event, such as loss of power or an unexpected Reset, the memory location just programmed should be verified and reprogrammed if needed. If the write operation is interrupted by a $\overline{\text{MCLR}}$ Reset or a WDT Time-out Reset during normal operation, the WRERR bit will be set which the user can check to decide whether a rewrite of the location(s) is needed.

13.1.6.4 Protection Against Spurious Writes

A write sequence is valid only when both the following conditions are met, this prevents spurious writes which might lead to data corruption.

1. The WR bit is gated through the WREN bit. It is suggested to have the WREN bit cleared at all times except during memory writes. This prevents memory writes if the WR bit gets set accidentally.
2. The NVM unlock sequence must be performed each time before a write operation.

13.2 Device Information Area, Device Configuration Area, User ID, Device ID and Configuration Word Access

When REG<1:0> = 0x01 or 0x11 in the NVMCON1 register, the Device Information Area, the Device Configuration Area, the User ID's, Device ID/ Revision ID and Configuration Words can be accessed. Different access may exist for reads and writes (see Table 13-1).

13.2.1 Reading Access

The user can read from these blocks by setting the REG bits to 0x01 or 0x11. The user needs to load the address into the TBLPTR registers. Executing a TBLRD after that moves the byte pointed to the TABLAT register. The CPU operation is suspended during the read and resumes after. When read access is initiated on an address outside the parameters listed in Table 13-1, the TABLAT register is cleared, reading back '0's.

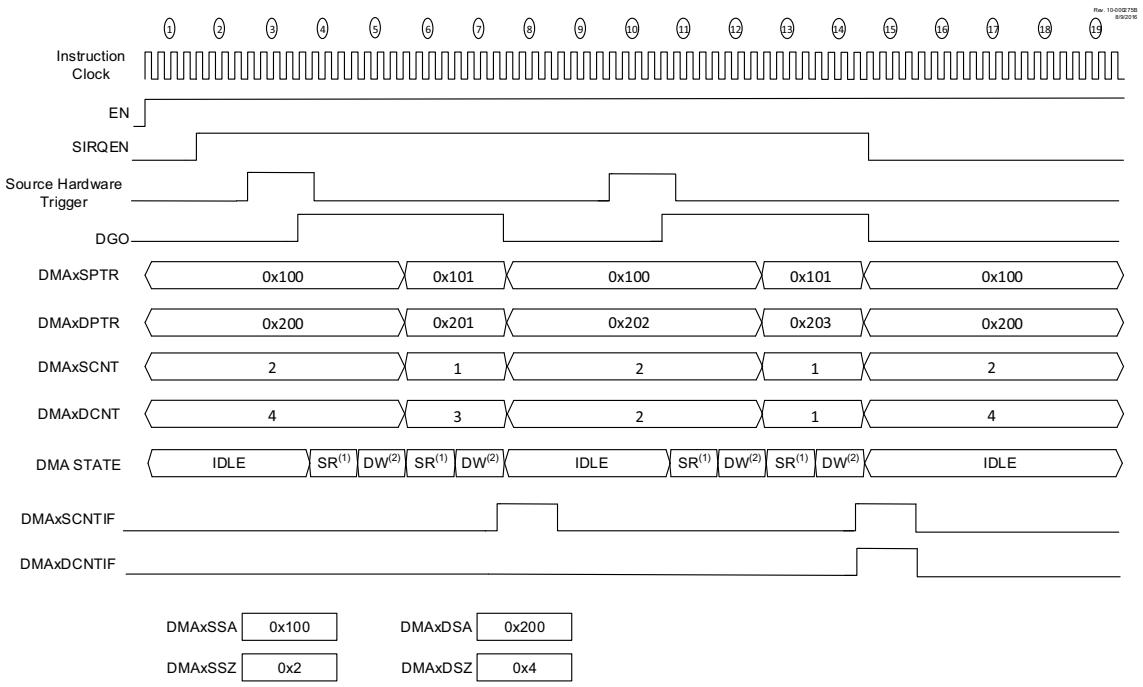
13.2.2 Writing Access

The WREN bit in NVMCON1 must be set to enable writes. This prevents accidental writes to the CONFIG words due to errant (unexpected) code execution. The WREN bit should be kept clear at all times, except when updating the CONFIG words. The WREN bit is not cleared by hardware. The WR bit will be inhibited from being set unless the WREN bit is set.

15.9.2 DESTINATION STOP

When the Destination Stop bit is set (DSTP = 1) and the DMAxDCNT register reloads, the DMA clears the SIRQEN bit to stop receiving new start interrupt request signals and sets the DMAxDCNTIF flag.

FIGURE 15-6: GPR-GPR TRANSACTIONS WITH HARDWARE TRIGGERS, DSTP = 1



Note 1: SR – Source Read

2: DW – Destination Write

REGISTER 15-1: DMAxCON0: DMAx CONTROL REGISTER 0

R/W-0/0	R/W/HC-0/0	R/W/HS/HC-0/0	U-0	U-0	R/W/HC-0/0	U-0	R/HS/HC-0/0
EN	SIRQEN	DGO	—	—	AIRQEN	—	XIP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n/n = Value at POR and BOR/Value at all other Resets		0 = bit is cleared	x = bit is unknown u = bit is unchanged

bit 7 **EN:** DMA Module Enable bit
- 1 = Enables module
- 0 = Disables module

bit 6 **SIRQEN:** Start of Transfer Interrupt Request Enable bits
- 1 = Hardware triggers are allowed to start DMA transfers
- 0 = Hardware triggers are not allowed to start DMA transfers

bit 5 **DGO:** DMA transaction bit
- 1 = DMA transaction is in progress
- 0 = DMA transaction is not in progress

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **AIRQEN:** Abort of Transfer Interrupt Request Enable bits
- 1 = Hardware triggers are allowed to abort DMA transfers
- 0 = Hardware triggers are not allowed to abort DMA transfers

bit 1 **Unimplemented:** Read as '0'

bit 0 **XIP:** Transfer in Progress Status bit
- 1 = The DMAxBUF register currently holds contents from a read operation and has not transferred data to the destination.
- 0 = The DMAxBUF register is empty or has successfully transferred data to the destination address

TABLE 17-2: PPS OUTPUT REGISTER DETAILS

RxyPPS<5:0>	Pin Rxy Output Source	Device Configuration		
		PIC18(L)F2xK83		
0b11 1111 - 0b11 0101	Reserved			
0b11 0100	CANTX1	—	B	C
0b11 0011	CANTX0	—	B	C
0b11 0010	ADGRDB	A	—	C
0b11 0001	ADGRDA	A	—	C
0b11 0000	CWG3D	A	—	C
0b10 1111	CWG3C	A	—	C
0b10 1110	CWG3B	A	—	C
0b10 1101	CWG3A	—	B	C
0b10 1100	CWG2D	—	B	C
0b10 1011	CWG2C	—	B	C
0b10 1010	CWG2B	—	B	C
0b10 1001	CWG2A	—	B	C
0b10 1000	DSM1	A	—	C
0b10 0111	CLKR	—	B	C
0b10 0110	NCO1	A	—	C
0b10 0101	TMR0	—	B	C
0b10 0100	I^2C2 (SDA)	—	B	C
0b10 0011	I^2C2 (SCL)	—	B	C
0b10 0010	I^2C1 (SDA)	—	B	C
0b10 0001	I^2C1 (SCL)	—	B	C
0b10 0000	SPI1 ($\overline{SS}$)	A	—	C
0b01 1111	SPI1 (SDO)	—	B	C
0b01 1110	SPI1 (SCK)	—	B	C
0b01 1101	C2OUT	A	—	C
0b01 1100	C1OUT	A	—	C
0b01 1011 - 0b01 1001	Reserved			
0b01 1000	UART2 ($\overline{RTS}$)	—	B	C
0b01 0111	UART2 (TXDE)	—	B	C
0b01 0110	UART2 (TX)	—	B	C
0b01 0101	UART1 ($\overline{RTS}$)	—	B	C
0b01 0100	UART1 (TXDE)	—	B	C
0b01 0011	UART1 (TX)	—	B	C
0b01 0010 - 0b01 0001	Reserved			
0b01 0000	PWM8	A	—	C
0b00 1111	PWM7	A	—	C
0b00 1110	PWM6	A	—	C
0b00 1101	PWM5	A	—	C
0b00 1100	CCP4	—	B	C
0b00 1011	CCP3	—	B	C
0b00 1010	CCP2	—	B	C
0b00 1001	CCP1	—	B	C
0b00 1000	CWG1D	—	B	C
0b00 0111	CWG1C	—	B	C
0b00 0110	CWG1B	—	B	C

TABLE 17-2: PPS OUTPUT REGISTER DETAILS

RxyPPS<5:0>	Pin Rxy Output Source	Device Configuration		
		PIC18(L)F2xK83		
0b00 0101	CWG1A	—	B	C
0b00 0100	CLC4OUT	—	B	C
0b00 0011	CLC3OUT	—	B	C
0b00 0010	CLC2OUT	A	—	C
0b00 0001	CLC1OUT	A	—	C
0b00 0000	LATxy	A	B	C

22.0 TIMER2/4/6 MODULE

The Timer2/4/6 modules are 8-bit timers that can operate as free-running period counters or in conjunction with external signals that control start, run, freeze, and reset operation in One-Shot and Monostable modes of operation. Sophisticated waveform control such as pulse density modulation are possible by combining the operation of these timers with other internal peripherals such as the comparators and CCP modules. Features of the timer include:

- 8-bit timer register
- 8-bit period register
- Selectable external hardware timer resets
- Programmable prescaler (1:1 to 1:128)
- Programmable postscaler (1:1 to 1:16)
- Selectable synchronous/asynchronous operation
- Alternate clock sources
- Interrupt on period
- Three modes of operation:
  - Free Running Period
  - One-Shot
  - Monostable

See Figure 22-1 for a block diagram of Timer2. See Figure 22-2 for the clock source block diagram.

Note:	Three identical Timer2 modules are implemented on this device. The timers are named Timer2, Timer4, and Timer6. All references to Timer2 apply as well to Timer4 and Timer6. All references to T2PR apply as well to T4PR and T6PR.

FIGURE 22-1: TIMER2 BLOCK DIAGRAM

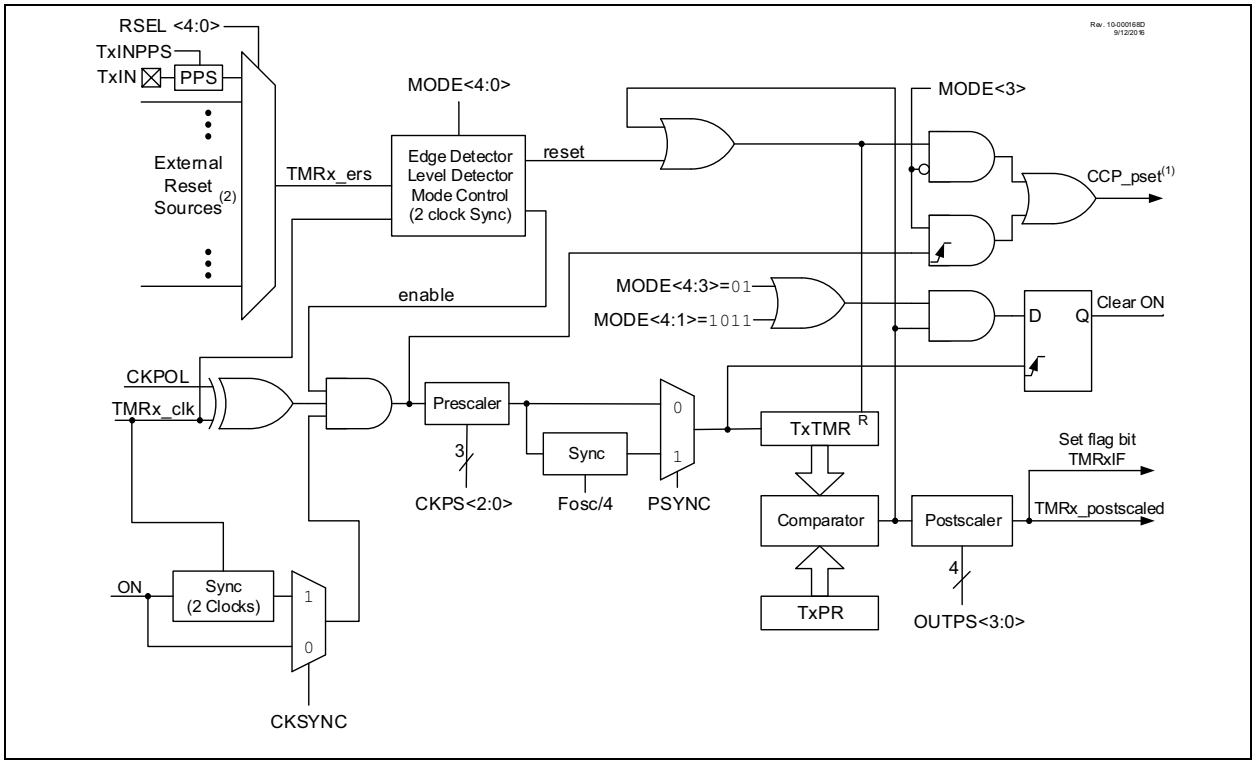
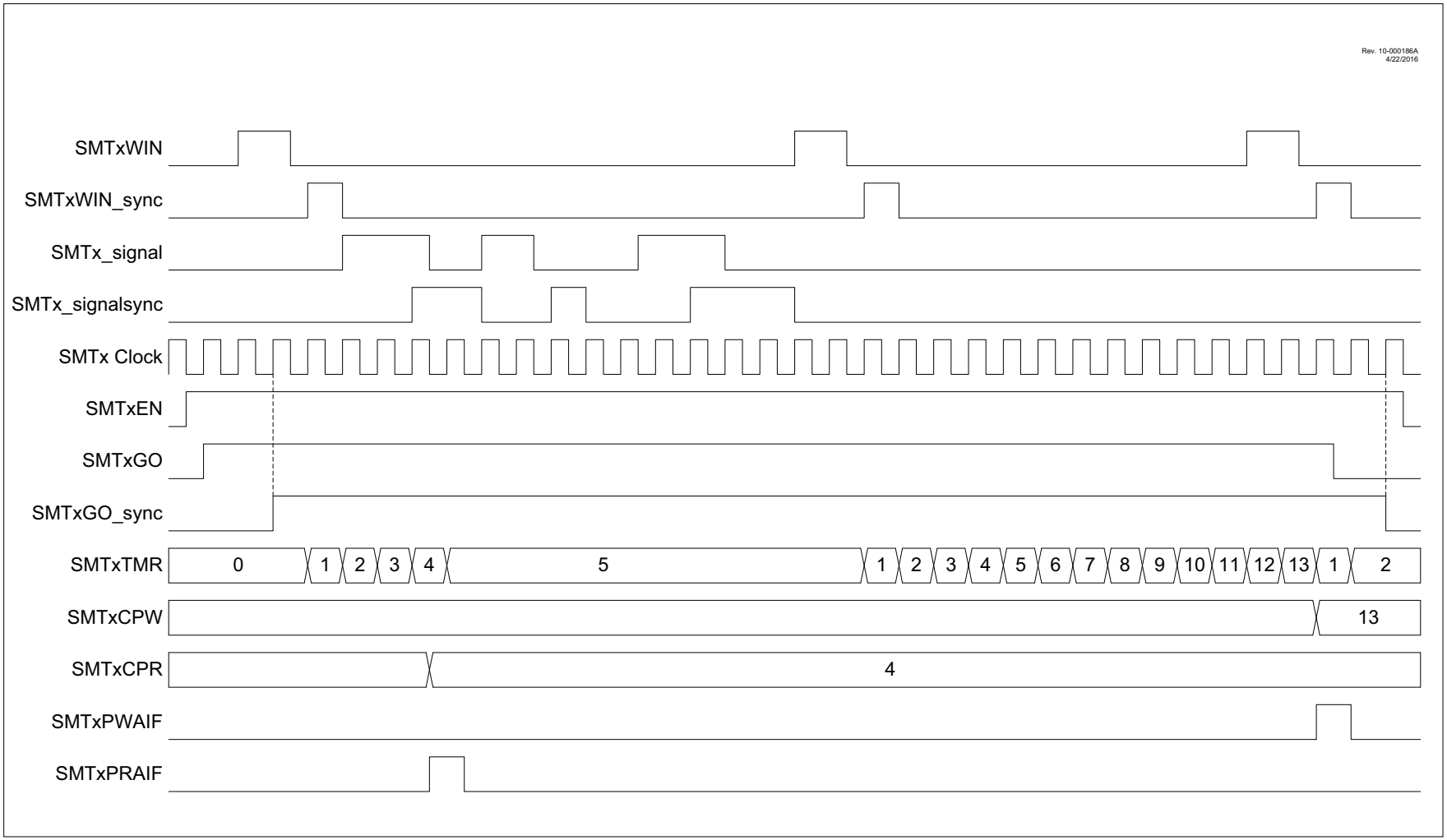


FIGURE 25-14: TIME OF FLIGHT MODE REPEAT ACQUISITION TIMING DIAGRAM



25.6.9 COUNTER MODE

This mode increments the timer on each pulse of the SMTx_signal input. This mode is asynchronous to the SMT clock and uses the SMTx_signal as a time source. The SMTxCPW register will be updated with the current SMTxTMR value on the rising edge of the SMTxWIN input. See Figure 25-18.

FIGURE 25-18: COUNTER MODE TIMING DIAGRAM

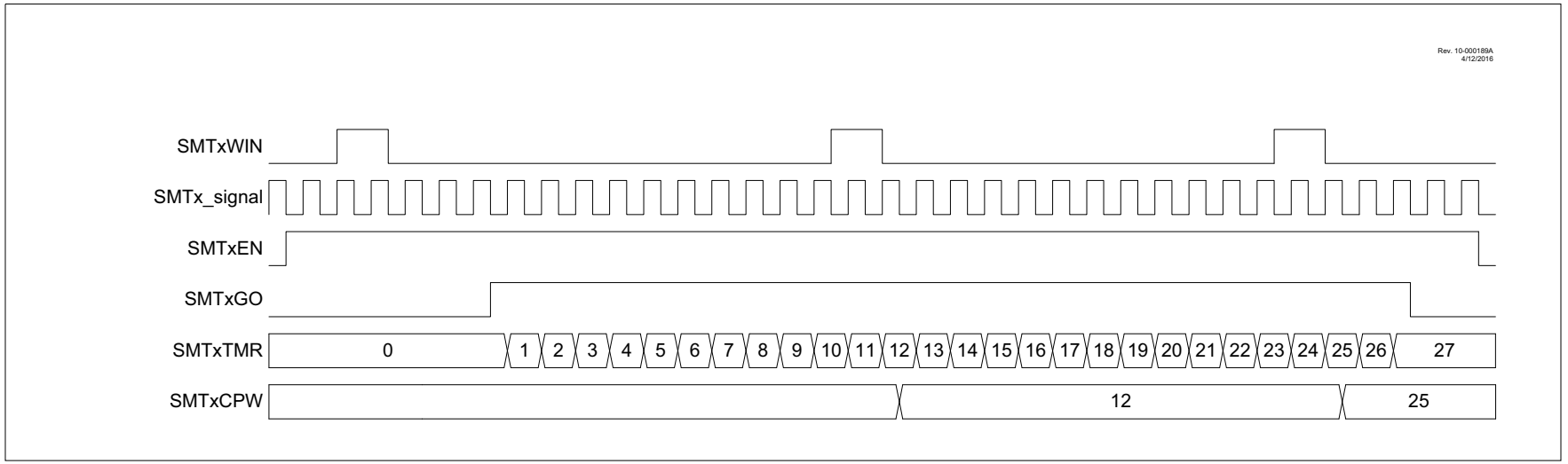
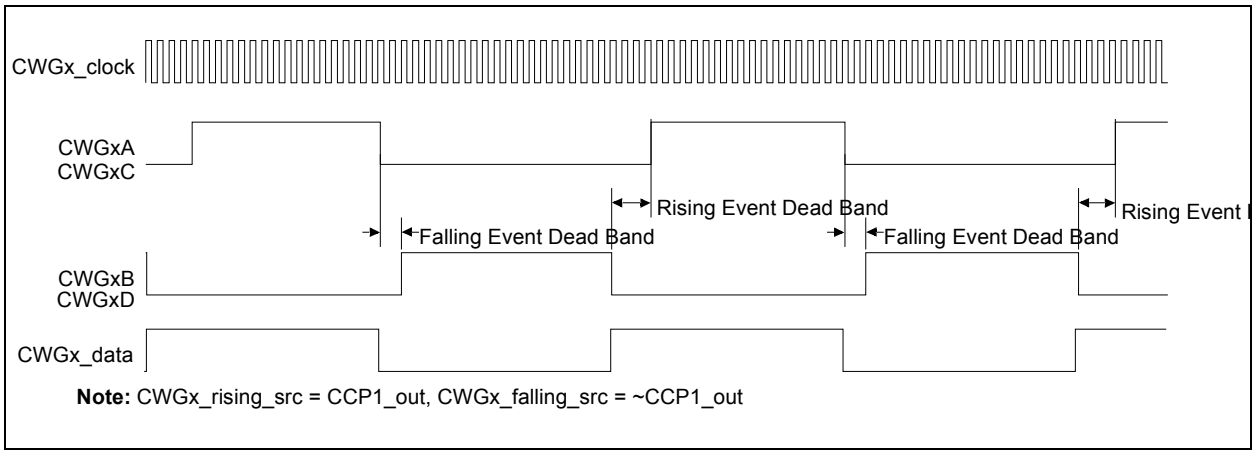


FIGURE 26-2: CWGx HALF-BRIDGE MODE OPERATION



Note: CWGx_rising_src = CCP1_out, CWGx_falling_src = ~CCP1_out

26.2.2 PUSH-PULL MODE

In Push-Pull mode, two output signals are generated, alternating copies of the input as illustrated in Figure 26-4. This alternation creates the push-pull effect required for driving some transformer-based power supply designs. Steering modes are not used in Push-Pull mode. A basic block diagram for the Push-Pull mode is shown in Figure 26-3.

The push-pull sequencer is reset whenever EN = 0 or if an auto-shutdown event occurs. The sequencer is clocked by the first input pulse, and the first output appears on CWGxA.

The unused outputs CWGxC and CWGxD drive copies of CWGxA and CWGxB, respectively, but with polarity controlled by the POLC and POLD bits of the CWGxCON1 register, respectively.

FIGURE 26-14: CWG SHUTDOWN BLOCK DIAGRAM

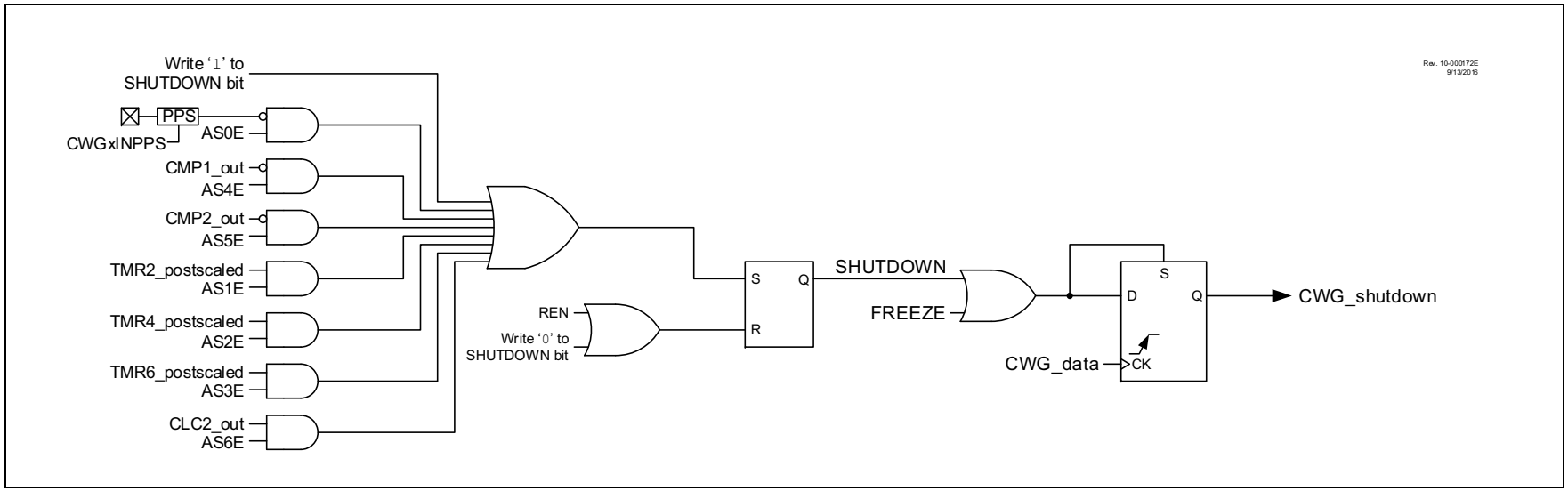
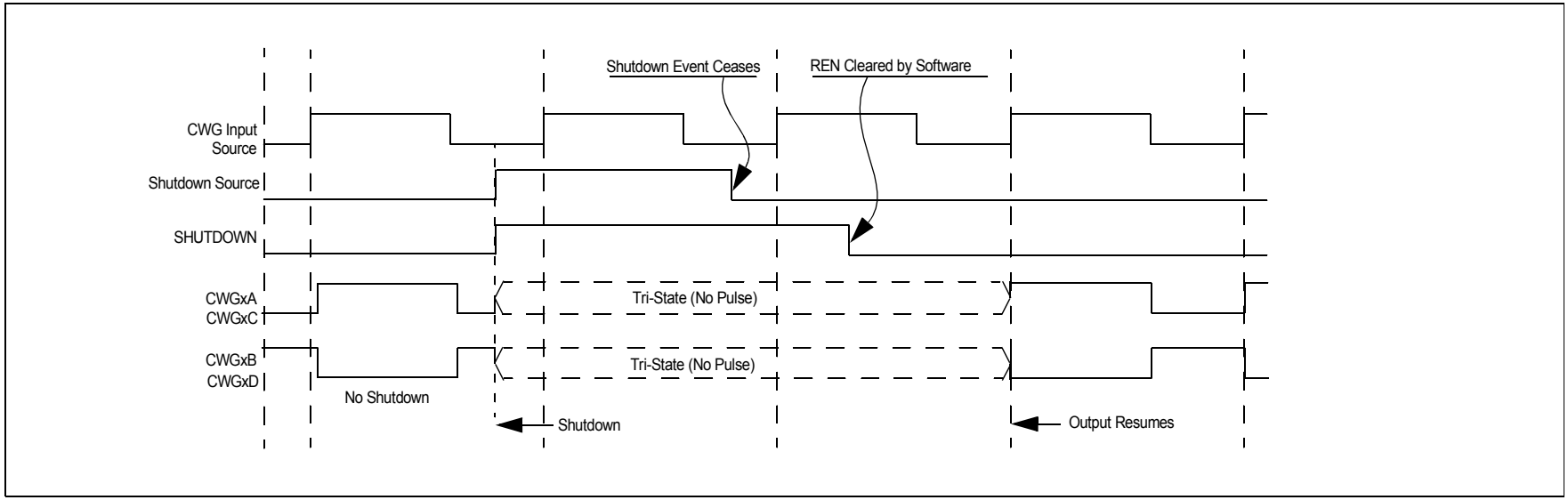


FIGURE 26-15: SHUTDOWN FUNCTIONALITY, AUTO-RESTART DISABLED (REN = 0, LSAC = 01, LSBD = 01)



REGISTER 26-4: CWGxISM: CWGx INPUT SELECTION REGISTER

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	IS<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented** Read as ‘0’

bit 4-0 **IS<4:0>:** CWG Data Input Selection Multiplexer Select bits

IS<4:0>	CWG1	CWG2	CWG3
	Input Selection	Input Selection	Input Selection
11111-10011	Reserved	Reserved	Reserved
10010	CLC4_out	CLC4_out	CLC4_out
10001	CLC3_out	CLC3_out	CLC3_out
10000	CLC2_out	CLC2_out	CLC2_out
01111	CLC1_out	CLC1_out	CLC1_out
01110	DSM_out	DSM_out	DSM_out
01101	CMP2OUT	CMP2OUT	CMP2OUT
01100	CMP1OUT	CMP1OUT	CMP1OUT
01011	NCO1OUT	NCO1OUT	NCO1OUT
01010-01001	Reserved	Reserved	Reserved
01000	PWM8OUT	PWM8OUT	PWM8OUT
00111	PWM7OUT	PWM7OUT	PWM7OUT
00110	PWM6OUT	PWM6OUT	PWM6OUT
00101	PWM5OUT	PWM5OUT	PWM5OUT
00100	CCP4_out	CCP4_out	CCP4_out
00011	CCP3_out	CCP3_out	CCP3_out
00010	CCP2_out	CCP2_out	CCP2_out
00001	CCP1_out	CCP1_out	CCP1_out
00000	Pin selected by CWG1PPS	Pin selected by CWG2PPS	Pin selected by CWG3PPS

FIGURE 30-2: On Off Keying (OOK) Synchronization

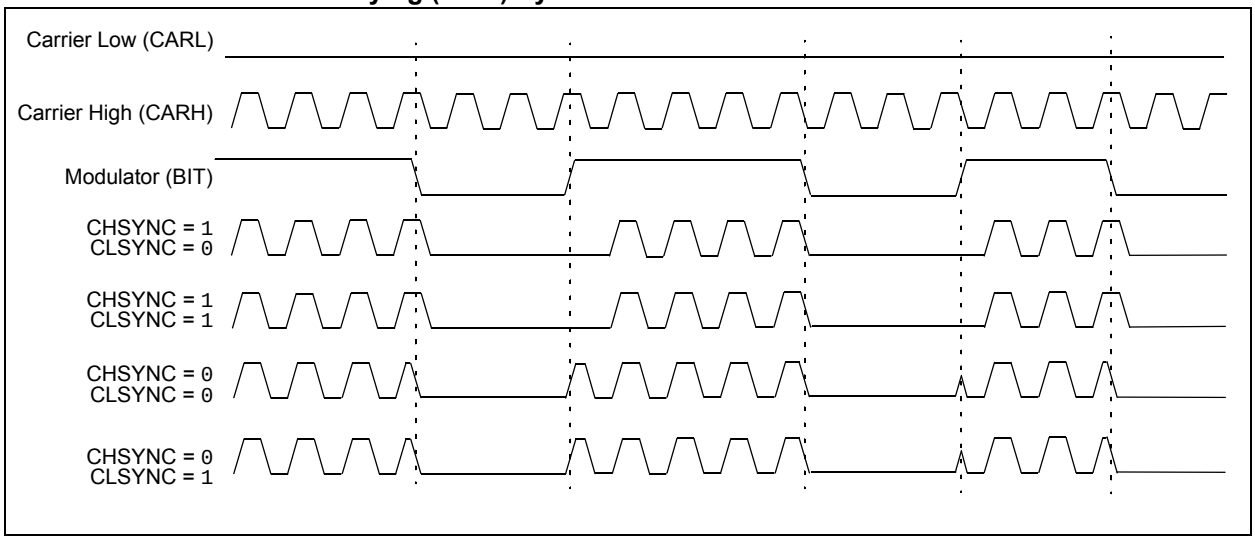


FIGURE 30-3: No Synchronization (CHSYNC = 0, CLSYNC = 0)

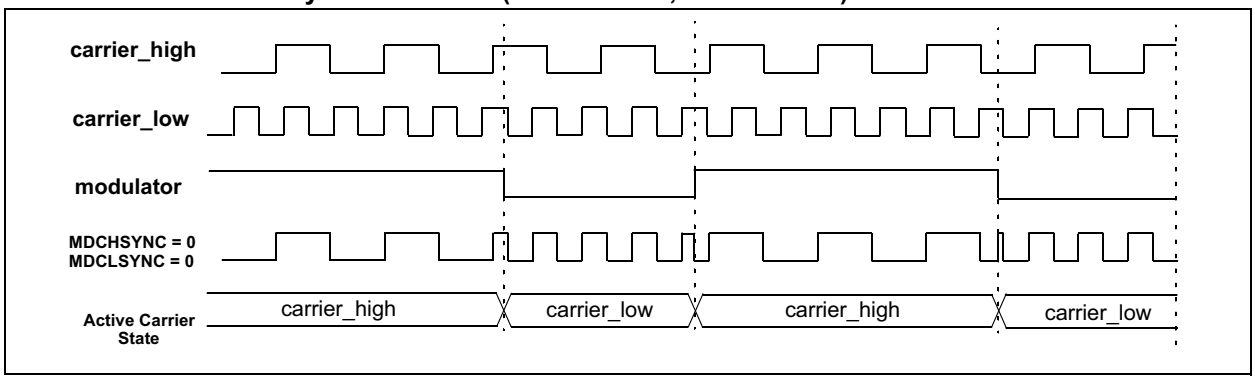
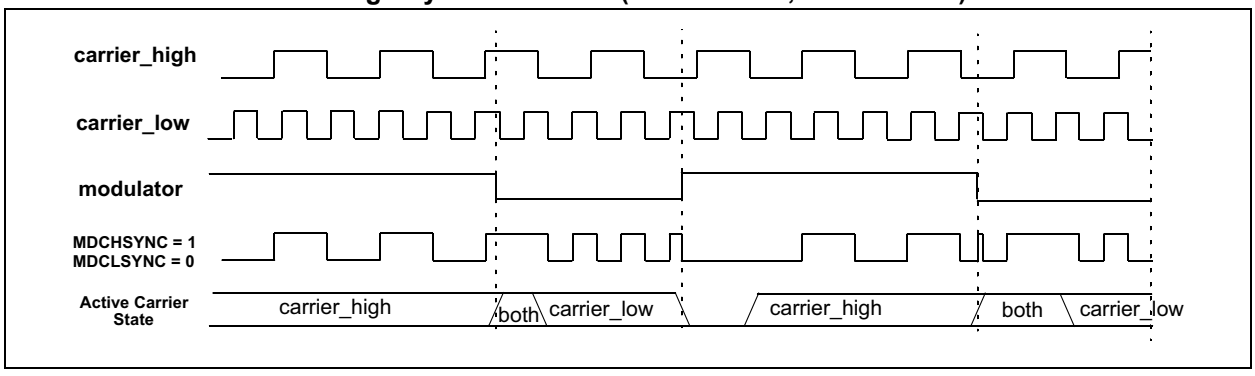


FIGURE 30-4: Carrier High Synchronization (CHSYNC = 1, CLSYNC = 0)



REGISTER 31-18: UxTXCHK: UART TRANSMIT CHECKSUM RESULT REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TXCHK<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **TXCHK<7:0>:** Checksum calculated from TX bytes
LIN mode and C0EN = 1:
Sum of all transmitted bytes including PID
LIN mode and C0EN = 0:
Sum of all transmitted bytes except PID
All other modes and C0EN = 1:
Sum of all transmitted bytes since last clear
All other modes and C0EN = 0:
Not used

REGISTER 31-19: UxRXCHK: UART RECEIVE CHECKSUM RESULT REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
RXCHK<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **RXCHK<7:0>:** Checksum calculated from RX bytes
LIN mode and C0EN = 1:
Sum of all received bytes including PID
LIN mode and C0EN = 0:
Sum of all received bytes except PID
All other modes and C0EN = 1:
Sum of all received bytes since last clear
All other modes and C0EN = 0:
Not used

34.15 CAN Module Registers

Note:	Not all CAN registers are available in the Access Bank.

There are many control and data registers associated with the CAN module. For convenience, their descriptions have been grouped into the following sections:

- Control and Status Registers
- Dedicated Transmit Buffer Registers
- Dedicated Receive Buffer Registers
- Programmable TX/RX and Auto RTR Buffers
- Baud Rate Control Registers
- I/O Control Register
- Interrupt Status and Control Registers

Detailed descriptions of each register and their usage are described in the following sections.

34.15.1 CAN CONTROL AND STATUS REGISTERS

The registers described in this section control the overall operation of the CAN module and show its operational status.

REGISTER 34-13: RXB0CON: RECEIVE BUFFER 0 CONTROL REGISTER (CONTINUED)

bit 2 Mode 0:
RB0DBEN: Receive Buffer 0 Double-Buffer Enable bit
1 = Receive Buffer 0 overflow will write to Receive Buffer 1
0 = No Receive Buffer 0 overflow to Receive Buffer 1
Mode 1, 2:
FILHIT<4:0>: Filter Hit bit 2
This bit combines with other bits to form filter acceptance bits<4:0>.

bit 1 Mode 0:
JTOFF: Jump Table Offset bit (read-only copy of RXB0DBEN)**(2)**
1 = Allows jump table offset between 6 and 7
0 = Allows jump table offset between 1 and 0
Mode 1, 2:
FILHIT<4:0>: Filter Hit bit 1
This bit combines with other bits to form filter acceptance bits<4:0>.

bit 0 Mode 0:
FILHIT0: Filter Hit bit 0
This bit indicates which acceptance filter enabled the message reception into Receive Buffer 0.
1 = Acceptance Filter 1 (RXF1)
0 = Acceptance Filter 0 (RXF0)
Mode 1, 2:
FILHIT<4:0>: Filter Hit bit 0
This bit, in combination with FILHIT<4:1>, indicates which acceptance filter enabled the message reception into this receive buffer.
01111 = Acceptance Filter 15 (RXF15)
01110 = Acceptance Filter 14 (RXF14)
...
00000 = Acceptance Filter 0 (RXF0)

Note 1: This bit is set by the CAN module upon receiving a message and must be cleared by software after the buffer is read. As long as RXFUL is set, no new message will be loaded and the buffer will be considered full. After clearing the RXFUL flag, the PIR5 bit, RXB0IF, can be cleared. If RXB0IF is cleared, but RXFUL is not cleared, then RXB0IF is set again.

2: This bit allows the same filter jump table for both RXB0CON and RXB1CON.

37.2.5 AUTO-CONVERSION TRIGGER

The auto-conversion trigger allows periodic ADC measurements without software intervention. When a rising edge of the selected source occurs, the GO bit is set by hardware.

The auto-conversion trigger source is selected by the ADACT register.

Using the auto-conversion trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met. See Register 37-33 for auto-conversion sources.

37.2.6 ADC CONVERSION PROCEDURE (BASIC MODE)

This is an example procedure for using the ADC to perform an analog-to-digital conversion:

1. Configure Port:
   - Disable pin output driver (Refer to the TRISx register)
   - Configure pin as analog (Refer to the ANSELx register)
2. Configure the ADC module:
   - Select ADC conversion clock
   - Select voltage reference
   - Select ADC input channel
   - Precharge and acquisition
   - Turn on ADC module
3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable global interrupt (GIEL bit)**(1)**
4. If ADACQ = 0, software must wait the required acquisition time**(2)**.
5. Start conversion by setting the GO bit.
6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO bit
   - Polling the ADIF bit
   - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result.
8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: Refer to **Section 37.3 "ADC Acquisition Requirements"**.

EXAMPLE 37-1: ADC CONVERSION

```
/*This code block configures the ADC
for polling, VDD and VSS references, FRC
oscillator and AN0 input.
Conversion start & polling for completion
are included.
 */
void main() {
    //System Initialize
    initializeSystem();

    //Setup ADC
    ADCON0bits.FM = 1; //right justify
    ADCON0bits.CS = 1; //FRC Clock
    ADPCH = 0x00; //RA0 is Analog channel
    TRISAbits.TRISA0 = 1; //Set RA0 to input
    ANSELAbits.ANSELA0 = 1; //Set RA0 to analog
    ADCON0bits.ON = 1; //Turn ADC On

    while (1) {
        ADCON0bits.GO = 1; //Start conversion
        while (ADCON0bits.GO); //Wait for conversion done
        resultHigh = ADRESH; //Read result
        resultLow = ADRESL; //Read result
    }
}
```

BNOV **Branch if Not Overflow**

Syntax: BNOV n

Operands: -128 ≤ n ≤ 127

Operation: if OVERFLOW bit is '0'
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0101	nnnn	nnnn

Description: If the OVERFLOW bit is '0', then the program will branch.
The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example:
```
HERE    BNOV  Jump
Before Instruction
    PC          =   address (HERE)
After Instruction
    If OVERFLOW =   0;
        PC      =   address (Jump)
    If OVERFLOW =   1;
        PC      =   address (HERE + 2)
```

BNZ **Branch if Not Zero**

Syntax: BNZ n

Operands: -128 ≤ n ≤ 127

Operation: if ZERO bit is '0'
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0001	nnnn	nnnn

Description: If the ZERO bit is '0', then the program will branch.
The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example:
```
HERE    BNZ  Jump
Before Instruction
    PC          =   address (HERE)
After Instruction
    If ZERO     =   0;
        PC      =   address (Jump)
    If ZERO     =   1;
        PC      =   address (HERE + 2)
```

INFSNZ **Increment f, skip if not 0**

Syntax: INFSNZ f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) + 1 → dest,
skip if result ≠ 0

Status Affected: None

Encoding:

0100	10da	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default).
If the result is not '0', the next instruction, which is already fetched, is discarded and a NOP is executed instead, making it a 2-cycle instruction.
If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 42.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    INFSNZ  REG, 1, 0
ZERO
NZERO
```
Before Instruction
PC = Address (HERE)
After Instruction
REG = REG + 1
If REG ≠ 0;
PC = Address (NZERO)
If REG = 0;
PC = Address (ZERO)

IORLW **Inclusive OR literal with W**

Syntax: IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. k → W

Status Affected: N, Z

Encoding:

0000	1001	kkkk	kkkk

Description: The contents of W are ORed with the 8-bit literal 'k'. The result is placed in W.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example:
```
IORLW   35h
```
Before Instruction
W = 9Ah
After Instruction
W = BFh

RETFIE **Return from Interrupt**

Syntax: RETFIE {s}

Operands: s ∈ [0,1]

Operation: (TOS) → PC,
if s = 1, context is restored into WREG, STATUS, BSR, FSR0H, FSR0L, FSR1H, FSR1L, FSR2H, FSR2L, PRODH, PRODL, PCLATH and PCLATU registers from the corresponding shadow registers.

if s = 0, there is no change in status of any register.

Status Affected: STAT<1:0> in INTCON1 register

Encoding:

0000	0000	0001	000s

Description: Return from interrupt. Stack is popped and Top-of-Stack (TOS) is loaded into the PC. Interrupts are enabled by setting either the high or low priority global interrupt enable bit. If 's' = 1, the contents of the shadow registers, WREG, STATUS, BSR, FSR0H, FSR0L, FSR1H, FSR1L, FSR2H, FSR2L, PRODH, PRODL, PCLATH and PCLATU, are loaded into corresponding registers. There are two sets of shadow registers, main context and low context. The set retrieved on RETFIE instruction execution depends on what the state of operation of the CPU was when RETFIE was executed. If 's' = 0, no update of these registers occurs (default).

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	No operation	POP PC from stack Set GIEH or GIEL
No operation	No operation	No operation	No operation

Example: RETFIE 1

After Interrupt
PC = TOS
WREG = WREG_SHAD
BSR = BSR_SHAD
STATUS = STATUS_SHAD
FSR0L/H = FSR0L/H_SHAD
FSR1L/H = FSR1L/H_SHAD
FSR2L/H = FSR2L/H_SHAD
PROD/H = PROD/H_SHAD
PCLATH/U = PCLATH/U_SHAD

RETLW **Return literal to W**

Syntax: RETLW k

Operands: 0 ≤ k ≤ 255

Operation: k → W,
(TOS) → PC,
PCLATU, PCLATH are unchanged

Status Affected: None

Encoding:

0000	1100	kkkk	kkkk

Description: W is loaded with the 8-bit literal 'k'. The Program Counter is loaded from the top of the stack (the return address). The high address latch (PCLATH) remains unchanged.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	POP PC from stack, Write to W
No operation	No operation	No operation	No operation

Example:

```
    CALL TABLE ; W contains table
               ; offset value
               ; W now has
               ; table value
    :
TABLE
    ADDWF PCL  ; W = offset
    RETLW k0   ; Begin table
    RETLW k1   ;
    :
    :
    RETLW kn   ; End of table
```

Before Instruction
W = 07h
After Instruction
W = value of kn