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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

•XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	CANbus, I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf26k83t-i-ml

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 2: PACKAGES

Device	SPDIP	SOIC	SSOP	UQFN	QFN
PIC18(L)F25K83	•	•	•	•	•
PIC18(L)F26K83	•	•	•	•	•

Note 1: Pin details are subject to change.

Pin Diagrams



U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/W-1	
_	_	_	_	_	_	—	CP	
bit 7						·	bit 0	
Legend:								
R = Readable bit W = Writable bit				U = Unimplemented bit, read as '1'				
-n = Value for b	lank device	ik device '1' = Bit is set '0' = Bit is cleared x = Bit is unknown						

REGISTER 5-9: CONFIGURATION WORD 5L (30 0008h)

bit 7-1 Unimplemented: Read as '1'

bit 0

CP: User Program Flash Memory and Data EEPROM Code Protection bit

1 = User Program Flash Memory and Data EEPROM code protection is disabled

0 = User Program Flash Memory and Data EEPROM code protection is enabled

REGISTER 5-10: CONFIGURATION WORD 5H (30 0009h)

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
_	—	_	—	_	—	_	_
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '1'
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 Unimplemented: Read as '1'

TABLE 5-2:SUMMARY OF CONFIGURATION WORDS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
30 0000h	CONFIG1L	_	I	RSTOSC<2:0>				FEXTOSC<2	:0>	1111 1111
30 0001h	CONFIG1H	_	_	FCMEN	_	CSWEN	_	PR1WAY	CLKOUTEN	1111 1111
30 0002h	CONFIG2L	BORE	N<1:0>	LPBOREN	IVT1WAY	MVECEN	PWR	TS<1:0>	MCLRE	1111 1111
30 0003h	CONFIG2H	XINST	—	DEBUG	STVREN	PPS1WAY	ZCD BORV<1:0>		1111 1111	
30 0004h	CONFIG3L	_	WDT	E<1:0>			WDTCPS<4	4:0>		1111 1111
30 0005h	CONFIG3H	_	_	v	VDTCCS<2:0	>		WDTCWS<2	:0>	1111 1111
30 0006h	CONFIG4L	WRTAPP	_	_	SAFEN	BBEN	BBSIZE<2:0>			1111 1111
30 0007h	CONFIG4H	_	_	LVP	_	WRTSAF	WRTD	WRTC	WRTB	1111 1111
30 0008h	CONFIG5L	_	_	_	_	_	—	_	CP	1111 1111
30 0009h	CONFIG5H	_	_	_	_	_	_	_	_	1111 1111

9.4.2 SERVING A HIGH PRIORITY INTERRUPT WHILE A LOW PRIORITY INTERRUPT PENDING

A high priority interrupt request will always take precedence over any interrupt of a lower priority. The high priority interrupt is acknowledged first, then the low-priority interrupt is acknowledged. Upon a return from the high priority ISR (by executing the RETFIE instruction), the low priority interrupt is serviced, see Figure 9-3.

If any other high priority interrupts are pending and enabled, then they are serviced before servicing the pending low priority interrupt. If no other high priority interrupt requests are active, the low priority interrupt is serviced.

FIGURE 9-3: INTERRUPT EXECUTION: HIGH PRIORITY INTERRUPT WITH A LOW PRIORITY INTERRUPT PENDING



FIGURE 15-2: DMA POINTERS BLOCK DIAGRAM



The DMA can initiate data transfers from the PFM, Data EEPROM or SFR/GPR Space. The SMR<1:0> bits in the DMAxCON1 register are used to select the type of memory being pointed to by the Source Address Pointer. The SMR<1.0> bits are required because the PFM and SFR/GPR spaces have overlapping addresses that do not allow the specified address to uniquely define the memory location to be accessed.

Note 1:	For proper memory read access to occur,
	the combination of address and space
	selection must be valid.
-	

2: The destination does not have space selection bits because it can only write to the SFR/GPR space.

15.4.2 DMA MESSAGE SIZE/COUNTERS

A transaction is the transfer of one byte. A message consists of one or more transactions. A complete DMA process consists of one or more messages. The size registers determine how many transactions are in a message. The DMAxSSZ registers determine the source size and DMAxDSZ registers determine the destination size.

When a DMA transfer is initiated, the size registers are copied to corresponding counter registers that control the duration of the message. The DMAxSCNT registers count the source transactions and the DMAxDCNT registers count the destination transactions. Both are simultaneously decremented by one after each transaction. A message is started by setting the DGO bit of the DMAxCON0 register and terminates when the smaller of the two counters reaches zero.

When either counter reaches zero the DGO bit is cleared and the counter and pointer registers are immediately reloaded with the corresponding size and address data. If the other counter did not reach zero then the next message will continue with the count and address corresponding to that register.

When the source and destination size registers are not equal then the ratio of the largest to the smallest size determines how many messages are in the DMA process. For example, when the destination size is 6 and the source size is 2 then each message will consist of two transactions and the complete DMA process will consist of three messages. When the larger size is not an even integer of the smaller size then the last message in the process will terminate early when the larger count reaches zero. In that case, the larger counter will reset and the smaller counter will have a remainder skewing any subsequent messages by that amount.

Note:	Reading the DMAxSCNT or DMAxDCNT registers will never return zero. When either register is decremented from '1' it is				
	immediately reloaded from the corresponding size register.				

REGISTE	ER 15-2: DI	MAxCON1: D	MAx CONTRO	OL REGISTER	1		
R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
DMC	DE<1:0>	DSTP	SMR	<1:0>	SMOD	E<1:0>	SSTP
bit 7 bit							
Legend:							
R = Reada	ble bit	W = Writable bit	:	U = Unimplemen	ted bit, read as '0	,	
u = Bit is u	nchanged	x = Bit is unknow	wn	-n/n = Value at P	OR and BOR/Valu	ue at all other Re	sets
11 = Reserved, Do not use 10 = DMAxDPTR<15:0> is decremented after each transfer completion 01 = DMAxDPTR<15:0> is incremented after each transfer completion 00 = DMAxDPTR<15:0> remains unchanged after each transfer completion bit 5 DSTP: Destination Counter Reload Stop bit							
	0 = SIRQEN	bit is not clear	ed when Destin	ation Counter re	loads		
bit 4-3	SMR[1:0]: So	ource Memory F	Region Select bi	ts			
	1x =DMAxSSA<21:0> points to Data EEPROM01 =DMAxSSA<21:0> points to Program Flash Memory00 =DMAxSSA<21:0> points to SFR/GPR Data Space						
bit 2-1	SMODE[1:0]	: Source Addres	ss Mode Selecti	on bits			
	11 = Reser	ved, Do not use	; 				

- 10 = DMAxSPTR<21:0> is decremented after each transfer completion
- 01 = DMAxSPTR<21:0> is incremented after each transfer completion
- 00 = DMAxSPTR<21:0> remains unchanged after each transfer completion
- bit 0 **SSTP:** Source Counter Reload Stop bit
 - 1 = SIRQEN bit is cleared when Source Counter reloads
 - 0 = SIRQEN bit is not cleared when Source Counter reloads

20.3 Programmable Prescaler

A software programmable prescaler is available for exclusive use with Timer0. There are 16 prescaler options for Timer0 ranging in powers of two from 1:1 to 1:32768. The prescaler values are selected using the CKPS<3:0> bits of the T0CON1 register.

The prescaler is not directly readable or writable. Clearing the prescaler register can be done by writing to the TMR0L register or to the T0CON0/T0CON1 register or by any Reset.

20.4 Programmable Postscaler

A software programmable postscaler (output divider) is available for exclusive use with Timer0. There are 16 postscaler options for Timer0 ranging from 1:1 to 1:16. The postscaler values are selected using the OUTPS bits of the T0CON0 register.

The postscaler is not directly readable or writable. Clearing the postscaler register can be done by writing to the TMR0L register or to the T0CON0/T0CON1 register or by any Reset.

20.5 Operation During Sleep

When operating synchronously, Timer0 will halt. When operating asynchronously, Timer0 will continue to increment and wake the device from Sleep (if Timer0 interrupts are enabled) provided that the input clock source is active.

20.6 Timer0 Interrupts

The Timer0 interrupt flag bit (TMR0IF) is set when either of the following conditions occur:

- 8-bit TMR0L matches the TMR0H value
- 16-bit TMR0 rolls over from 'FFFFh'

When the postscaler bits (OUTPS) are set to 1:1 operation (no division), the T0IF flag bit will be set with every TMR0 match or rollover. In general, the TMR0IF flag bit will be set every OUTPS +1 matches or rollovers.

If Timer0 interrupts are enabled (TMR0IE bit of the PIE3 register = '1'), the CPU will be interrupted and the device may wake from Sleep (see **Section 20.2 "Clock Source Selection"** for more details).

20.7 Timer0 Output

The Timer0 output can be routed to any I/O pin via the RxyPPS output selection register (see **Section 17.0 "Peripheral Pin Select (PPS) Module**" for additional information). The Timer0 output can also be used by other peripherals, such as the auto-conversion trigger of the Analog-to-Digital Converter. Finally, the Timer0 output can be monitored through software via the Timer0 output bit (OUT) of the T0CON0 register (Register 20-1).

TMR0_out will be a pulse of one postscaled clock period when a match occurs between TMR0L and PR0 (Period register for TMR0) in 8-bit mode, or when TMR0 rolls over in 16-bit mode. The Timer0 output is a 50% duty cycle that toggles on each TMR0_out rising clock edge.

22.5.8 LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODES

In Level Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from reset level to the active level while the ON bit is set. Reset levels are selected as follows:

- Low reset level (MODE<4:0> = 01110)
- High reset level (MODE<4:0> = 01111)

When the timer count matches the T2PR period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a T2PR match or by software control a new external signal edge is required after the ON bit is set to start the counter.

When Level Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse-width count. The PWM drive does not go active when the timer count clears at the T2PR period count match.

FIGURE 22-11: LOW LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 01110)



23.0 CAPTURE/COMPARE/PWM MODULE

The Capture/Compare/PWM module is a peripheral that allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate pulse-width modulated signals of varying frequency and duty cycle.

This family of devices contains four standard Capture/ Compare/PWM modules (CCP1, CCP2, CCP3 and CCP4). Each individual CCP module can select the timer source that controls the module. Each module has an independent timer selection which can be accessed using the CxTSEL bits in the CCPTMRS0 register (Register 23-2). The default timer selection is TMR1 when using Capture/Compare mode and TMR2 when using PWM mode in the CCPx module.

Please note that the Capture/Compare mode operation is described with respect to TMR1 and the PWM mode operation is described with respect to TMR2 in the following sections.

The Capture and Compare functions are identical for all CCP modules.

- Note 1: In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.
 - 2: Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to CCPx module. Register names, module signals, I/O pins, and bit names may use the generic designator 'x' to indicate the use of a numeral to distinguish a particular module, when required.

23.1 CCP Module Configuration

Each Capture/Compare/PWM module is associated with a control register (CCPxCON), a capture input selection register (CCPxCAP) and a data register (CCPRx). The data register, in turn, is comprised of two 8-bit registers: CCPRxL (low byte) and CCPRxH (high byte).

23.1.1 CCP MODULES AND TIMER RESOURCES

The CCP modules utilize Timers 1 through 6 that vary with the selected mode. Various timers are available to the CCP modules in Capture, Compare or PWM modes, as shown in Table 23-1.

TABLE 23-1: CCP MODE – TIMER RESOURCE

CCP Mode	Timer Resource			
Capture	T			
Compare	Timer1, Timer3 or Timer5			
PWM	Timer2, Timer4 or Timer6			

The assignment of a particular timer to a module is determined by the timer to CCP enable bits in the CCPTMRS0 register (see Register 23-2) All of the modules may be active at once and may share the same timer resource if they are configured to operate in the same mode (Capture/Compare or PWM) at the same time.

23.1.2 OPEN-DRAIN OUTPUT OPTION

When operating in Output mode (the Compare or PWM modes), the drivers for the CCPx pins can be optionally configured as open-drain outputs. This feature allows the voltage level on the pin to be pulled to a higher level through an external pull-up resistor and allows the output to communicate with external circuits without the need for additional level shifters.





R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1
P8TSE	L<1:0>	P7TSE	L<1:0>	P6TSE	EL<1:0>	P5TSE	L<1:0>
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 7-6	P8TSEL<1:0> 11 = PWM8 b 10 = PWM8 b 01 = PWM8 b 00 = PWM8 b	•: PWM8 Time based on TMR based on TMR based on TMR based on TMR	r Selection bit 3 5 4 2	S			
bit 5-4	P7TSEL<1:0> 11 = PWM7 k 10 = PWM7 k 01 = PWM7 k 00 = PWM7 k	PWM7 Time based on TMR8 based on TMR6 based on TMR6 based on TMR6 based on TMR8	^r Selection bit 3 5 4 2	s			
bit 3-2	P6TSEL<1:0> 11 = PWM6 k 10 = PWM6 k 01 = PWM6 k 00 = PWM6 k	•: PWM6 Time based on TMR8 based on TMR6 based on TMR6 based on TMR	⁻ Selection bit 3 5 4 2	S			
bit 1-0	P5TSEL<1:0> 11 = PWM5 k 10 = PWM5 k 01 = PWM5 k 00 = PWM5 k	•: PWM5 Times based on TMR8 based on TMR6 based on TMR6 based on TMR	^r Selection bit 3 5 4 2	S			

REGISTER 23-3: CCPTMRS1: CCP TIMERS CONTROL REGISTER 1

24.2 Register Definitions: PWM Control

Long bit name prefixes for the PWM peripherals are shown below. Refer to **Section 1.3.2.2 "Long Bit Names"** for more information.

Peripheral	Bit Name Prefix
PWM3	PWM3
PWM4	PWM4

REGISTER 24-1: PWMxCON: PWM CONTROL REGISTER

R/W-0/0	U-0	R-0/0	R/W-0/0	U-0	U-0	U-0	U-0
EN	—	OUT	POL	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	EN: PWM Module Enable bit
	1 = PWM module is enabled0 = PWM module is disabled
bit 6	Unimplemented: Read as '0'
bit 5	OUT: PWM Module Output Level When Bit is Read
bit 4	POL: PWM Output Polarity Select bit
	1 = PWM output is inverted0 = PWM output is normal
bit 3-0	Unimplemented: Read as '0'

30.1 DSM Operation

The DSM module can be enabled by setting the EN bit in the MD1CON0 register. Clearing the EN bit in the MD1CON0 register, disables the DSM module output and switches the carrier high and carrier low signals to the default option of MD1CARHPPS and MD1CARLPPS, respectively. The modulator signal source is also switched to the BIT in the MD1CON0 register.

The values used to select the carrier high, carrier low, and modulator sources held by the Modulation Source, Modulation High Carrier, and Modulation Low Carrier control registers are not affected when the EN bit is cleared and the DSM module is disabled. The values inside these registers remain unchanged while the DSM is inactive. The sources for the carrier high, carrier low and modulator signals will once again be selected when the EN bit is set and the DSM module is again enabled and active.

30.2 Modulator Signal Sources

The modulator signal can be supplied from the sources specified in Table 30-3.

The modulator signal is selected by configuring the MS<4:0> bits in the MD1SRC register.

30.3 Carrier Signal Sources

The carrier high signal and carrier low signal can be supplied from the sources specified in Table 30-1.

The carrier high signal is selected by configuring the CH<4:0> bits in the MD1CARH register. The carrier low signal is selected by configuring the CL<4:0> bits in the MD1CARL register.

30.4 Carrier Synchronization

During the time when the DSM switches between carrier high and carrier low signal sources, the carrier data in the modulated output signal can become truncated. To prevent this, the carrier signal can be synchronized to the modulator signal. When synchronization is enabled, the carrier pulse that is being mixed at the time of the transition is allowed to transition low before the DSM switches over to the next carrier source.

Synchronization is enabled separately for the carrier high and carrier low signal sources. Synchronization for the carrier high signal is enabled by setting the CHSYNC bit in the MD1CON1 register. Synchronization for the carrier low signal is enabled by setting the CLSYNC bit in the MD1CON1 register.

Figure 30-2 through Figure 30-6 show timing diagrams of using various synchronization methods.

31.16 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as VDD or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value of the OSCTUNE register allows for fine resolution changes to the system clock source. See **Section 7.2.2.3 "Internal Oscillator Frequency Adjustment"** for more information.

The other method adjusts the value of the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see **Section 31.17.1 "Auto-Baud Detect"**). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change of the peripheral clock frequency.

31.17 UART Baud Rate Generator (BRG)

The Baud Rate Generator (BRG) is a 16-bit timer that is dedicated to the support of the UART operation.

The UxBRGH, UxBRGL register pair determines the period of the free running baud rate timer. The multiplier of the baud rate period is determined by the BRGS bit in the UxCON0 register.

Table 31-1 contains the formulas for determining the baud rate. Example 31-1 provides a sample calculation for determining the baud rate and baud rate error.

The high baud rate range (BRGS = 1) is intended to extend the baud rate range up to a faster rate when the desired baud rate is not possible otherwise. Using the normal baud rate range (BRGS = 0) is recommended when the desired baud rate is achievable with either range.

Writing a new value to the UxBRGH, UxBRGL register pair causes the BRG timer to be reset (or cleared). This ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

If the system clock is changed during an active receive operation, a receive error or data loss may result. To avoid this problem, check the status of the RXIDL bit to make sure that the receive operation is idle before changing the system clock.

EXAMPLE 31-1: CALCULATING BAUD RATE ERROR



TABLE 31-1: BAUD RATE FORMULAS

BRGS	BRG/UART Mode	Baud Rate Formula
1	High Rate	Fosc/[4 (n+1)]
0	Normal Rate	Fosc/[16(n+1)]

Legend: n = value of UxBRGH, UxBRGL register pair.

32.8.3.1 Shift Register Empty Interrupt

The Shift Register Empty interrupt flag and enable are the SRMTIF and SRMTIE bits, respectively. This interrupt is only available in Master mode and triggers when a data transfer completes and conditions are not present to start a new transfer, as dictated by the TXR and RXR bits (see Table 32-1 for conditions for starting a new Master mode data transfer with different TXR/ RXR settings). This interrupt will be triggered at the end of the last full bit period, after SCK has been low for one 1/2-baud period. See Figure 32-14 for more details of the timing of this interrupt as well as other interrupts. This bit will not clear itself when the conditions for starting a new transfer occur, and must be cleared in software.

32.8.3.2 Transfer Counter is Zero Interrupt

The transfer counter is zero interrupt flag and enable are the TCZIF and TCZIE bits, respectively. This interrupt will trigger when the transfer counter (defined by BMODE, SPIxTCTH/L and SPIxTWIDTH) decrements from one to zero. See Figure 32-14 for more details on the timing of this interrupt as well as other interrupts. This bit must be cleared in software. Note: The TCZIF flag only indicates that the transfer counter has decremented from one to zero, and may not indicate that the entire data transfer process is complete. Either poll the BUSY bit of SPIxCON2 and wait for it to be cleared or use the Shift Register Empty Interrupt (SRMTIF) to determine if a data transfer is fully complete.

32.8.3.3 Start of Slave Select and End of Slave Select Interrupts

The start of Slave Select interrupt flag and enable are the SOSIF and SOSIE bits, respectively, and the end of Slave Select interrupt flag and enable are similarly designated by the EOSIF and EOSIE bits. These interrupts trigger at the leading and trailing edges of the Slave Select input. Note that the interrupts are active in both master and Slave mode, and will trigger on transitions of the Slave Select input regardless of which mode the SPI is in. In Master mode, PPS should be used to route the Slave Select input to the same pin as the Slave Select output, allowing these interrupts to trigger on changes to the Slave Select output. Also note that in Slave mode, changing the SSET bit can trigger these interrupts, as it changes the effective input value of Slave Select. Both SOSIF and EOSIF must be cleared in software



FIGURE 32-14: TRANSFER AND SLAVE SELECT INTERRUPT TIMINGS

U-0 U-0 U-0 U-0 R/W-x/u R/W-x/u R/W-x/u R/W-x/u ADRES<11:8> ___ _ ____ ____ bit 7 bit 0 Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n/n = Value at POR and BOR/Value at all other Resets u = Bit is unchanged x = Bit is unknown

REGISTER 37-20: ADRESH: ADC RESULT REGISTER HIGH, FM = 1

bit 7-4 Reserved

'1' = Bit is set

bit 3-0 ADRES<11:8>: ADC Sample Result bits. Upper four bits of 12-bit conversion result.

REGISTER 37-21: ADRESL: ADC RESULT REGISTER LOW, FM = 1

'0' = Bit is cleared

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
			ADRES	S<7:0>			
bit 7 bit 0							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 ADRES<7:0>: ADC Result Register bits. Lower eight bits of 12-bit conversion result.

REGISTER 37-32: ADLTHL: ADC LOWER THRESHOLD LOW BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
			LTH	<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimplen	nented bit, read	d as '0'	
u = Bit is unch	anged	x = Bit is unkn	iown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				

bit 7-0 LTH<7:0>: ADC Lower Threshold LSB. LTH and UTH are compared with ERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

REGISTER 37-33: ADUTHH: ADC UPPER THRESHOLD HIGH BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
			UTH<	15:8>			
bit 7							bit 0
Legend:							
R = Readable bi	t	W = Writable bit	ŀ	II = I Inimpler	mented hit read	1 as '0'	

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **UTH<15:8>**: ADC Upper Threshold MSB. LTH and UTH are compared with ERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

REGISTER 37-34: ADUTHL: ADC UPPER THRESHOLD LOW BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
UTH<7:0>							
bit 7	bit 7 bit						bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **UTH<7:0>**: ADC Upper Threshold LSB. LTH and UTH are compared with ERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

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39.0 COMPARATOR MODULE

Note: The PIC18(L)F25/26K83 devices have two comparators. Therefore, all information in this section refers to both C1 and C2.

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution.

The analog comparator module includes the following features:

- Programmable input selection
- Programmable output polarity
- Rising/falling output edge interrupts

39.1 Comparator Overview

A single comparator is shown in Figure 39-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.





PIC18(L)F25/26K83

CALLW	Subroutine Call Using WREG						
Syntax:	CALLW						
Operands:	None						
Operation:	$(PC + 2) \rightarrow TOS,$ $(W) \rightarrow PCL,$ $(PCLATH) \rightarrow PCH,$ $(PCLATU) \rightarrow PCU$						
Status Affected:	None						
Encoding:	0000	0000	0100				
Description	First, the return address (PC + 2) is pushed onto the return stack. Next, the contents of W are written to PCL; the existing value is discarded. Then, the contents of PCLATH and PCLATU are latched into PCH and PCU, respectively. The second cycle is executed as a NOP instruction while the new next instruction is fetched. Unlike CALL, there is no option to update W, Status or BSR.						
Words:							
Cycles:	2						
Q Cycle Activity:							
	Q1	Q2	Q3	Q4			
	Decode	Read WREG	PUSH PC to stack	No operation			
	No operation	No opera- tion	No operation	No operation			
Example:	HERE	CALLW					
Before Instructio PC = PCLATH = PCLATU = W = W = After Instruction PC = TOS = PCLATH = PCLATU = W =	n addres 10h 00h 00h 06h 001006 addres 10h 00h 00h	S (HERE Sh S (HERE) + 2)				

CLR	RF	Clear f							
Synt	ax:	CLRF f{	CLRF f {,a}						
Oper	rands:	$\begin{array}{l} 0 \leq f \leq 255 \\ a \in [0,1] \end{array}$							
Oper	ration:	$\begin{array}{l} 000h \rightarrow f \\ 1 \rightarrow Z \end{array}$							
Statu	is Affected:	Z							
Enco	oding:	0110	0110 101a ffff ffff						
		register. If 'a' is '0', If 'a' is '1', GPR bank If 'a' is '0' a set is enab in Indexed mode whe tion 42.2.3 Oriented I eral Offse	register. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Sec- tion 42.2.3 "Byte-Oriented and Bit- Oriented Instructions in Indexed Lit- eral Offset Mode" for details						
Word	ds:	1	1						
Cycles:		1							
QC	ycle Activity:								
	Q1	Q2	Q3	}	Q4				
	Decode	Read register 'f'	Proce Dat	ess a	Write register 'f'				
Example: CLRF FLAG_REG, 1 Before Instruction FLAG_REG = 5Ah After Instruction									
$FLAG_REG = 00n$									

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
3773h	B3EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	626
3772h	B3SIDL	SID2	SID1	SID0	SRR	EXIDE	_	EID17	EID16	625
3771h	B3SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	624
3770h	B3CON	RXFUL	RXM1	RXRTRRO	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0	622
3770h	B3CON	TXBIF	TXABT	TXLARB	TXERR	TXREQ	RTREN	TXPRI1	TXPRI0	623
376Fh	CANCON_RO7				CANCON	I_R07				603
376Eh	CANSTAT_R07				CANSTA	[_R07				604
376Dh	B2D7		 B2D7							627
376Ch	B2D6		B2D6							627
376Bh	B2D5		B2D5							627
376Ah	B2D4				B2D	4				627
3769h	B2D3				B2D	3				627
3768h	B2D2				B2D	2				627
3767h	B2D1				B2D	1				627
3766h	B2D0				B2D	0				627
3765h	B2DLC	_	RXRTR	RB1	RB0	DLC3	DLC2	DLC1	DLC0	628
3765h	B2DLC	_	TXRTR	_	_	DLC3	DLC2	DLC1	DLC0	629
3764h	B2EIDL	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	626
3763h	B2EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	626
3762h	B2SIDL	SID2	SID1	SID0	SRR	EXIDE	_	EID17	EID16	625
3761h	B2SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	624
3760h	B2CON	RXFUL	RXM1	RXRTRRO	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0	622
3760h	B2CON	TXBIF	TXABT	TXLARB	TXERR	TXREQ	RTREN	TXPRI1	TXPRI0	623
375Fh	CANCON_RO8	CANCON_RO8						603		
375Eh	CANSTAT_RO8	CANSTAT_RO8						604		
375Dh	B1D7		B1D7						627	
375Ch	B1D6		B1D6						627	
375Bh	B1D5		B1D5						627	
375Ah	B1D4		B1D4						627	
3759h	B1D3		B1D3						627	
3758h	B1D2		B1D2						627	
3757h	B1D1	B1D1						627		
3756h	B1D0	B1D0						627		
3755h	B1DLC	_	RXRTR	RB1	RB0	DLC3	DLC2	DLC1	DLC0	628
3755h	B1DLC	_	TXRTR	_	_	DLC3	DLC2	DLC1	DLC0	629
3754h	B1EIDL	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	626
3753h	B1EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	626
3752h	B1SIDL	SID2	SID1	SID0	SRR	EXIDE	_	EID17	EID16	625
3751h	B1SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	624
3750h	B1CON	RXFUL	RXM1	RXRTRRO	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0	622
3750h	B1CON	TXBIF	TXABT	TXLARB	TXERR	TXREQ	RTREN	TXPRI1	TXPRI0	623
374Fh	CANCON_RO9	CANCON_RO9						603		
374Eh	CANSTAT_RO9	CANSTAT_RO9						604		
374Dh	B0D7		B0D7						627	
374Ch	B0D6	B0D6						627		
374Bh	B0D5	B0D5						627		
374Ah	B0D4	B0D4						627		
3749h	B0D3	B0D3						627		
3748h	B0D2	B0D2						627		
3747h	B0D1	B0D1					627			
Legend: x = unknown u = unchanged — = unimplemented a = value depends on condition							•			

Not present in LF devices. Note 1:

45.0 ELECTRICAL SPECIFICATIONS

45.1 Absolute Maximum Ratings ^(†)	
Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on pins with respect to Vss	
on VDD pin	
PIC18F25/26K83	-0.3V to +6.5V
PIC18LF25/26K83	-0.3V to +4.0V
on MCLR pin	-0,3V to +9.0V
on all other pins	to (VDD + 0.3V)
Maximum current	•
on Vss pin ⁽¹⁾	
-40°C ≤ TA ≤ +85°C	350 mA
85°C < TA ≤ +125°C	120 mA
on VDD pin for 28-Pin devices ⁽¹⁾	
$-40^{\circ}C \le TA \le +85^{\circ}C$	250 mA
85°C < TA ≤ +125°C	85 mA
on any standard I/O pin	±50 mA
Clamp current, IK (VPIN < 0 or VPIN > VDD)	±20 mA
Total power dissipation ⁽²⁾	800 mW

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 45-6 to calculate device specifications.

- 2: Power dissipation is calculated as follows:
 - PDIS = VDD x {IDD Σ {OH} + Σ {(VDD VOH) x IOH} + Σ (VOI x IOL)

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.