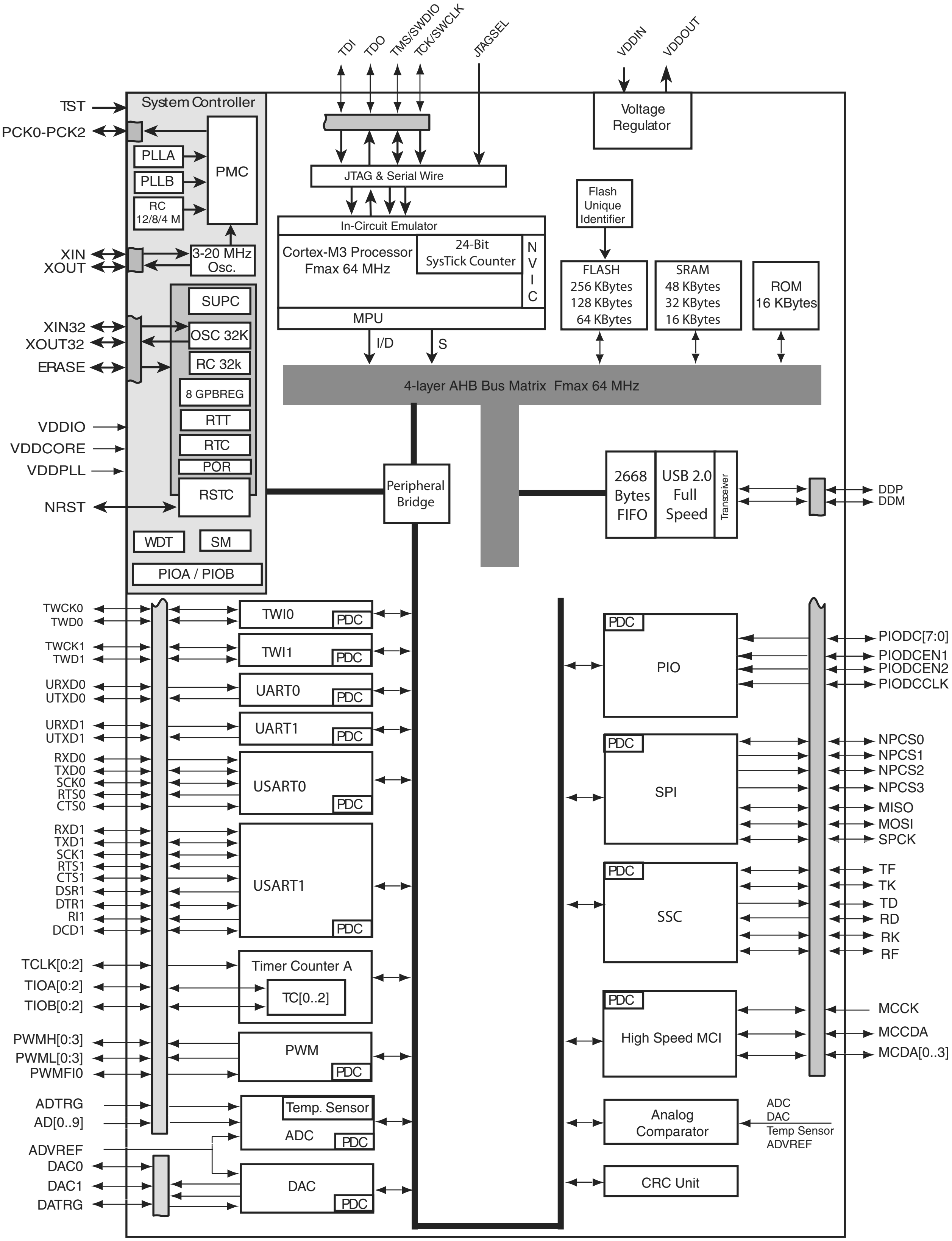
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	I²C, MMC, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	47
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x10/12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3s1bb-au

1. Features

- Core
  - ARM® Cortex®-M3 revision 2.0 running at up to 64 MHz
  - Memory Protection Unit (MPU)
  - Thumb®-2 instruction set
- Pin-to-pin compatible with AT91SAM7S series (48- and 64-pin versions)
- Memories
  - From 64 to 256 Kbytes embedded Flash, 128-bit wide access, memory accelerator, single plane
  - From 16 to 48 Kbytes embedded SRAM
  - 16 Kbytes ROM with embedded bootloader routines (UART, USB) and IAP routines
  - 8-bit Static Memory Controller (SMC): SRAM, PSRAM, NOR and NAND Flash support
  - Memory Protection Unit (MPU)
- System
  - Embedded voltage regulator for single supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz main power with Failure Detection and optional low power 32.768 kHz for RTC or device clock
  - High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz default frequency for device startup. In-application trimming access for frequency adjustment
  - Slow Clock Internal RC oscillator as permanent low-power mode device clock
  - Two PLLs up to 130 MHz for device clock and for USB
  - Temperature Sensor
  - Up to 22 peripheral DMA (PDC) channels
- Low Power Modes
  - Sleep and Backup modes, down to 1.8 µA in Backup mode
  - Ultra low power RTC
- Peripherals
  - USB 2.0 Device: 12 Mbps, 2668 byte FIFO, up to 8 bidirectional Endpoints. On-Chip Transceiver
  - Up to 2 USARTs with ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Mode
  - Two 2-wire UARTs
  - Up to 2 Two Wire Interface (I2C compatible), 1 SPI, 1 Serial Synchronous Controller (I2S), 1 High Speed Multimedia Card Interface (SDIO/SD Card/MMC)
  - Up to 6 Three-Channel 16-bit Timer/Counter with capture, waveform, compare and PWM mode. Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
  - 4-channel 16-bit PWM with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter for Motor Control
  - 32-bit Real-time Timer and RTC with calendar and alarm features
  - Up to 15-channel, 1Msps ADC with differential input mode and programmable gain stage
  - One 2-channel 12-bit 1Msps DAC
  - One Analog Comparator with flexible input selection, Selectable input hysteresis
  - 32-bit Cyclic Redundancy Check Calculation Unit (CRCCU)
  - Write Protected Registers
- I/O
  - Up to 79 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination
  - Three 32-bit Parallel Input/Output Controllers, Peripheral DMA assisted Parallel Capture Mode
- Packages
  - 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm/100-ball TFBGA, 9 x 9 mm, pitch 0.8 mm
  - 64-lead LQFP, 10 x 10 mm, pitch 0.5 mm/64-pad QFN 9x9 mm, pitch 0.5 mm
  - 48-lead LQFP, 7 x 7 mm, pitch 0.5 mm/48-pad QFN 7x7 mm, pitch 0.5 mm

Figure 2-2. SAM3S 64-pin Version Block Diagram



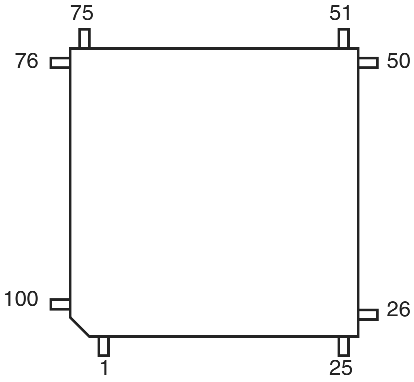
4. Package and Pinout

4.1 SAM3S4/2/1C Package and Pinout

Figure 4-2 shows the orientation of the 100-ball TFBGA Package

4.1.1 100-lead LQFP Package Outline

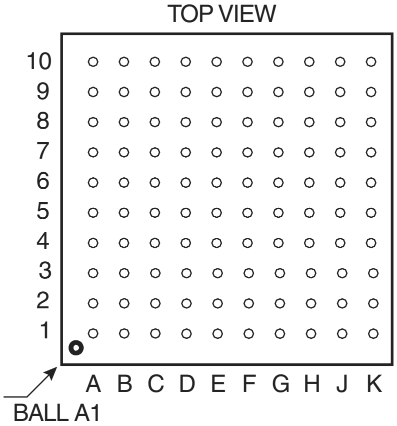
Figure 4-1. Orientation of the 100-lead LQFP Package



4.1.2 100-ball TFBGA Package Outline

The 100-Ball TFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 9 x 9 x 1.1 mm.

Figure 4-2. Orientation of the 100-BALL TFBGA Package



4.2 SAM3S4/2/1B Package and Pinout

Figure 4-3. Orientation of the 64-pad QFN Package

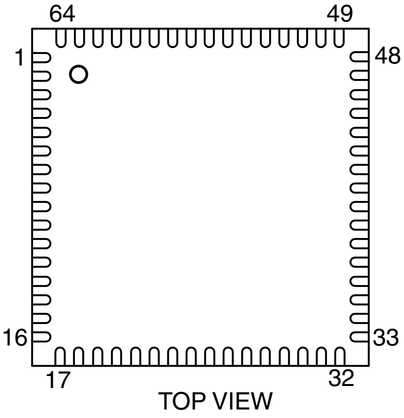


Figure 4-4. Orientation of the 64-lead LQFP Package

64

1

4.3.1 48-Lead LQFP and QFN Pinout

Table 4-4. 48-pin SAM3S4/2/1A Pinout

1	ADVREF	13	VDDIO	25	TDI/PB4	37	TDO/TRACESWO/ PB5
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	PB0/AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS/SWDIO/PB6
4	PB1/AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK/SWCLK/PB7
5	PB2/AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	PB3/AD7	18	VDDCORE	30	TST	42	ERASE/PB12
7	VDDIN	19	PA12/PGMD0	31	PA3	43	DDM/PB10
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	DDP/PB11
9	PA17/PGMD5/ AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT/PB8
10	PA18/PGMD6/ AD1	22	PA9/PGMM1	34	GND	46	XIN/PB9/PGMCK
11	PA19/PGMD7/ AD2	23	PA8/*XOUT32/* PGMM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/*XIN32/* PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

5. Power Considerations

5.1 Power Supplies

The SAM3S product has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals; voltage ranges from 1.62V and 1.95V.
- VDDIO pins: Power the Peripherals I/O lines (Input/Output Buffers); USB transceiver; Backup part, 32kHz crystal oscillator and oscillator pads; ranges from 1.62V and 3.6V
- VDDIN pin: Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply; Voltage ranges from 1.8V to 3.6V
- VDDPLL pin: Powers the PLLA, PLLB, the Fast RC and the 3 to 20 MHz oscillator; voltage ranges from 1.62V and 1.95V.

5.2 Voltage Regulator

The SAM3S embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3S. It features two different operating modes:

- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 µA.

• In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is inferior to 100 µs.

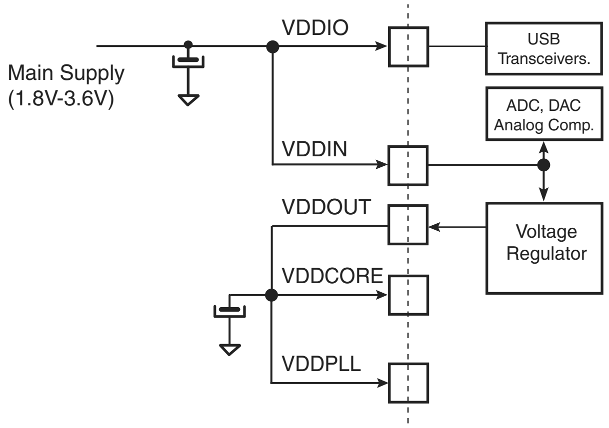
For adequate input and output power supply decoupling/bypassing, refer to the Voltage Regulator section in the Electrical Characteristics section of the datasheet.

5.3 Typical Powering Schematics

The SAM3S supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-1 shows the power schematics.

As VDDIN powers the voltage regulator, the ADC/DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that it is different from Backup mode).

Figure 5-1. Single Supply



Note: For USB, VDDIO needs to be greater than 3.0V.
For ADC, VDDIN needs to be greater than 2.0V.
For DAC, VDDIN needs to be greater than 2.4V.

5.4 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.5 Low Power Modes

The various low power modes of the SAM3S are described below:

5.5.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time (<0.1ms). Total current consumption is 3 µA typical.

The Supply Controller, zero-power power-on reset, RTT, RTC, Backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup mode is based on the Cortex-M3 deepsleep mode with the voltage regulator disabled.

The SAM3S can be awakened from this mode through WUP0-15 pins, the supply monitor (SM), the RTT or RTC wake-up event.

Backup mode is entered by using WFE instructions with the SLEEPDEEP bit in the System Control Register of the Cortex-M3 set to 1. (See the Power management description in The ARM Cortex M3 Processor section of the product datasheet).

Exit from Backup mode happens if one of the following enable wake up events occurs:

- WKUPEN0-15 pins (level transition, configurable debouncing)
- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current Consumption in Wait mode is typically 15 µA (total current consumption) if the internal voltage regulator is used or 8 µA if an external regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake-up the core (WFE). This is done by configuring the external lines WUP0-15 as fast startup wake-up pins (refer to Section 5.7 “Fast Startup”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Entering Wait Mode:

- Select the 4/8/12 MHz fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, Waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

The bit MOSCRCEN should be automatically set to '0'. So you have to add after this instruction the following: while (MOSCRCEN ==0); so that you are sure to stay in the loop until you awake from the wait mode. In that case you are sure the core will not continue to fetch the code but once you have exited the wait mode (in that case MOSCRCEN will be automatically set to '1').

Table 6-1. System I/O Configuration List

SYSTEM_IO bit number	Default function after reset	Other function	Constraints for normal start	Configuration
12	ERASE	PB12	Low Level at startup[1]	In Matrix User Interface Registers (Refer to the SystemIO Configuration Register in the Bus Matrix section of the product datasheet.)
10	DDM	PB10	-	
11	DDP	PB11	-	
7	TCK/SWCLK	PB7	-	
6	TMS/SWDIO	PB6	-	
5	TDO/TRACESWO	PB5	-	
4	TDI	PB4	-	
-	PA7	XIN32	-	See footnote [2] below
-	PA8	XOUT32	-	
-	PB9	XIN	-	See footnote [3] below
-	PB8	XOUT	-	

Notes:
1. If PB12 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PB12 into PIO mode,
2. In the product Datasheet Refer to: Slow Clock Generator of the Supply Controller section.
3. In the product Datasheet Refer to: 3 to 20 MHZ Crystal Oscillator information in PMC section.

6.2.1 Serial Wire JTAG Debug Port (SWJ-DP) Pins

The SWJ-DP pins are TCK/SWCLK, TMS/SWDIO, TDO/SWO, TDI and commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage reference and reset state, refer to Table 3-1 on page 7.

At startup, SWJ-DP pins are configured in SWJ-DP mode to allow connection with debugging probe. Please refer to the Debug and Test Section of the product datasheet.

SWJ-DP pins can be used as standard I/Os to provide users more general input/output pins when the debug port is not needed in the end application. Mode selection between SWJ-DP mode (System IO mode) and general IO mode is performed through the AHB Matrix Special Function Registers (MATRIX_SFR). Configuration of the pad for pull-up, triggers, debouncing and glitch filters is possible regardless of the mode.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

By default, the JTAG Debug Port is active. If the debugger host wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables the JTAG-DP and enables the SW-DP. When the Serial Wire Debug Port is active, TDO/TRACESWO can be used for trace.

The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchronous trace can only be used with SW-DP, not JTAG-DP. For more information about SW-DP and JTAG-DP switching, please refer to the Debug and Test Section.

6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM3S series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the Fast Flash Programming Interface (FFPI) section. For more on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

7. Processor and Architecture

7.1 ARM Cortex-M3 Processor

- Version 2.0
- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store
- Three-stage pipeline
- Single cycle 32-bit multiply
- Hardware divide
- Thumb and Debug states
- Handler and Thread modes
- Low latency ISR entry and exit

7.2 APB/AHB bridge

The SAM3S product embeds one peripheral bridge:

The peripherals of the bridge are clocked by MCK.

7.3 Matrix Masters

The Bus Matrix of the SAM3S product manages 4 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	Cortex-M3 Instruction/Data
Master 1	Cortex-M3 System
Master 2	Peripheral DMA Controller (PDC)
Master 3	CRC Calculation Unit

7.4 Matrix Slaves

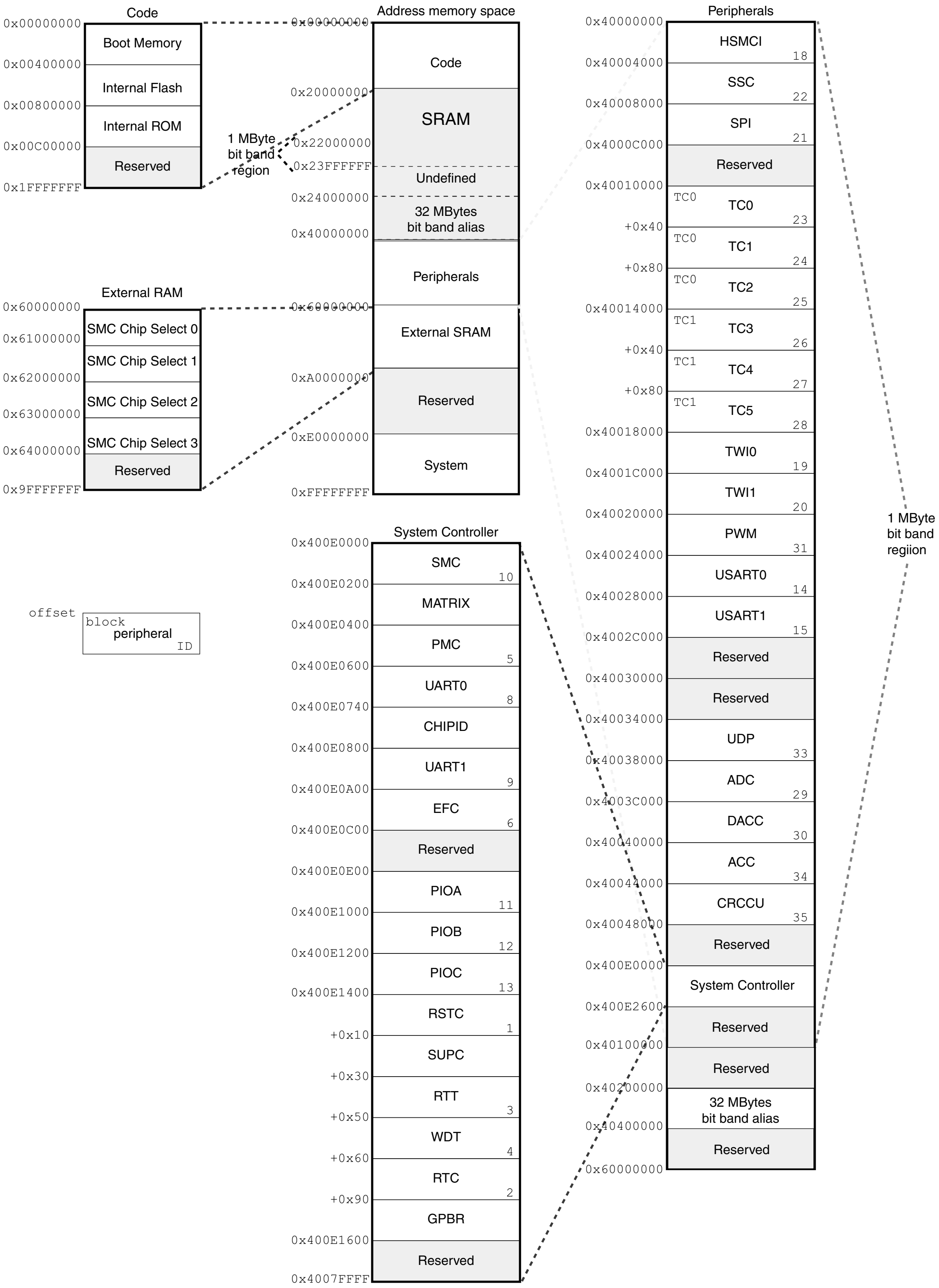
The Bus Matrix of the SAM3S product manages 5 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	Internal Flash
Slave 3	External Bus Interface
Slave 4	Peripheral Bridge

8. Product Mapping

Figure 8-1. SAM3S Product Mapping



9.1.3.5 Lock Regions

Several lock bits used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 9-1. Number of Lock Bits

Product	Number of Lock Bits	Lock Region Size
ATSAM3S4	16	16 kbytes (64 pages)
ATSAM3S2	8	16 kbytes (64 pages)
ATSAM3S1	4	16 kbytes (64 pages)

If a locked-region’s erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.6 Security Bit Feature

The SAM3S features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, SRAM, Core Registers and Internal Peripherals either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the command “Set General Purpose NVM Bit 0” of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash, SRAM, Core registers, Internal Peripherals are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.7 Calibration Bits

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.8 Unique Identifier

Each device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

9.1.3.9 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when TST is tied high and PA0 and PA1 are tied low.

9.1.3.10 SAM-BA® Boot

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART and USB.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

9.1.3.11 GPNVM Bits

The SAM3S features two GPNVM bits that can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

Table 9-2. General Purpose Non-volatile Memory Bits

GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed via GPNVM.

A general-purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

Setting GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

9.2 External Memories

The SAM3S features an External Bus Interface to provide the interface to a wide range of external memories and to any parallel peripheral.

9.2.1 Static Memory Controller

- 8-bit Data Bus
- Up to 24-bit Address Bus (up to 16 MBytes linear per chip select)
- Up to 4 chip selects, Configurable Assignment
- Multiple Access Modes supported
  - Chip Select, Write enable or Read enable Control Mode
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported
- Additional Logic for NAND Flash

10.9 Real Time Timer

- Real Time Timer, allowing backup of time with different accuracies
    - 32-bit free-running back-up counter
    - Integrates a 16-bit programmable prescaler running on slow clock
    - Alarm register capable to generate a wake-up of the system through the Shut Down Controller

10.10 Real Time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

10.11 General Purpose Backup Registers

- Eight 32-bit general-purpose backup registers

10.12 Nested Vectored Interrupt Controller

- Thirty maskable external interrupts
- Sixteen priority levels
- Processor state automatically saved on interrupt entry, and restored on
- Dynamic reprioritization of interrupts
- Priority grouping.
    - selection of preempting interrupt levels and non-preempting interrupt levels.
- Support for tail-chaining and late arrival of interrupts.
    - back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

10.13 Chip Identification

- Chip Identifier (CHIPID) registers permit recognition of the device and its revision.

Table 10-1. SAM3S Chip IDs Register

Chip Name	Flash Size (KBytes)	Pin Count	DBGU_CIDR	CHIPID_EXID
ATSAM3S4A (Rev A)	256	48	0x28800960	0x0
ATSAM3S2A (Rev A)	128	48	0x288A0760	0x0
ATSAM3S1A (Rev A)	64	48	0x28890560	0x0
ATSAM3S4B (Rev A)	256	64	0x28900960	0x0
ATSAM3S2B (Rev A)	128	64	0x289A0760	0x0
ATSAM3S1B (Rev A)	64	64	0x28990560	0x0
ATSAM3S4C (Rev A)	256	100	0x28A00960	0x0
ATSAM3S2C (Rev A)	128	100	0x28AA0760	0x0
ATSAM3S1C (Rev A)	64	100	0x28A90560	0x0

- JTAG ID: 0x05B2D03F

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3S. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 11-1. Peripheral Identifiers

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	**SUPC**	**X**		Supply Controller
1	**RSTC**	**X**		Reset Controller
2	**RTC**	**X**		Real Time Clock
3	**RTT**	**X**		Real Time Timer
4	**WDT**	**X**		Watchdog Timer
5	**PMC**	**X**		Power Management Controller
6	**EEFC**	**X**		Enhanced Embedded Flash Controller
7	**-**	**-**		Reserved
8	**UART0**	**X**	**X**	UART 0
9	**UART1**	**X**	**X**	UART 1
10	**SMC**	**X**	**X**	SMC
11	**PIOA**	**X**	**X**	Parallel I/O Controller A
12	**PIOB**	**X**	**X**	Parallel I/O Controller B
13	**PIOC**	**X**	**X**	Parallel I/O Controller C
14	**USART0**	**X**	**X**	USART 0
15	**USART1**	**X**	**X**	USART 1
16	**-**	**-**	**-**	Reserved
17	**-**	**-**	**-**	Reserved
18	**HSMCI**	**X**	**X**	High Speed Multimedia Card Interface
19	**TWI0**	**X**	**X**	Two Wire Interface 0
20	**TWI1**	**X**	**X**	Two Wire Interface 1
21	**SPI**	**X**	**X**	Serial Peripheral Interface
22	**SSC**	**X**	**X**	Synchronous Serial Controller
23	**TC0**	**X**	**X**	Timer/Counter 0
24	**TC1**	**X**	**X**	Timer/Counter 1
25	**TC2**	**X**	**X**	Timer/Counter 2
26	**TC3**	**X**	**X**	Timer/Counter 3
27	**TC4**	**X**	**X**	Timer/Counter 4
28	**TC5**	**X**	**X**	Timer/Counter 5
29	**ADC**	**X**	**X**	Analog-to-Digital Converter
30	**DACC**	**X**	**X**	Digital-to-Analog Converter
31	**PWM**	**X**	**X**	Pulse Width Modulation
32	**CRCCU**	**X**	**X**	CRC Calculation Unit
33	**ACC**	**X**	**X**	Analog Comparator
34	**UDP**	**X**	**X**	USB Device Port

11.2 Peripheral Signal Multiplexing on I/O Lines

The SAM3S product features 2 PIO controllers on 48-pin and 64-pin versions (PIOA, PIOB) or 3 PIO controllers on the 100-pin version, (PIOA, PIOB, PIOC), that multiplex the I/O lines of the peripheral set.

The SAM3S 64-pin and 100-pin PIO Controllers control up to 32 lines. (See, Table 10-2.) Each line can be assigned to one of three peripheral functions: A, B or C. The multiplexing tables in the following pages define how the I/O lines of the peripherals A, B and C are multiplexed on the PIO Controllers. The column “Comments” has been inserted in this table for the user’s own comments; it may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the tables.

11.2.3 PIO Controller C Multiplexing

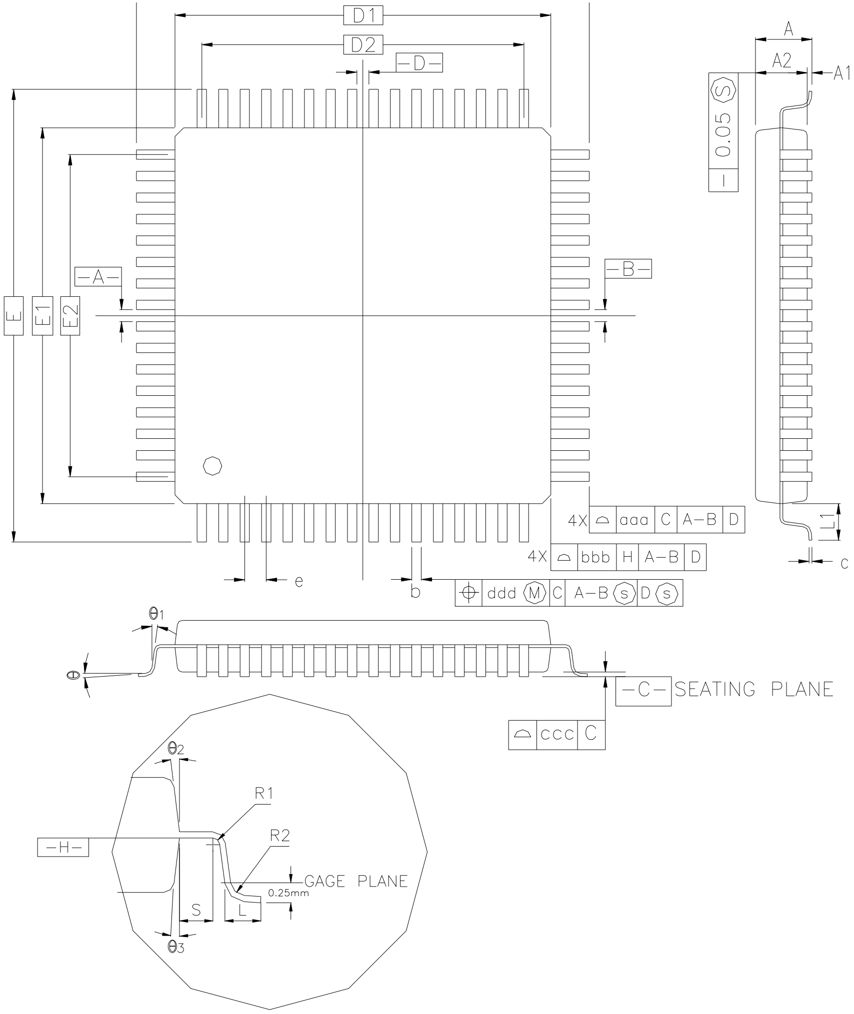
Table 11-4. Multiplexing on PIO Controller C (PIOC)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PC0	D0	PWML0				100-pin version
PC1	D1	PWML1				100-pin version
PC2	D2	PWML2				100-pin version
PC3	D3	PWML3				100-pin version
PC4	D4	NPCS1				100-pin version
PC5	D5					100-pin version
PC6	D6					100-pin version
PC7	D7					100-pin version
PC8	NWE					100-pin version
PC9	NANDOE					100-pin version
PC10	NANDWE					100-pin version
PC11	NRD					100-pin version
PC12	NCS3			AD12		100-pin version
PC13	NWAIT	PWML0		AD10		100-pin version
PC14	NCS0					100-pin version
PC15	NCS1	PWML1		AD11		100-pin version
PC16	A21/NANDALE					100-pin version
PC17	A22/NANDCLE					100-pin version
PC18	A0	PWMH0				100-pin version
PC19	A1	PWMH1				100-pin version
PC20	A2	PWMH2				100-pin version
PC21	A3	PWMH3				100-pin version
PC22	A4	PWML3				100-pin version
PC23	A5	TIOA3				100-pin version
PC24	A6	TIOB3				100-pin version
PC25	A7	TCLK3				100-pin version
PC26	A8	TIOA4				100-pin version
PC27	A9	TIOB4				100-pin version
PC28	A10	TCLK4				100-pin version
PC29	A11	TIOA5		AD13		100-pin version
PC30	A12	TIOB5		AD14		100-pin version
PC31	A13	TCLK5				100-pin version

13. Package Drawings

The SAM3S series devices are available in LQFP, QFN and TFBGA packages.

Figure 13-1. 100-lead LQFP Package Mechanical Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

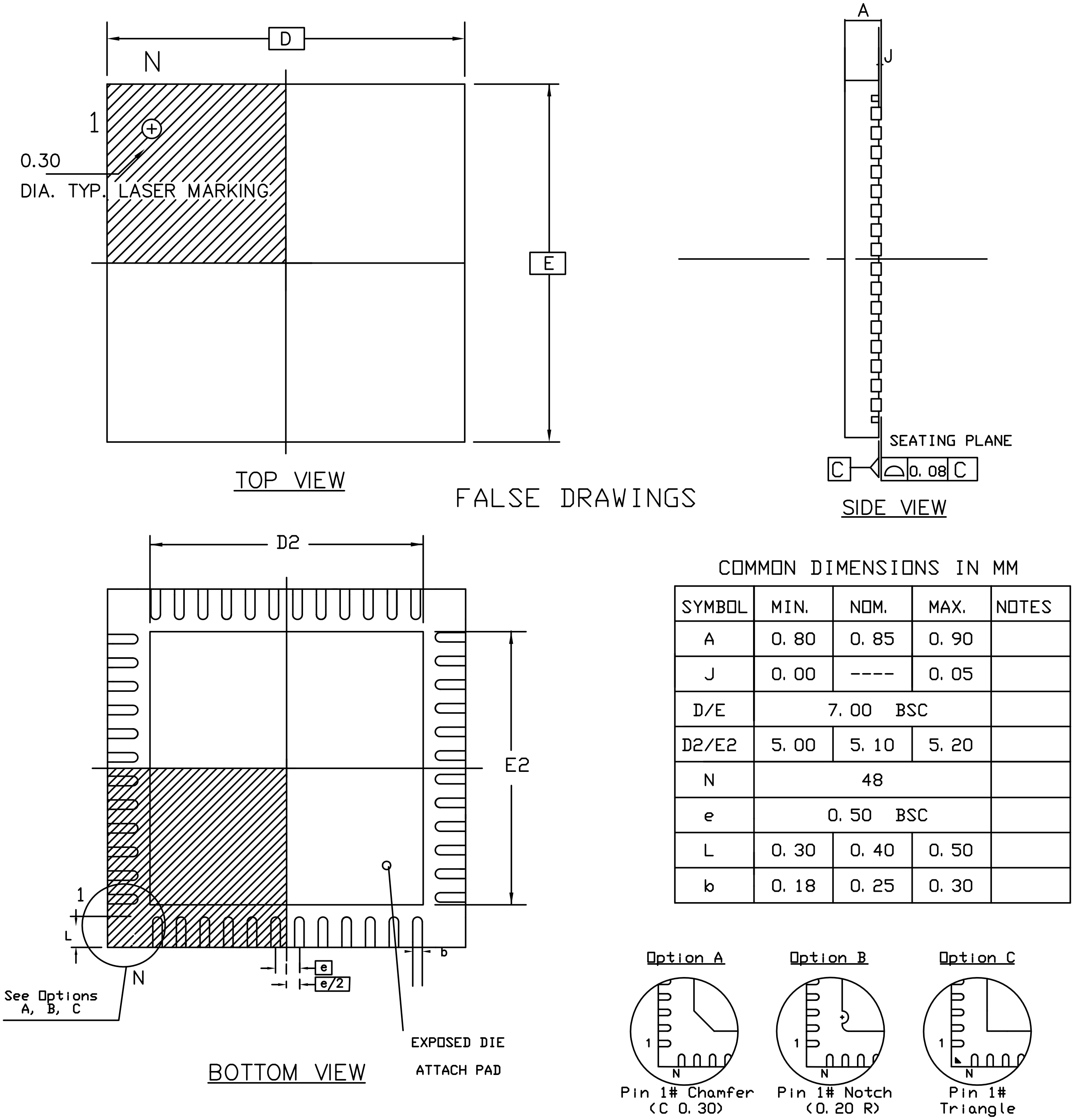
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	
A	—	—	1.60	—	—	0
A_1	0.05	—	0.15	0.002	—	0
A_2	1.35	1.40	1.45	0.053	0.055	0
D	16.00 BSC.			0.630 BSC		
D_1	14.00 BSC.			0.551 BSC		
E	16.00 BSC.			0.630 BSC		
E_1	14.00 BSC.			0.551 BSC		
R_2	0.08	—	0.20	0.003	—	0
R_1	0.08	—	—	0.003	—	
θ	0°	3.5°	7°	0°	3.5°	
θ_1	0°	—	—	0°	—	
θ_2	11°	12°	13°	11°	12°	
θ_3	11°	12°	13°	11°	12°	
c	0.09	—	0.20	0.004	—	0
L	0.45	0.60	0.75	0.018	0.024	0
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	
b	0.17	0.20	0.27	0.007	0.008	
e	0.50 BSC.			0.020 BSC.		
D2	12.00			0.472		
E2	12.00			0.472		
	TOLERANCES OF FORM AND POSITIC					
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Note : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026 for additional information.

Table 13-2. 64-lead LQFP Package Dimensions (in mm)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.383 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.383 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 13-4. 48-pad QFN Package



COMMON DIMENSIONS IN MM

SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	0.85	0.90	
J	0.00	----	0.05	
D/E	7.00 BSC			
D2/E2	5.00	5.10	5.20	
N	48			
e	0.50 BSC			
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	

14. Ordering Information

Table 14-1. Ordering Codes for SAM3S Series Devices

Ordering Code	MRL A	MRL B	Flash (Kbytes)	Package (Kbytes)	Package Type	Temperature Operating Range
ATSAM3S4CA-AU	A	–	256	QFP100	Green	Industrial -40°C to 85°C
ATSAM3S4CA-CU	A	–	256	BGA100	Green	Industrial -40°C to 85°C
ATSAM3S4BA-AU	A	–	256	QFP64	Green	Industrial -40°C to 85°C
ATSAM3S4BA-MU	A	–	256	QFN64	Green	Industrial -40°C to 85°C
ATSAM3S4AA-AU	A	–	256	QFP48	Green	Industrial -40°C to 85°C
ATSAM3S4AA-MU	A	–	256	QFN48	Green	Industrial -40°C to 85°C
ATSAM3S2CA-AU	A	–	128	QFP100	Green	Industrial -40°C to 85°C
ATSAM3S2CA-CU	A	–	128	BGA100	Green	Industrial -40°C to 85°C
ATSAM3S2BA-AU	A	–	128	QFP64	Green	Industrial -40°C to 85°C
ATSAM3S2BA-MU	A	–	128	QFN64	Green	Industrial -40°C to 85°C
ATSAM3S2AA-AU	A	–	128	QFP48	Green	Industrial -40°C to 85°C
ATSAM3S2AA-MU	A	–	128	QFN48	Green	Industrial -40°C to 85°C
ATSAM3S1CA-AU	A	–	64	QFP100	Green	Industrial -40°C to 85°C
ATSAM3S1CA-CU	A	–	64	BGA100	Green	Industrial -40°C to 85°C
ATSAM3S1BA-AU	A	–	64	QFP64	Green	Industrial -40°C to 85°C
ATSAM3S1BA-MU	A	–	64	QFN64	Green	Industrial -40°C to 85°C
ATSAM3S1AA-AU	A	–	64	QFP48	Green	Industrial -40°C to 85°C
ATSAM3S1AA-MU	A	–	64	QFN48	Green	Industrial -40°C to 85°C
ATSAM3S1CB-AU	–	B	64	QFP100	Green	Industrial -40°C to 85°C
ATSAM3S1CB-CU	–	B	64	BGA100	Green	Industrial -40°C to 85°C
ATSAM3S1BB-AU	–	B	64	QFP64	Green	Industrial -40°C to 85°C
ATSAM3S1BB-MU	–	B	64	QFN64	Green	Industrial -40°C to 85°C
ATSAM3S1AB-AU	–	B	64	QFP48	Green	Industrial -40°C to 85°C
ATSAM3S1AB-MU	–	B	64	QFN48	Green	Industrial -40°C to 85°C