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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	I ² C, MMC, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	47
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x10/12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3s1bb-mu

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2. SAM3S Block Diagram





Figure 2-3. SAM3S 48-pin Version Block Diagram



Signal Name	Function	Type	Active Level	Voltage reference	Comments			
	Universal Asynchronous	Receiver Trans	smitter - U	ARTx				
URXDx	UART Receive Data	Input						
UTXDx	UART Transmit Data	Output						
	PIO Controller - PIOA - PIOB - PIOC							
PA0 - PA31	Parallel IO Controller A	I/O			Reset State:			
PB0 - PB14	Parallel IO Controller B	I/O			- PIO or System IOs ⁽²⁾			
D00 D004		1/0			- Internal pull-up enabled			
PC0 - PC31	Parallel 10 Controller C	1/0			- Schmitt Trigger enabled ⁽¹⁾			
	PIO Controller - Paralle	I Capture Mode	e (PIOA Or	nly)				
PIODC0-PIODC7	Parallel Capture Mode Data	Input		_				
PIODCCLK	Parallel Capture Mode Clock	Input		VDDIO				
PIODCEN1-2	Parallel Capture Mode Enable	Input						
	External	Bus Interface						
D0 - D7	Data Bus	I/O						
A0 - A23	Address Bus	Output						
NWAIT	External Wait Signal	Input	Low					
	Static Memory	y Controller - S	SMC					
NCS0 - NCS3	Chip Select Lines	Output	Low					
NRD	Read Signal	Output	Low					
NWE	Write Enable	Output	Low					
	NAND	Flash Logic						
NANDOE	NAND Flash Output Enable	Output	Low					
NANDWE	NAND Flash Write Enable	Output	Low					
	High Speed Multimed	lia Card Interfa	ce - HSMC					
МССК	Multimedia Card Clock	I/O						
MCCDA	Multimedia Card Slot A Command	I/O						
MCDA0 - MCDA3	Multimedia Card Slot A Data	I/O						
	Universal Synchronous Asynchr	onous Receive	er Transmi	tter USARTx	(
SCKx	USARTx Serial Clock	I/O						
TXDx	USARTx Transmit Data	I/O						
RXDx	USARTx Receive Data	Input						
RTSx	USARTx Request To Send	Output						
CTSx	USARTx Clear To Send	Input						
DTR1	USART1 Data Terminal Ready	I/O						
DSR1	USART1 Data Set Ready	Input						
DCD1	USART1 Data Carrier Detect	Input						
RI1	USART1 Ring Indicator	Input						

Table 3-1. Signal Description List (Continued)

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Туре	Active Level	Voltage reference	Comments			
	Fast Flash Programming Interface - FFPI							
PGMEN0-PGMEN2	Programming Enabling	Input		VDDIO				
PGMM0-PGMM3	Programming Mode	Input						
PGMD0-PGMD15	Programming Data	I/O						
PGMRDY	Programming Ready	Output	High					
PGMNVALID	Data Direction	Output	Low	VDDIO				
PGMNOE	Programming Read	Input	Low					
PGMCK	Programming Clock	Input						
PGMNCMD	Programming Command	Input	Low					
USB Full Speed Device								
DDM	USB Full Speed Data -	A			Reset State:			
DDP	USB Full Speed Data +	Analog, Digital		VDDIO	- USB Mode - Internal Pull-down ⁽³⁾			

Notes: 1. Schmitt Triggers can be disabled through PIO registers.

- 2. Some PIO lines are shared with System IOs.
- 3. Refer to the USB sub section in the product Electrical Characteristics Section for Pull-down value in USB Mode.
- 4. See Section 5.3 "Typical Powering Schematics" for restriction on voltage range of Analog Cells.
- 5. TDO pin is set in input mode when the Cortex-M3 Core is not in debug mode. Thus the internal pull-up corresponding to this PIO line must be enabled to avoid current consumption due to floating input.

4.3.1 48-Lead LQFP and QFN Pinout

Table 4-4.	48-pin SAM3S4/2/1A Pinout
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1	ADVREF	13	VDDIO	25	TDI/PB4	37	TDO/TRACESWO/ PB5
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	PB0/AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS/SWDIO/PB6
4	PB1/AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK/SWCLK/PB7
5	PB2/AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	PB3/AD7	18	VDDCORE	30	TST	42	ERASE/PB12
7	VDDIN	19	PA12/PGMD0	31	PA3	43	DDM/PB10
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	DDP/PB11
9	PA17/PGMD5/ AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT/PB8
10	PA18/PGMD6/ AD1	22	PA9/PGMM1	34	GND	46	XIN/PB9/PGMCK
11	PA19/PGMD7/ AD2	23	PA8/ <i>XOUT3</i> 2/ PGMM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/ <i>XIN32/</i> PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

7. Processor and Architecture

7.1 ARM Cortex-M3 Processor

- Version 2.0
- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store
- Three-stage pipeline
- Single cycle 32-bit multiply
- Hardware divide
- Thumb and Debug states
- Handler and Thread modes
- Low latency ISR entry and exit

7.2 APB/AHB bridge

The SAM3S product embeds one peripheral bridge: The peripherals of the bridge are clocked by MCK.

7.3 Matrix Masters

The Bus Matrix of the SAM3S product manages 4 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Master 0	Cortex-M3 Instruction/Data
Master 1	Cortex-M3 System
Master 2	Peripheral DMA Controller (PDC)
Master 3	CRC Calculation Unit

Table 7-1. List of Bus Matrix Masters

7.4 Matrix Slaves

The Bus Matrix of the SAM3S product manages 5 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	Internal Flash
Slave 3	External Bus Interface
Slave 4	Peripheral Bridge

7.5 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the Cortex-M3 S Bus to the Internal ROM. Thus, these paths are forbidden or simply not wired and shown as "-" in the following table.

	Masters	0	1	2	3
Slaves		Cortex-M3 I/D Bus	Cortex-M3 S Bus	PDC	CRCCU
0	Internal SRAM	-	Х	х	Х
1	Internal ROM	х	-	х	х
2	Internal Flash	х	-	-	Х
3	External Bus Interface	-	Х	Х	Х
4	Peripheral Bridge	-	Х	Х	-

Table 7-3.	SAM3S	Master to	Slave	Access

7.6 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Low bus arbitration overhead
 - One Master Clock cycle needed for a transfer from memory to peripheral
 - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirement

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Instance Name	Channel T/R	100 & 64 Pins	48 Pins
PWM	Transmit	x	х
TWI1	Transmit	x	х
TWIO	Transmit	x	х
UART1	Transmit	x	х
UART0	Transmit	x	х
USART1	Transmit	x	N/A
USART0	Transmit	x	х
DAC	Transmit	x	N/A
SPI	Transmit	x	х
SSC	Transmit	x	х
HSMCI	Transmit	x	N/A
PIOA	Transmit	x	х
TWI1	Receive	x	x
TWIO	Receive	x	x
UART1	Receive	x	N/A
UART0	Receive	x	x

Table 7-4. Peripheral DMA Controller

Table 7-4.	Peripheral	DMA	Controller	(Continued)
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Instance Name	Channel T/R	100 & 64 Pins	48 Pins
USART1	Receive	x	x
USART0	Receive	x	х
ADC	Receive	x	х
SPI	Receive	x	х
SSC	Receive	x	х
HSMCI	Receive	x	N/A
PIOA	Receive	x	x

7.7 Debug and Test Features

- Debug access to all memory and registers in the system, including Cortex-M3 register bank when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE1149.1 JTAG Boundary-can on All Digital Pins

9.1.3.5 Lock Regions

Several lock bits used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Product	Number of Lock Bits	Lock Region Size
ATSAM3S4	16	16 kbytes (64 pages)
ATSAM3S2	8	16 kbytes (64 pages)
ATSAM3S1	4	16 kbytes (64 pages)

Table 9-1. Number of Lock Bits

If a locked-region's erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.6 Security Bit Feature

The SAM3S features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, SRAM, Core Registers and Internal Peripherals either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the command "Set General Purpose NVM Bit 0" of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash, SRAM, Core registers, Internal Peripherals are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.7 Calibration Bits

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.8 Unique Identifier

Each device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

9.1.3.9 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when TST is tied high and PA0 and PA1 are tied low.

9.1.3.10 SAM-BA® Boot

Atmel

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART and USB.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

9.1.3.11 GPNVM Bits

The SAM3S features two GPNVM bits that can be cleared or set respectively through the commands "Clear GPNVM Bit" and "Set GPNVM Bit" of the EEFC User Interface.

Table 9-2.	General Purpose	Non-volatile	Memory Bits
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GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed via GPNVM.

A general-purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands "Clear General-purpose NVM Bit" and "Set General-purpose NVM Bit" of the EEFC User Interface.

Setting GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

9.2 External Memories

The SAM3S features an External Bus Interface to provide the interface to a wide range of external memories and to any parallel peripheral.

9.2.1 Static Memory Controller

- 8-bit Data Bus
- Up to 24-bit Address Bus (up to 16 MBytes linear per chip select)
- Up to 4 chip selects, Configurable Assignment
- Multiple Access Modes supported
 - Chip Select, Write enable or Read enable Control Mode
 - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
 - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
 - Programmable Wait State Generation
 - External Wait Request
 - Programmable Data Float Time
- Slow Clock mode supported
- Additional Logic for NAND Flash

10.9 Real Time Timer

- Real Time Timer, allowing backup of time with different accuracies
 - 32-bit free-running back-up counter
 - Integrates a 16-bit programmable prescaler running on slow clock
 - Alarm register capable to generate a wake-up of the system through the Shut Down Controller

10.10 Real Time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

10.11 General Purpose Backup Registers

• Eight 32-bit general-purpose backup registers

10.12 Nested Vectored Interrupt Controller

- Thirty maskable external interrupts
- Sixteen priority levels
- Processor state automatically saved on interrupt entry, and restored on
- Dynamic reprioritization of interrupts
- Priority grouping.
 - selection of preempting interrupt levels and non-preempting interrupt levels.
 - Support for tail-chaining and late arrival of interrupts.
 - back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

10.13 Chip Identification

• Chip Identifier (CHIPID) registers permit recognition of the device and its revision.

Table 10-1. SAM3S Chip IDs Register

	Flash Size			
Chip Name	(KBytes)	Pin Count	DBGU_CIDR	CHIPID_EXID
ATSAM3S4A (Rev A)	256	48	0x28800960	0x0
ATSAM3S2A (Rev A)	128	48	0x288A0760	0x0
ATSAM3S1A (Rev A)	64	48	0x28890560	0x0
ATSAM3S4B (Rev A)	256	64	0x28900960	0x0
ATSAM3S2B (Rev A)	128	64	0x289A0760	0x0
ATSAM3S1B (Rev A)	64	64	0x28990560	0x0
ATSAM3S4C (Rev A)	256	100	0x28A00960	0x0
ATSAM3S2C (Rev A)	128	100	0x28AA0760	0x0
ATSAM3S1C (Rev A)	64	100	0x28A90560	0x0

JTAG ID: 0x05B2D03F

10.14 UART

- Two-pin UART
 - Implemented features are 100% compatible with the standard Atmel USART
 - Independent receiver and transmitter with a common programmable Baud Rate Generator
 - Even, Odd, Mark or Space Parity Generation
 - Parity, Framing and Overrun Error Detection
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
 - Support for two PDC channels with connection to receiver and transmitter

10.15 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB and PIOC (100-pin version only) controlling a maximum of 79 I/O Lines
- Fully programmable through Set/Clear Registers

Table 10-2. PIO available according to pin count

Version	48 pin	64 pin	100 pin
PIOA	21	32	32
PIOB	13	15	15
PIOC	-	-	32

- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
 - Input change, rising edge, falling edge, low level and level interrupt
 - Debouncing and Glitch filter
 - Multi-drive option enables driving in open drain
 - Programmable pull-up or pull-down on each I/O line
 - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3S. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

			PMC Clock	
Instance ID	Instance Name	NVIC Interrupt	Control	Instance Description
0	SUPC	X		Supply Controller
1	RSTC	X		Reset Controller
2	RTC	X		Real Time Clock
3	RTT	X		Real Time Timer
4	WDT	X		Watchdog Timer
5	PMC	X		Power Management Controller
6	EEFC	X		Enhanced Embedded Flash Controller
7	-	-		Reserved
8	UART0	X	X	UART 0
9	UART1	X	X	UART 1
10	SMC	X	X	SMC
11	PIOA	X	X	Parallel I/O Controller A
12	PIOB	X	X	Parallel I/O Controller B
13	PIOC	X	X	Parallel I/O Controller C
14	USART0	X	X	USART 0
15	USART1	X	X	USART 1
16	-	-	-	Reserved
17	-	-	-	Reserved
18	HSMCI	X	X	High Speed Multimedia Card Interface
19	TWI0	X	X	Two Wire Interface 0
20	TWI1	X	X	Two Wire Interface 1
21	SPI	X	X	Serial Peripheral Interface
22	SSC	X	X	Synchronous Serial Controller
23	TC0	X	X	Timer/Counter 0
24	TC1	X	X	Timer/Counter 1
25	TC2	X	X	Timer/Counter 2
26	TC3	X	X	Timer/Counter 3
27	TC4	X	X	Timer/Counter 4
28	TC5	X	X	Timer/Counter 5
29	ADC	X	X	Analog-to-Digital Converter
30	DACC	X	X	Digital-to-Analog Converter
31	PWM	X	X	Pulse Width Modulation
32	CRCCU	X	X	CRC Calculation Unit
33	ACC	X	X	Analog Comparator
34	UDP	X	X	USB Device Port

Table 11-1. Peripheral Identifiers

11.2.1 PIO Controller A Multiplexing

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PA0	PWMH0	TIOA0	A17	WKUP0		High drive
PA1	PWMH1	TIOB0	A18	WKUP1		High drive
PA2	PWMH2	SCK0	DATRG	WKUP2		High drive
PA3	TWD0	NPCS3				High drive
PA4	TWCK0	TCLK0		WKUP3		
PA5	RXD0	NPCS3		WKUP4		
PA6	TXD0	PCK0				
PA7	RTS0	PWMH3			XIN32	
PA8	CTS0	ADTRG		WKUP5	XOUT32	
PA9	URXD0	NPCS1	PWMFI0	WKUP6		
PA10	UTXD0	NPCS2				
PA11	NPCS0	PWMH0		WKUP7		
PA12	MISO	PWMH1				
PA13	MOSI	PWMH2				
PA14	SPCK	PWMH3		WKUP8		
PA15	TF	TIOA1	PWML3	WKUP14/PIODCEN1		
PA16	тк	TIOB1	PWML2	WKUP15/PIODCEN2		
PA17	TD	PCK1	PWMH3	AD0		
PA18	RD	PCK2	A14	AD1		
PA19	RK	PWML0	A15	AD2/WKUP9		
PA20	RF	PWML1	A16	AD3/WKUP10		
PA21	RXD1	PCK1		AD8		64/100-pin versions
PA22	TXD1	NPCS3	NCS2	AD9		64/100-pin versions
PA23	SCK1	PWMH0	A19	PIODCCLK		64/100-pin versions
PA24	RTS1	PWMH1	A20	PIODC0		64/100-pin versions
PA25	CTS1	PWMH2	A23	PIODC1		64/100-pin versions
PA26	DCD1	TIOA2	MCDA2	PIODC2		64/100-pin versions
PA27	DTR1	TIOB2	MCDA3	PIODC3		64/100-pin versions
PA28	DSR1	TCLK1	MCCDA	PIODC4		64/100-pin versions
PA29	RI1	TCLK2	MCCK	PIODC5		64/100-pin versions
PA30	PWML2	NPCS2	MCDA0	WKUP11/PIODC6		64/100-pin versions
PA31	NPCS1	PCK2	MCDA1	PIODC7		64/100-pin versions

Table 11-2. Multiplexing on PIO Controller A (PIOA)

- By 8 or by-16 over-sampling receiver frequency
- Hardware handshaking RTS-CTS
- Receiver time-out and transmitter timeguard
- Optional Multi-drop Mode with address generation and detection
- Optional Manchester Encoding
- Full modem line support on USART1 (DCD-DSR-DTR-RI)
- RS485 with driver control signal
 - ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
 - NACK handling, error counter with repetition and iteration limit
- SPI Mode
 - Master or Slave
 - Serial Clock programmable Phase and Polarity
 - SPI Serial Clock (SCK) Frequency up to MCK/4
- IrDA modulation and demodulation
 - Communication at up to 115.2 Kbps
- Test Modes
 - Remote Loopback, Local Loopback, Automatic Echo

12.5 Synchronous Serial Controller (SSC)

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I²S, TDM Buses, Magnetic Card Reader)
- Contains an independent receiver and transmitter and a common clock divider
- Offers configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

12.6 Timer Counter (TC)

- Six 16-bit Timer Counter Channels
 - Wide range of functions including:
 - Frequency Measurement
 - Event Counting
 - Interval Measurement
 - Pulse Generation
 - Delay Timing
 - Pulse Width Modulation
 - Up/down Capabilities
 - Each channel is user-configurable and contains:
 - Three external clock inputs
 - Five internal clock inputs
 - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels
- Quadrature decoder
 - Advanced line filtering
 - Position / revolution / speed
- 2-bit Gray Up/Down Counter for Stepper Motor

12.7 Pulse Width Modulation Controller (PWM)

- One Four-channel 16-bit PWM Controller, 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
 - A Modulo n counter providing eleven clocks
 - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
 - Independent Enable Disable Commands
 - Independent Clock Selection
 - Independent Period and Duty Cycle, with Double Buffering
 - Programmable selection of the output waveform polarity
 - Programmable center or left aligned output waveform
 - Independent Output Override for each channel
 - Independent complementary Outputs with 12-bit dead time generator for each channel
 - Independent Enable Disable Commands
 - Independent Clock Selection
 - Independent Period and Duty Cycle, with Double Buffering
- Synchronous Channel mode
 - Synchronous Channels share the same counter
 - Mode to update the synchronous channels registers after a programmable number of periods
- Connection to one PDC channel
 - Offers Buffer transfer without Processor Intervention, to update duty cycle of synchronous channels
- independent event lines which can send up to 4 triggers on ADC within a period
- Programmable Fault Input providing an asynchronous protection of outputs
- Stepper motor control (2 Channels)

12.8 High Speed Multimedia Card Interface (HSMCI)

- 4-bit or 1-bit Interface
- Compatibility with MultiMedia Card Specification Version 4.3
- Compatibility with SD and SDHC Memory Card Specification Version 2.0
- Compatibility with SDIO Specification Version V1.1.
- Compatibility with CE-ATA Specification 1.1
- Cards clock rate up to Master Clock divided by 2
- Boot Operation Mode support
- High Speed mode support
- Embedded power management to slow down clock rate when not used
- HSMCI has one slot supporting
 - One MultiMediaCard bus (up to 30 cards) or
 - One SD Memory Card
 - One SDIO Card
- Support for stream, block and multi-block data read and write

12.9 USB Device Port (UDP)

- USB V2.0 full-speed compliant,12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 2688-byte dual-port RAM for endpoints

- Eight endpoints
 - Endpoint 0: 64 bytes
 - Endpoint 1 and 2: 64 bytes ping-pong
 - Endpoint 3: 64 bytes
 - Endpoint 4 and 5: 512 bytes ping-pong
 - Endpoint 6 and 7: 64 bytes ping-pong
 - Ping-pong Mode (two memory banks) for Isochronous and bulk endpoints
- Suspend/resume logic
- Integrated Pull-up on DDP
- Pull-down resistor on DDM and DDP when disabled

12.10 Analog-to-Digital Converter (ADC)

- up to 16 Channels,
- 10/12-bit resolution
- up to 1 MSample/s
- programmable sequence of conversion on each channel
- Integrated temperature sensor
- Single ended/differential conversion
- Programmable gain: 1, 2, 4

12.11 Digital-to-Analog Converter (DAC)

- Up to 2 channel 12-bit DAC
- Up to 2 mega-samples conversion rate in single channel mode
- Flexible conversion range
- Multiple trigger sources for each channel
- 2 Sample/Hold (S/H) outputs
- Built-in offset and gain calibration
- Possibility to drive output to ground
- Possibility to use as input to analog comparator or ADC (as an internal wire and without S/H stage)
- Two PDC channels
- Power reduction mode

12.12 Static Memory Controller

- 16-Mbyte Address Space per Chip Select
- 8- bit Data Bus
- Word, Halfword, Byte Transfers
- Programmable Setup, Pulse And Hold Time for Read Signals per Chip Select
- Programmable Setup, Pulse And Hold Time for Write Signals per Chip Select
- Programmable Data Float Time per Chip Select
- External Wait Request
- Automatic Switch to Slow Clock Mode
- Asynchronous Read in Page Mode Supported: Page Size Ranges from 4 to 32 Bytes
- NAND FLASH additional logic supporting NAND Flash with Multiplexed Data/Address buses
- Hardware Configurable number of chip select from 1 to 4
- Programmable timing on a per chip select basis

Symbol		Millimeter		Inch			
Symbol	Min	Nom	Max	Min	Nom	Max	
A	_	-	1.60	_	-	0.063	
A1	0.05	-	0.15	0.002	-	0.006	
A2	1.35	1.40	1.45	0.053	0.055	0.057	
D	12.00 BSC 0.472 BSC						
D1		10.00 BSC			0.383 BSC		
E		12.00 BSC			0.472 BSC		
E1		10.00 BSC			0.383 BSC		
R2	0.08	-	0.20	0.003	-	0.008	
R1	0.08	-	-	0.003	-	-	
q	0°	3.5°	7 °	0°	3.5°	7 °	
θ1	0°	-	-	0°	-	-	
θ2	11°	12°	13°	11°	12°	13°	
θ3	11°	12°	13°	11°	12°	13°	
С	0.09	_	0.20	0.004	-	0.008	
L	0.45	0.60	0.75	0.018	0.024	0.030	
L1		1.00 REF		0.039 REF			
S	0.20	-	-	0.008	-	-	
b	0.17	0.20	0.27	0.007	0.008	0.011	
е		0.50 BSC.			0.020 BSC.		
D2		7.50			0.285		
E2	7.50			0.285			
	Tolerances of Form and Position						
aaa	0.20				0.008		
bbb	0.20			0.008			
ccc		0.08			0.003		
ddd		0.08		0.003			

Table 13-2. 64-lead LQFP Package Dimensions (in mm)

Symbol	Millimeter			Inch		
Symbol	Min	Nom	Max	Min	Nom	Max
А	_	_	090	_	_	0.035
A1	_	-	0.050	_	_	0.002
A2	_	0.65	0.70	_	0.026	0.028
A3		0.20 REF			0.008 REF	
b	0.18	0.20	0.23	0.007	0.008	0.009
D		7.00 bsc		0.276 bsc		
D2	5.45	5.60	5.75	0.215	0.220	0.226
E		7.00 bsc		0.276 bsc		
E2	5.45	5.60	5.75	0.215	0.220	0.226
L	0.35	0.40	0.45	0.014	0.016	0.018
е		0.50 bsc			0.020 bsc	
R	0.09	-	-	0.004	-	_
Tolerances of Form and Position						
aaa	0.10				0.004	
bbb	0.10			0.004		
ссс		0.05		0.002		

Table 13-3. 48-pad QFN Package Dimensions (in mm)

Doc. Rev	Comments	Change Request Ref.
	Section 1. "Features" updated, "Low Power Modes" , Sleep and Backup modes, down to 1.8 μA in Backup mode	rfo
6500ES	Figure 8-1, "SAM3S Product Mapping", SRAM associated 1 MByte bit band region mapping changed: 0x22000000 to 0x23FFFFFF.	
	Document format updated, subsequently pagination changed	
	Section 14. "Ordering Information" Introduced MRL B for SAM3S1 parts	8545
	Replace all mention to 100-ball LFBGA into 100-ball TFBGA.	8044
	Add table note 5 in Table 3-1, "Signal Description List".	7632
	Add MOSCRCEN bit details in Section 5.5.2 "Wait Mode".	7639
	Section 9.1.3.9 "Fast Flash Programming Interface" updated.	7668-7901
	Notes under Figure 5-1, "Single Supply" and Figure 5-2, "Core Externally Supplied" modified.	7887
6500DS	Cross-References (1) added for 64-pin packages in table Table 1-1, "Configuration Summary".	8033
	Pin 22 value changed for PA23/PGMD11 in Table 4-1, "100-lead LQFP SAM3S4/2/1C Pinout".	8093
	"High Frequency Asynchronous clocking mode" removed from Section 12.7 "Pulse Width Modulation Controller (PWM)"	8095
	"Write Protected Registers" added in "Description", in Peripherals list.	8213
	ADC column values updated in Table 1-1, "Configuration Summary".	rfo
	Missing PGMD8 to 15 added to Table 4-1, "100-lead LQFP SAM3S4/2/1C Pinout" and Table 4-2, "100-ball TFBGA SAM3S4/2/1C Pinout".	rfo
	Section 5.7 "Fast Startup" updated.	
	Typo fixed on back page: 'techincal'> 'technical'.	7536
	Typos fixed in Section 1. "Features".	7524
6500CS	Missing title added to Table 14-1.	
	PLLA input frequency range updated in Section 10.5 "Clock Generator".	7494
	A sentence completed in Section 5.5.2 "Wait Mode".	7492
	Last sentence removed from Section 9.1.3.10 "SAM-BA [®] Boot".	7428
	'three GPNVM bits' replaced by 'two GPNVM bits' in Section 9.1.3.11 "GPNVM Bits".	
	Leftover sentence removed from Section 4.1 "SAM3S4/2/1C Package and Pinout".	7394
	"Packages" on page 2, package size or pitch updated.	
	Table 1-1, "Configuration Summary", ADC column updated, footnote gives precision on reserved	7214
	channel.	6981
	Table 4-2, "100-ball TFBGA SAM3S4/2/1C Pinout", pinout information is available.	7201
6500BS	Figure 5-1, "Single Supply", Figure 5-2, "Core Externally Supplied", updated notes below figures.	7243/rfo
	Figure 5-2, "Core Externally Supplied", Figure 5-3, "Backup Battery", ADC, DAC, Analog Comparator supply is 2.0V-3.6V.	
	Section 12.13 "Analog Comparator", "Peripherals" on page 2, reference to "window function" removed.	7103
	Section 9.1.3.8 "Unique Identifier", Each device integrates its own 128-bit unique identifier.	7307
6500AS	First issue	