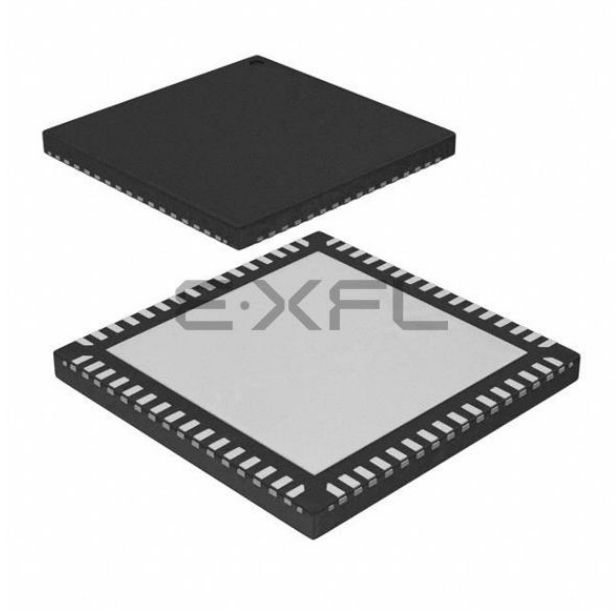

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What is "Embedded - Microcontrollers"?

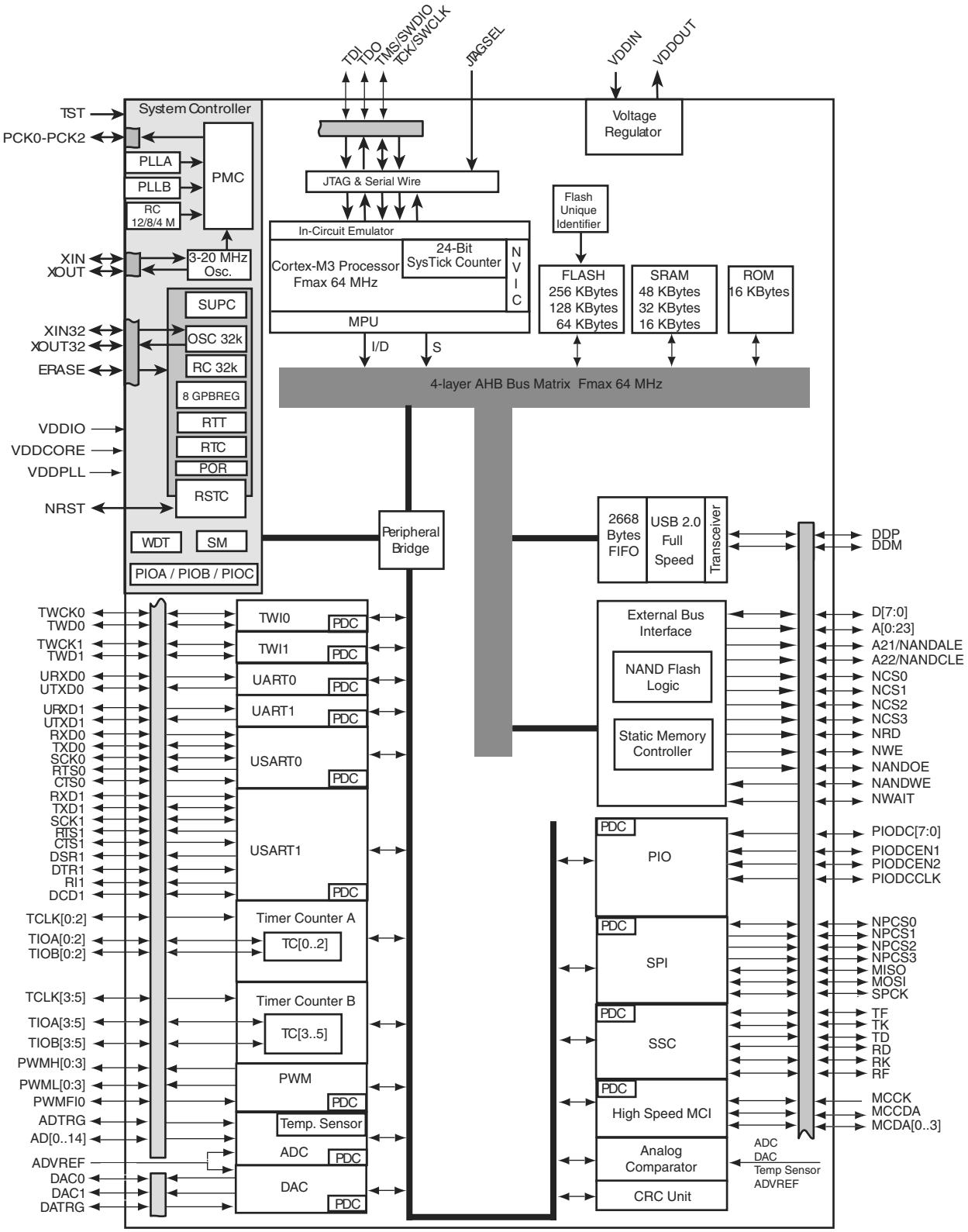
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	I²C, MMC, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	47
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x10/12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3s1bb-mur

2. SAM3S Block Diagram

Figure 2-1. SAM3S 100-pin Version Block Diagram



4.2 SAM3S4/2/1B Package and Pinout

Figure 4-3. Orientation of the 64-pad QFN Package

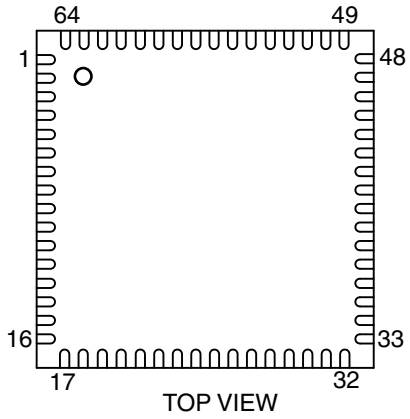


Figure 4-4. Orientation of the 64-lead LQFP Package

64

1

4.3 SAM3S4/2/1A Package and Pinout

Figure 4-5. Orientation of the 48-pad QFN Package

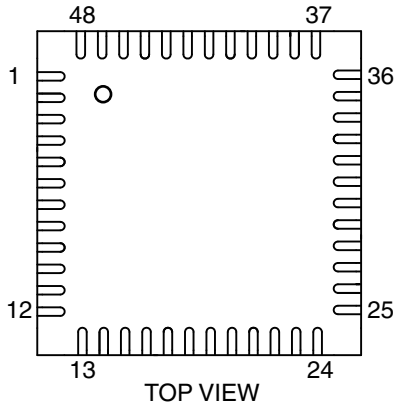


Figure 4-6. Orientation of the 48-lead LQFP Package

48

1

4.3.1 48-Lead LQFP and QFN Pinout

Table 4-4. 48-pin SAM3S4/2/1A Pinout

1	ADVREF	13	VDDIO	25	TDI/PB4	37	TDO/TRACESWO/ PB5
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	PB0/AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS/SWDIO/PB6
4	PB1/AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK/SWCLK/PB7
5	PB2/AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	PB3/AD7	18	VDDCORE	30	TST	42	ERASE/PB12
7	VDDIN	19	PA12/PGMD0	31	PA3	43	DDM/PB10
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	DDP/PB11
9	PA17/PGMD5/ AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT/PB8
10	PA18/PGMD6/ AD1	22	PA9/PGMM1	34	GND	46	XIN/PB9/PGMCK
11	PA19/PGMD7/ AD2	23	PA8/*XOUT32*/ PGMM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/*XIN32*/ PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

5. Power Considerations

5.1 Power Supplies

The SAM3S product has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals; voltage ranges from 1.62V and 1.95V.
- VDDIO pins: Power the Peripherals I/O lines (Input/Output Buffers); USB transceiver; Backup part, 32kHz crystal oscillator and oscillator pads; ranges from 1.62V and 3.6V
- VDDIN pin: Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply; Voltage ranges from 1.8V to 3.6V
- VDDPLL pin: Powers the PLLA, PLLB, the Fast RC and the 3 to 20 MHz oscillator; voltage ranges from 1.62V and 1.95V.

5.2 Voltage Regulator

The SAM3S embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3S. It features two different operating modes:

- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 µA.

• In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is inferior to 100 µs.

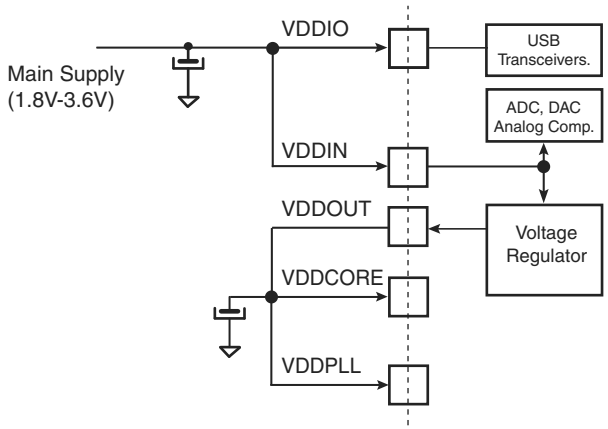
For adequate input and output power supply decoupling/bypassing, refer to the Voltage Regulator section in the Electrical Characteristics section of the datasheet.

5.3 Typical Powering Schematics

The SAM3S supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-1 shows the power schematics.

As VDDIN powers the voltage regulator, the ADC/DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that it is different from Backup mode).

Figure 5-1. Single Supply



Note: For USB, VDDIO needs to be greater than 3.0V.
For ADC, VDDIN needs to be greater than 2.0V.
For DAC, VDDIN needs to be greater than 2.4V.

5.7 Fast Startup

The device allows the processor to restart in a few microseconds while the processor is in wait mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + SM + RTC + RTT).

The fast restart circuitry, as shown in Figure 5-5, is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4/8/12 MHz fast RC oscillator, switches the master clock on this 4MHz clock and reenables the processor clock.

Figure 5-5. Fast Start-Up Circuitry

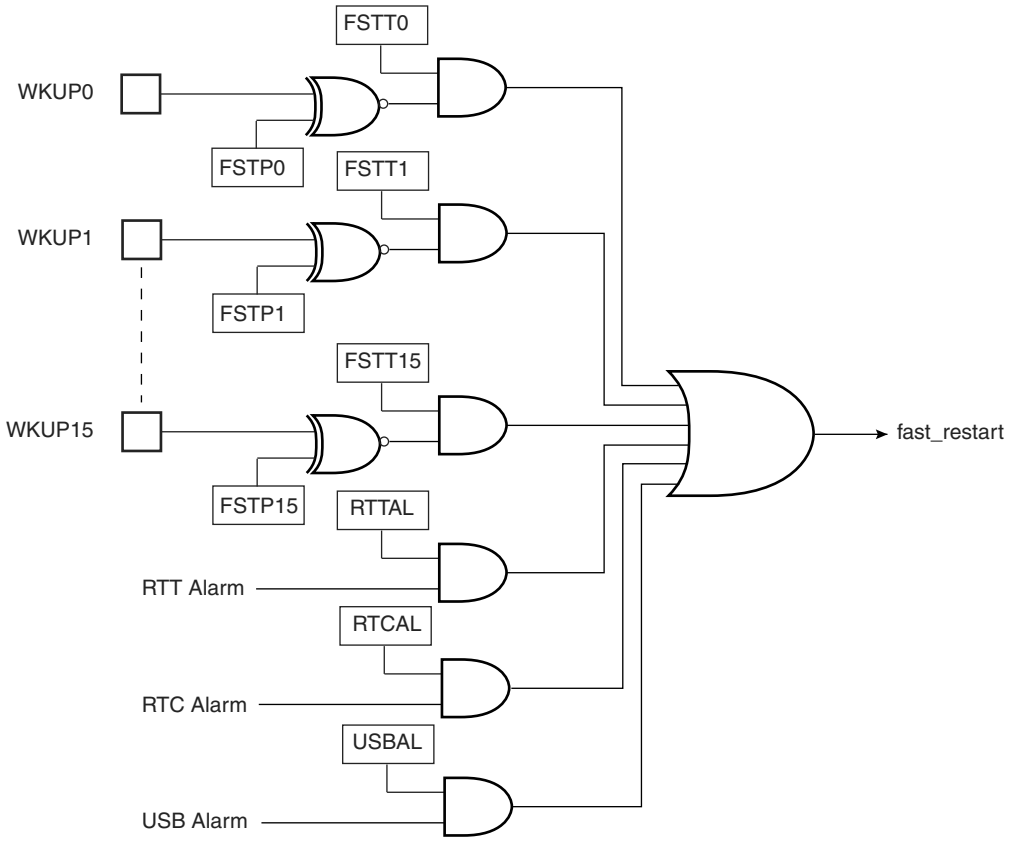


Table 6-1. System I/O Configuration List

SYSTEM_IO bit number	Default function after reset	Other function	Constraints for normal start	Configuration
12	ERASE	PB12	Low Level at startup(1)	In Matrix User Interface Registers (Refer to the SystemIO Configuration Register in the Bus Matrix section of the product datasheet.)
10	DDM	PB10	-	
11	DDP	PB11	-	
7	TCK/SWCLK	PB7	-	
6	TMS/SWDIO	PB6	-	
5	TDO/TRACESWO	PB5	-	
4	TDI	PB4	-	
-	PA7	XIN32	-	See footnote (2) below
-	PA8	XOUT32	-	
-	PB9	XIN	-	See footnote (3) below
-	PB8	XOUT	-	

Notes: 1. If PB12 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PB12 into PIO mode,

2. In the product Datasheet Refer to: Slow Clock Generator of the Supply Controller section.

3. In the product Datasheet Refer to: 3 to 20 MHZ Crystal Oscillator information in PMC section.

6.2.1 Serial Wire JTAG Debug Port (SWJ-DP) Pins

The SWJ-DP pins are TCK/SWCLK, TMS/SWDIO, TDO/SWO, TDI and commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage reference and reset state, refer to Table 3-1 on page 7.

At startup, SWJ-DP pins are configured in SWJ-DP mode to allow connection with debugging probe. Please refer to the Debug and Test Section of the product datasheet.

SWJ-DP pins can be used as standard I/Os to provide users more general input/output pins when the debug port is not needed in the end application. Mode selection between SWJ-DP mode (System IO mode) and general IO mode is performed through the AHB Matrix Special Function Registers (MATRIX_SFR). Configuration of the pad for pull-up, triggers, debouncing and glitch filters is possible regardless of the mode.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

By default, the JTAG Debug Port is active. If the debugger host wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables the JTAG-DP and enables the SW-DP. When the Serial Wire Debug Port is active, TDO/TRACESWO can be used for trace.

The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchronous trace can only be used with SW-DP, not JTAG-DP. For more information about SW-DP and JTAG-DP switching, please refer to the Debug and Test Section.

6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM3S series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the Fast Flash Programming Interface (FFPI) section. For more on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

7.5 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the Cortex-M3 S Bus to the Internal ROM. Thus, these paths are forbidden or simply not wired and shown as “-” in the following table.

Table 7-3. SAM3S Master to Slave Access

Slaves	Masters	0	1	2	3
		Cortex-M3 I/D Bus	Cortex-M3 S Bus	PDC	CRCCU
0	Internal SRAM	-	X	X	X
1	Internal ROM	X	-	X	X
2	Internal Flash	X	-	-	X
3	External Bus Interface	-	X	X	X
4	Peripheral Bridge	-	X	X	-

7.6 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Low bus arbitration overhead
  - One Master Clock cycle needed for a transfer from memory to peripheral
  - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirement

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Table 7-4. Peripheral DMA Controller

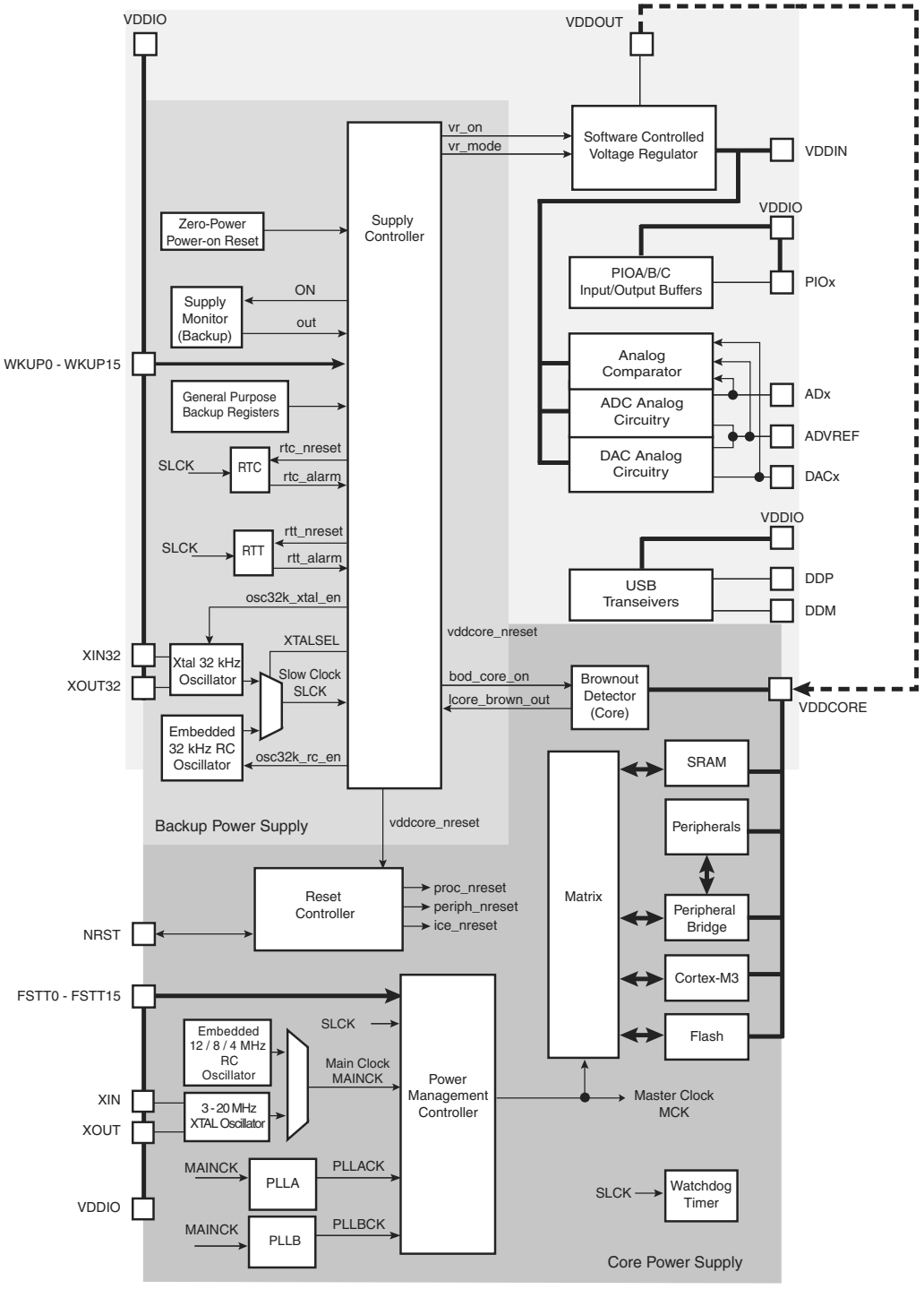
Instance Name	Channel T/R	100 & 64 Pins	48 Pins
PWM	Transmit	x	x
TWI1	Transmit	x	x
TWI0	Transmit	x	x
UART1	Transmit	x	x
UART0	Transmit	x	x
USART1	Transmit	x	N/A
USART0	Transmit	x	x
DAC	Transmit	x	N/A
SPI	Transmit	x	x
SSC	Transmit	x	x
HSMCI	Transmit	x	N/A
PIOA	Transmit	x	x
TWI1	Receive	x	x
TWI0	Receive	x	x
UART1	Receive	x	N/A
UART0	Receive	x	x

10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc...

See the system controller block diagram in Figure 10-1 on page 34.

Figure 10-1. System Controller Block Diagram



FSTT0 - FSTT15 are possible Fast Startup Sources, generated by WKUP0-WKUP15 Pins, but are not physical pins.

10.1 System Controller and Peripheral Mapping

Please refer to Section 8-1 “SAM3S Product Mapping” on page 30.

All the peripherals are in the bit band region and are mapped in the bit band alias region.

10.2 Power-on-Reset, Brownout and Supply Monitor

The SAM3S embeds three features to monitor, warn and/or reset the chip:

• Power-on-Reset on VDDIO

• Brownout Detector on VDDCORE

• Supply Monitor on VDDIO

10.2.1 Power-on-Reset

The Power-on-Reset monitors VDDIO. It is always activated and monitors voltage at start up but also during power down. If VDDIO goes below the threshold voltage, the entire chip is reset. For more information, refer to the Electrical Characteristics section of the datasheet.

10.2.2 Brownout Detector on VDDCORE

The Brownout Detector monitors VDDCORE. It is active by default. It can be deactivated by software through the Supply Controller (SUPC_MR). It is especially recommended to disable it during low-power modes such as wait or sleep modes.

If VDDCORE goes below the threshold voltage, the reset of the core is asserted. For more information, refer to the Supply Controller (SUPC) and Electrical Characteristics sections of the datasheet.

10.2.3 Supply Monitor on VDDIO

The Supply Monitor monitors VDDIO. It is not active by default. It can be activated by software and is fully programmable with 16 steps for the threshold (between 1.9V to 3.4V). It is controlled by the Supply Controller (SUPC). A sample mode is possible. It allows to divide the supply monitor power consumption by a factor of up to 2048. For more information, refer to the SUPC and Electrical Characteristics sections of the datasheet.

10.3 Reset Controller

The Reset Controller is based on a Power-on-Reset cell, and a Supply Monitor on VDDCORE.

The Reset Controller is capable to return to the software the source of the last reset, either a general reset, a wake-up reset, a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin input/output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

The configuration of the Reset Controller is saved as supplied on VDDIO.

10.4 Supply Controller (SUPC)

The Supply Controller controls the power supplies of each section of the processor and the peripherals (via Voltage regulator control)

The Supply Controller has its own reset circuitry and is clocked by the 32 kHz Slow clock generator.

The reset circuitry is based on a zero-power power-on reset cell and a brownout detector cell. The zero-power power-on reset allows the Supply Controller to start properly, while the software-programmable brownout detector allows detection of either a battery discharge or main voltage loss.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

The Supply Controller starts up the device by sequentially enabling the internal power switches and the Voltage Regulator, then it generates the proper reset signals to the core power supply.

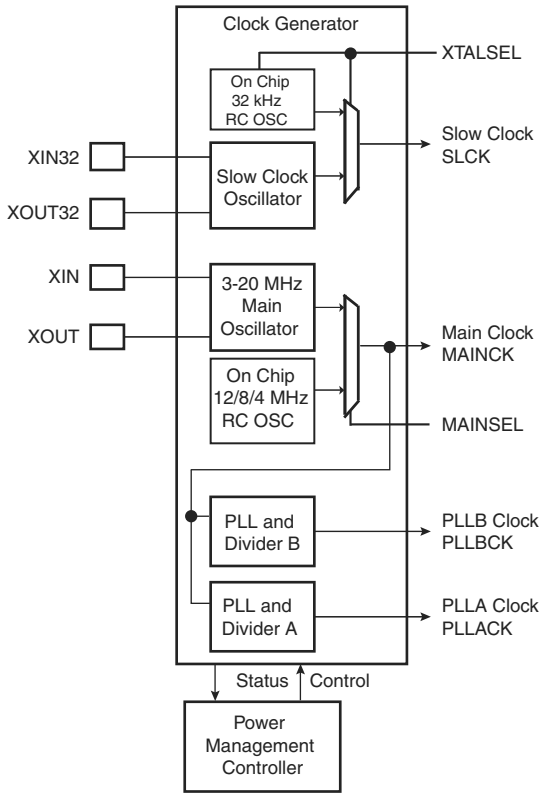
It also enables to set the system in different low power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low Power 32768Hz Slow Clock oscillator with bypass mode
- One Low-Power RC oscillator
- One 3-20 MHz Crystal Oscillator, which can be bypassed
- One Fast RC oscillator factory programmed, 3 output frequencies can be selected: 4, 8 or 12 MHz. By default 4 MHz is selected.
- One 60 to 130 MHz PLL (PLLB) providing a clock for the USB Full Speed Controller
- One 60 to 130 MHz programmable PLL (PLLA), capable to provide the clock MCK to the processor and to the peripherals. The PLLA input frequency is from 3.5 to 20 MHz.

Figure 10-2. Clock Generator Block Diagram



10.6 Power Management Controller

The Power Management Controller provides all the clock signals to the system. It provides:

- the Processor Clock, HCLK
- the Free running processor clock, FCLK
- the Cortex SysTick external clock
- the Master Clock, MCK, in particular to the Matrix and the memory interfaces
- the USB Clock, UDPCK

10.14 UART

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

10.15 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB and PIOC (100-pin version only) controlling a maximum of 79 I/O Lines
- Fully programmable through Set/Clear Registers

Table 10-2. PIO available according to pin count

Version	48 pin	64 pin	100 pin
PIOA	21	32	32
PIOB	13	15	15
PIOC	-	-	32

- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change, rising edge, falling edge, low level and level interrupt
  - Debouncing and Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up or pull-down on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

11.2.2 PIO Controller B Multiplexing

Table 11-3. Multiplexing on PIO Controller B (PIOB)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PB0	PWMH0			AD4		
PB1	PWMH1			AD5		
PB2	URXD1	NPCS2		AD6/ WKUP12		
PB3	UTXD1	PCK2		AD7		
PB4	TWD1	PWMH2			TDI	
PB5	TWCK1	PWML0		WKUP13	TDO/TRACESWO	
PB6					TMS/SWDIO	
PB7					TCK/SWCLK	
PB8					XOUT	
PB9					XIN	
PB10					DDM	
PB11					DDP	
PB12	PWML1				ERASE	
PB13	PWML2	PCK0		DAC0		64/100-pin versions
PB14	NPCS1	PWMH3		DAC1		64/100-pin versions

12. Embedded Peripherals Overview

12.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

12.2 Two Wire Interface (TWI)

- Master, Multi-Master and Slave Mode Operation
- Compatibility with Atmel two-wire interface, serial memory and I^2C compatible devices
- One, two or three bytes for slave address
- Sequential read/write operations
- Bit Rate: Up to 400 kbit/s
- General Call Supported in Slave Mode
- Connecting to PDC channel capabilities optimizes data transfers in Master Mode only
  - One channel for the receiver, one channel for the transmitter
  - Next buffer support

12.3 Universal Asynchronous Receiver Transceiver (UART)

- Two-pin UART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

12.4 Universal Synchronous Asynchronous Receiver Transceiver (USART)

- Programmable Baud Rate Generator with Fractional Baud rate support
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection

12.7 Pulse Width Modulation Controller (PWM)

- One Four-channel 16-bit PWM Controller, 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock Selection
  - Independent Period and Duty Cycle, with Double Buffering
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform
  - Independent Output Override for each channel
  - Independent complementary Outputs with 12-bit dead time generator for each channel
  - Independent Enable Disable Commands
  - Independent Clock Selection
  - Independent Period and Duty Cycle, with Double Buffering
- Synchronous Channel mode
  - Synchronous Channels share the same counter
  - Mode to update the synchronous channels registers after a programmable number of periods
- Connection to one PDC channel
  - Offers Buffer transfer without Processor Intervention, to update duty cycle of synchronous channels
- independent event lines which can send up to 4 triggers on ADC within a period
- Programmable Fault Input providing an asynchronous protection of outputs
- Stepper motor control (2 Channels)

12.8 High Speed Multimedia Card Interface (HSMCI)

- 4-bit or 1-bit Interface
- Compatibility with MultiMedia Card Specification Version 4.3
- Compatibility with SD and SDHC Memory Card Specification Version 2.0
- Compatibility with SDIO Specification Version V1.1.
- Compatibility with CE-ATA Specification 1.1
- Cards clock rate up to Master Clock divided by 2
- Boot Operation Mode support
- High Speed mode support
- Embedded power management to slow down clock rate when not used
- HSMCI has one slot supporting
  - One MultiMediaCard bus (up to 30 cards) or
  - One SD Memory Card
  - One SDIO Card
- Support for stream, block and multi-block data read and write

12.9 USB Device Port (UDP)

- USB V2.0 full-speed compliant,12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 2688-byte dual-port RAM for endpoints

12.13 Analog Comparator

- One analog comparator
- High speed option vs. low power option
- Selectable input hysteresis:
  - 0, 20 mV, 50 mV
- Minus input selection:
  - DAC outputs
  - Temperature Sensor
  - ADVREF
  - AD0 to AD3 ADC channels
- Plus input selection:
  - All analog inputs
- output selection:
  - Internal signal
  - external pin
  - selectable inverter
- Interrupt on:
  - Rising edge, Falling edge, toggle

12.14 Cyclic Redundancy Check Calculation Unit (CRCCU)

- 32-bit cyclic redundancy check automatic calculation
- CRC calculation between two addresses of the memory

Table 13-2. 64-lead LQFP Package Dimensions (in mm)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.383 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.383 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

14. Ordering Information

Table 14-1. Ordering Codes for SAM3S Series Devices

Ordering Code	MRL A	MRL B	Flash (Kbytes)	Package (Kbytes)	Package Type	Temperature Operating Range
ATSAM3S4CA-AU	A	–	256	QFP100	Green	Industrial -40°C to 85°C
ATSAM3S4CA-CU	A	–	256	BGA100	Green	Industrial -40°C to 85°C
ATSAM3S4BA-AU	A	–	256	QFP64	Green	Industrial -40°C to 85°C
ATSAM3S4BA-MU	A	–	256	QFN64	Green	Industrial -40°C to 85°C
ATSAM3S4AA-AU	A	–	256	QFP48	Green	Industrial -40°C to 85°C
ATSAM3S4AA-MU	A	–	256	QFN48	Green	Industrial -40°C to 85°C
ATSAM3S2CA-AU	A	–	128	QFP100	Green	Industrial -40°C to 85°C
ATSAM3S2CA-CU	A	–	128	BGA100	Green	Industrial -40°C to 85°C
ATSAM3S2BA-AU	A	–	128	QFP64	Green	Industrial -40°C to 85°C
ATSAM3S2BA-MU	A	–	128	QFN64	Green	Industrial -40°C to 85°C
ATSAM3S2AA-AU	A	–	128	QFP48	Green	Industrial -40°C to 85°C
ATSAM3S2AA-MU	A	–	128	QFN48	Green	Industrial -40°C to 85°C
ATSAM3S1CA-AU	A	–	64	QFP100	Green	Industrial -40°C to 85°C
ATSAM3S1CA-CU	A	–	64	BGA100	Green	Industrial -40°C to 85°C
ATSAM3S1BA-AU	A	–	64	QFP64	Green	Industrial -40°C to 85°C
ATSAM3S1BA-MU	A	–	64	QFN64	Green	Industrial -40°C to 85°C
ATSAM3S1AA-AU	A	–	64	QFP48	Green	Industrial -40°C to 85°C
ATSAM3S1AA-MU	A	–	64	QFN48	Green	Industrial -40°C to 85°C
ATSAM3S1CB-AU	–	B	64	QFP100	Green	Industrial -40°C to 85°C
ATSAM3S1CB-CU	–	B	64	BGA100	Green	Industrial -40°C to 85°C
ATSAM3S1BB-AU	–	B	64	QFP64	Green	Industrial -40°C to 85°C
ATSAM3S1BB-MU	–	B	64	QFN64	Green	Industrial -40°C to 85°C
ATSAM3S1AB-AU	–	B	64	QFP48	Green	Industrial -40°C to 85°C
ATSAM3S1AB-MU	–	B	64	QFN48	Green	Industrial -40°C to 85°C

Revision History

Doc. Rev	Comments	Change Request Ref.
6500ES	Section 1. “Features”updated, “Low Power Modes” , Sleep and Backup modes, down to 1.8 µA in Backup mode	rfo
	Figure 8-1, "SAM3S Product Mapping", SRAM associated 1 MByte bit band region mapping changed: 0x22000000 to 0x23FFFFFF.	
	Document format updated, subsequently pagination changed	
	Section 14. “Ordering Information” Introduced MRL B for SAM3S1 parts..	8545
6500DS	Replace all mention to 100-ball LFBGA into 100-ball TFBGA.	8044
	Add table note 5 in Table 3-1, “Signal Description List”.	7632
	Add MOSCRCEN bit details in Section 5.5.2 “Wait Mode”.	7639
	Section 9.1.3.9 “Fast Flash Programming Interface” updated.	7668-7901
	Notes under Figure 5-1, "Single Supply" and Figure 5-2, "Core Externally Supplied" modified.	7887
	Cross-References (1) added for 64-pin packages in table Table 1-1, “Configuration Summary”.	8033
	Pin 22 value changed for PA23/PGMD11 in Table 4-1, “100-lead LQFP SAM3S4/2/1C Pinout”.	8093
	"High Frequency Asynchronous clocking mode" removed from Section 12.7 “Pulse Width Modulation Controller (PWM)”	8095
	“Write Protected Registers” added in “Description” , in Peripherals list.	8213
	ADC column values updated in Table 1-1, “Configuration Summary”.	rfo
6500CS	Missing PGMD8 to 15 added to Table 4-1, “100-lead LQFP SAM3S4/2/1C Pinout” and Table 4-2, “100-ball TFBGA SAM3S4/2/1C Pinout”.	rfo
	Section 5.7 “Fast Startup” updated.	
	Typo fixed on back page: ‘techincal’ --> ‘technical’.	7536
	Typos fixed in Section 1. “Features”.	7524
	Missing title added to Table 14-1.	
	PLLA input frequency range updated in Section 10.5 “Clock Generator”.	7494
	A sentence completed in Section 5.5.2 “Wait Mode”.	7492
	Last sentence removed from Section 9.1.3.10 “SAM-BA® Boot”.	7428
	‘three GPNVM bits’ replaced by ‘two GPNVM bits’ in Section 9.1.3.11 “GPNVM Bits”.	
	Leftover sentence removed from Section 4.1 “SAM3S4/2/1C Package and Pinout”.	7394
6500BS	“Packages” on page 2, package size or pitch updated.	
	Table 1-1, “Configuration Summary”, ADC column updated, footnote gives precision on reserved channel.	7214
	Table 4-2, “100-ball TFBGA SAM3S4/2/1C Pinout”, pinout information is available.	6981
	Figure 5-1, "Single Supply",Figure 5-2, "Core Externally Supplied" , updated notes below figures.	7201
	Figure 5-2, "Core Externally Supplied", Figure 5-3, "Backup Battery", ADC, DAC, Analog Comparator supply is 2.0V-3.6V.	7243/rfo
	Section 12.13 “Analog Comparator”, “Peripherals” on page 2, reference to “window function” removed.	7103
	Section 9.1.3.8 “Unique Identifier”, Each device integrates its own 128-bit unique identifier.	7307
6500AS	First issue	

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