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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	EBI/EMI, I²C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	79
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 15x10/12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3s1cb-aur

1. Features

- **Core**
  - **ARM® Cortex®-M3 revision 2.0 running at up to 64 MHz**
  - **Memory Protection Unit (MPU)**
  - **Thumb®-2 instruction set**
- **Pin-to-pin compatible with AT91SAM7S series (48- and 64-pin versions)**
- **Memories**
  - **From 64 to 256 Kbytes embedded Flash, 128-bit wide access, memory accelerator, single plane**
  - **From 16 to 48 Kbytes embedded SRAM**
  - **16 Kbytes ROM with embedded bootloader routines (UART, USB) and IAP routines**
  - **8-bit Static Memory Controller (SMC): SRAM, PSRAM, NOR and NAND Flash support**
  - **Memory Protection Unit (MPU)**
- **System**
  - **Embedded voltage regulator for single supply operation**
  - **Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe operation**
  - **Quartz or ceramic resonator oscillators: 3 to 20 MHz main power with Failure Detection and optional low power 32.768 kHz for RTC or device clock**
  - **High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz default frequency for device startup. In-application trimming access for frequency adjustment**
  - **Slow Clock Internal RC oscillator as permanent low-power mode device clock**
  - **Two PLLs up to 130 MHz for device clock and for USB**
  - **Temperature Sensor**
  - **Up to 22 peripheral DMA (PDC) channels**
- **Low Power Modes**
  - **Sleep and Backup modes, down to 1.8 µA in Backup mode**
  - **Ultra low power RTC**
- **Peripherals**
  - **USB 2.0 Device: 12 Mbps, 2668 byte FIFO, up to 8 bidirectional Endpoints. On-Chip Transceiver**
  - **Up to 2 USARTs with ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Mode**
  - **Two 2-wire UARTs**
  - **Up to 2 Two Wire Interface (I2C compatible), 1 SPI, 1 Serial Synchronous Controller (I2S), 1 High Speed Multimedia Card Interface (SDIO/SD Card/MMC)**
  - **Up to 6 Three-Channel 16-bit Timer/Counter with capture, waveform, compare and PWM mode. Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor**
  - **4-channel 16-bit PWM with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter for Motor Control**
  - **32-bit Real-time Timer and RTC with calendar and alarm features**
  - **Up to 15-channel, 1Msps ADC with differential input mode and programmable gain stage**
  - **One 2-channel 12-bit 1Msps DAC**
  - **One Analog Comparator with flexible input selection, Selectable input hysteresis**
  - **32-bit Cyclic Redundancy Check Calculation Unit (CRCCU)**
  - **Write Protected Registers**
- **I/O**
  - **Up to 79 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination**
  - **Three 32-bit Parallel Input/Output Controllers, Peripheral DMA assisted Parallel Capture Mode**
- **Packages**
  - **100-lead LQFP, 14 x 14 mm, pitch 0.5 mm/100-ball TFBGA, 9 x 9 mm, pitch 0.8 mm**
  - **64-lead LQFP, 10 x 10 mm, pitch 0.5 mm/64-pad QFN 9x9 mm, pitch 0.5 mm**
  - **48-lead LQFP, 7 x 7 mm, pitch 0.5 mm/48-pad QFN 7x7 mm, pitch 0.5 mm**

1.1 Configuration Summary

The SAM3S microcontrollers differ in memory size, package and features list. Table 1-1 below summarizes the configurations of the device family

Table 1-1. Configuration Summary

Device	Flash	SRAM	Timer Counter Channels	GPIOs	UART/ USARTs	ADC	12-bit DAC Output	External Bus Interface	HSMCI	Package
SAM3S4C	256 Kbytes single plane	48 Kbytes	6	79	2/2[1]	15 ch.	2	8-bit data, 4 chip selects, 24-bit address	1 port 4 bits	LQFP100 BGA100
SAM3S4B	256 Kbytes single plane	48 Kbytes	3	47	2/2[1]	10 ch.	2	-	1 port 4 bits	LQFP64 QFN 64
SAM3S4A	256 Kbytes single plane	48 Kbytes	3	34	2/1	8 ch.	-	-	-	LQFP48 QFN 48
SAM3S2C	128 Kbytes single plane	32 Kbytes	6	79	2/2[1]	15 ch.	2	8-bit data, 4 chip selects, 24-bit address	1 port 4 bits	LQFP100 BGA100
SAM3S2B	128 Kbytes single plane	32 Kbytes	3	47	2/2[1]	10 ch.	2	-	1 port 4 bits	LQFP64 QFN 64
SAM3S2A	128 Kbytes single plane	32 Kbytes	3	34	2/1	8 ch.	-	-	-	LQFP48 QFN 48
SAM3S1C	64 Kbytes single plane	16 Kbytes	6	79	2/2[1]	15 ch.	2	8-bit data, 4 chip selects, 24-bit address	1 port 4 bits	LQFP100 BGA100
SAM3S1B	64 Kbytes single plane	16 Kbytes	3	47	2/2[1]	10 ch.	2	-	1 port 4 bits	LQFP64 QFN 64
SAM3S1A	64 Kbytes single plane	16 Kbytes	3	34	2/1	8 ch.	-	-	-	LQFP48 QFN 48

Note: 1. Full Modem support on USART1.

2. SAM3S Block Diagram

Figure 2-1. SAM3S 100-pin Version Block Diagram

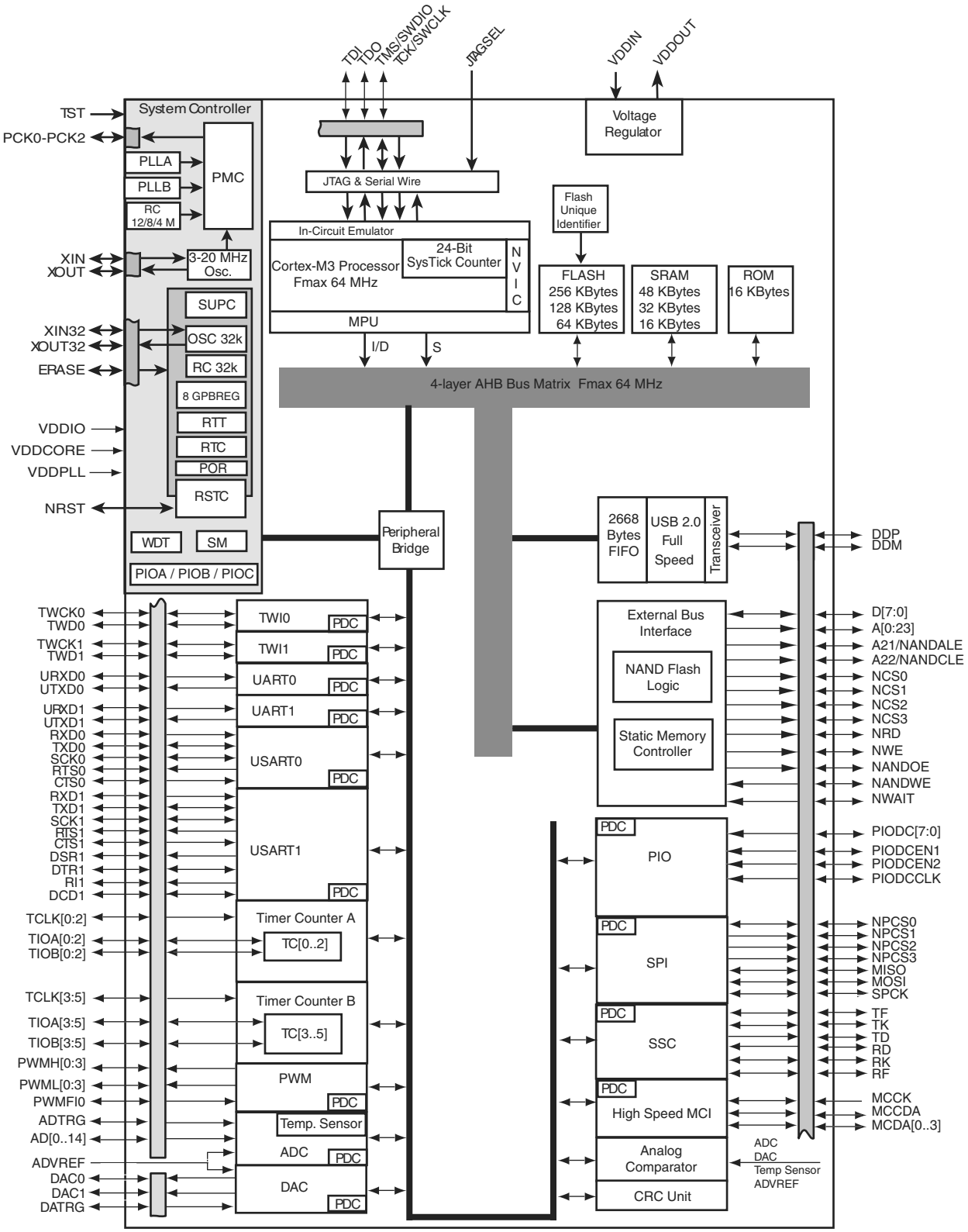


Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output			
RD	SSC Receive Data	Input			
TK	SSC Transmit Clock	I/O			
RK	SSC Receive Clock	I/O			
TF	SSC Transmit Frame Sync	I/O			
RF	SSC Receive Frame Sync	I/O			
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller- PWMC					
PWMHx	PWM Waveform Output High for channel x	Output			
PWMLx	PWM Waveform Output Low for channel x	Output			only output in complementary mode when dead time insertion is enabled
PWMFI0	**PWM Fault Input**	Input			
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
SPI_NPCS1 - SPI_NPCS3	SPI Peripheral Chip Select	Output	Low		
Two-Wire Interface- TWI					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
Analog					
ADVREF	ADC, DAC and Analog Comparator Reference	Analog			
Analog-to-Digital Converter - ADC					
AD0 - AD14	Analog Inputs	Analog, Digital			
ADTRG	ADC Trigger	Input		VDDIO	
12-bit Digital-to-Analog Converter - DAC					
DAC0 - DAC1	Analog output	Analog, Digital			
DACTRG	DAC Trigger	Input		VDDIO	

4.1.3 100-Lead LQFP Pinout

Table 4-1. 100-lead LQFP SAM3S4/2/1C Pinout

1	ADVREF	26	GND	51	TDI/PB4	76	TDO/TRACESWO/PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27/PGMD15	82	PC20
8	PC31	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24/PGMD12	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25/PGMD13	63	PA29	88	DDM/PB10
14	PA18/PGMD6/AD1	39	PA26/PGMD14	64	PA30	89	DDP/PB11
15	PA21/PGMD9/AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/AD2	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/PGMD10/AD9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23/PGMD11	47	PC1	72	PA1/PGMEN1	97	PB9/*PGMCK/XIN*
23	PC12/AD12	48	PA8/XOUT32/ PGMM0	73	PC16	98	VDDIO
24	PA20/PGMD8/AD3	49	PA7/XIN32/ PGMNVALID	74	PA0/PGMEN0	99	PB14/DAC1
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

5. Power Considerations

5.1 Power Supplies

The SAM3S product has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals; voltage ranges from 1.62V and 1.95V.
- VDDIO pins: Power the Peripherals I/O lines (Input/Output Buffers); USB transceiver; Backup part, 32kHz crystal oscillator and oscillator pads; ranges from 1.62V and 3.6V
- VDDIN pin: Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply; Voltage ranges from 1.8V to 3.6V
- VDDPLL pin: Powers the PLLA, PLLB, the Fast RC and the 3 to 20 MHz oscillator; voltage ranges from 1.62V and 1.95V.

5.2 Voltage Regulator

The SAM3S embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3S. It features two different operating modes:

- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 µA.

• In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is inferior to 100 µs.

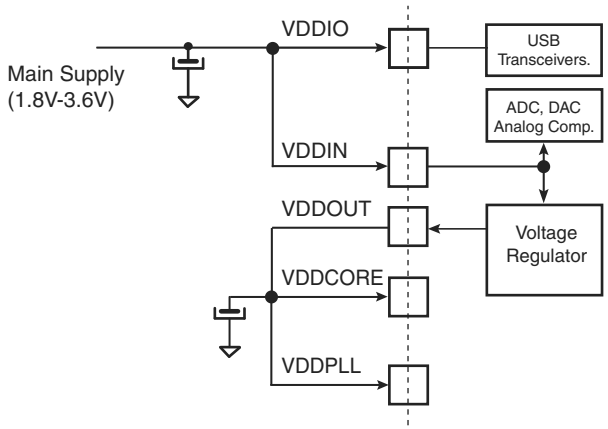
For adequate input and output power supply decoupling/bypassing, refer to the Voltage Regulator section in the Electrical Characteristics section of the datasheet.

5.3 Typical Powering Schematics

The SAM3S supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-1 shows the power schematics.

As VDDIN powers the voltage regulator, the ADC/DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that it is different from Backup mode).

Figure 5-1. Single Supply



Note: For USB, VDDIO needs to be greater than 3.0V.
For ADC, VDDIN needs to be greater than 2.0V.
For DAC, VDDIN needs to be greater than 2.4V.

5.4 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.5 Low Power Modes

The various low power modes of the SAM3S are described below:

5.5.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time (<0.1ms). Total current consumption is 3 µA typical.

The Supply Controller, zero-power power-on reset, RTT, RTC, Backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup mode is based on the Cortex-M3 deepsleep mode with the voltage regulator disabled.

The SAM3S can be awakened from this mode through WUP0-15 pins, the supply monitor (SM), the RTT or RTC wake-up event.

Backup mode is entered by using WFE instructions with the SLEEPDEEP bit in the System Control Register of the Cortex-M3 set to 1. (See the Power management description in The ARM Cortex M3 Processor section of the product datasheet).

Exit from Backup mode happens if one of the following enable wake up events occurs:

- WKUPEN0-15 pins (level transition, configurable debouncing)
- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current Consumption in Wait mode is typically 15 µA (total current consumption) if the internal voltage regulator is used or 8 µA if an external regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake-up the core (WFE). This is done by configuring the external lines WUP0-15 as fast startup wake-up pins (refer to Section 5.7 “Fast Startup”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Entering Wait Mode:

- Select the 4/8/12 MHz fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, Waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

The bit MOSCRCEN should be automatically set to '0'. So you have to add after this instruction the following: while (MOSCRCEN ==0); so that you are sure to stay in the loop until you awake from the wait mode. In that case you are sure the core will not continue to fetch the code but once you have exited the wait mode (in that case MOSCRCEN will be automatically set to '1').

5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.

The processor can be woke up from an interrupt if WFI instruction of the Cortex M3 is used, or from an event if the WFE instruction is used to enter this mode.

5.5.4 Low Power Mode Summary Table

The modes detailed above are the main low power modes. Each part can be set to on or off separately and wake up sources can be individually configured. Table 5-1 below shows a summary of the configurations of the low power modes.

Table 5-1. Low Power Mode Configuration Summary

Mode	SUPC, 32 kHz Oscillator RTC RTT Backup Registers, POR (Backup Region)	Regulator	Core Memory Peripherals	Mode Entry	Potential Wake Up Sources	Core at Wake Up	PIO State while in Low Power Mode	PIO State at Wake Up	Consumption (2) (3)	Wake-up Time(1)
Backup Mode	ON	OFF	OFF (Not powered)	WFE +SLEEPDEEP bit = 1	WUP0-15 pins SM alarm RTC alarm RTT alarm	Reset	Previous state saved	PIOA & PIOB & PIOC Inputs with pull ups	3 µA typ(4)	< 0.1 ms
Wait Mode	ON	ON	Powered (Not clocked)	WFE +SLEEPDEEP bit = 0 +LPM bit = 1	Any Event from: Fast startup through WUP0-15 pins RTC alarm RTT alarm USB wake-up	Clocked back	Previous state saved	Unchanged	5 µA/15 µA (5)	< 10 µs
Sleep Mode	ON	ON	Powered(7) (Not clocked)	WFE or WFI +SLEEPDEEP bit = 0 +LPM bit = 0	Entry mode =WFI Interrupt Only; Entry mode =WFE Any Enabled Interrupt and/or Any Event from: Fast start-up through WUP0-15 pins RTC alarm RTT alarm USB wake-up	Clocked back	Previous state saved	Unchanged	(6)	(6)

Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake up until the first instruction is fetched.
2. The external loads on PIOs are not taken into account in the calculation.
3. Supply Monitor current consumption is not included.
4. Total Current consumption.
5. 5 µA on VDDCORE, 15 µA for total current consumption (using internal voltage regulator), 8 µA for total current consumption (without using internal voltage regulator).
6. Depends on MCK frequency.
7. In this mode the core is supplied and not clocked but some peripherals can be clocked.

5.7 Fast Startup

The device allows the processor to restart in a few microseconds while the processor is in wait mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + SM + RTC + RTT).

The fast restart circuitry, as shown in Figure 5-5, is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4/8/12 MHz fast RC oscillator, switches the master clock on this 4MHz clock and reenables the processor clock.

Figure 5-5. Fast Start-Up Circuitry

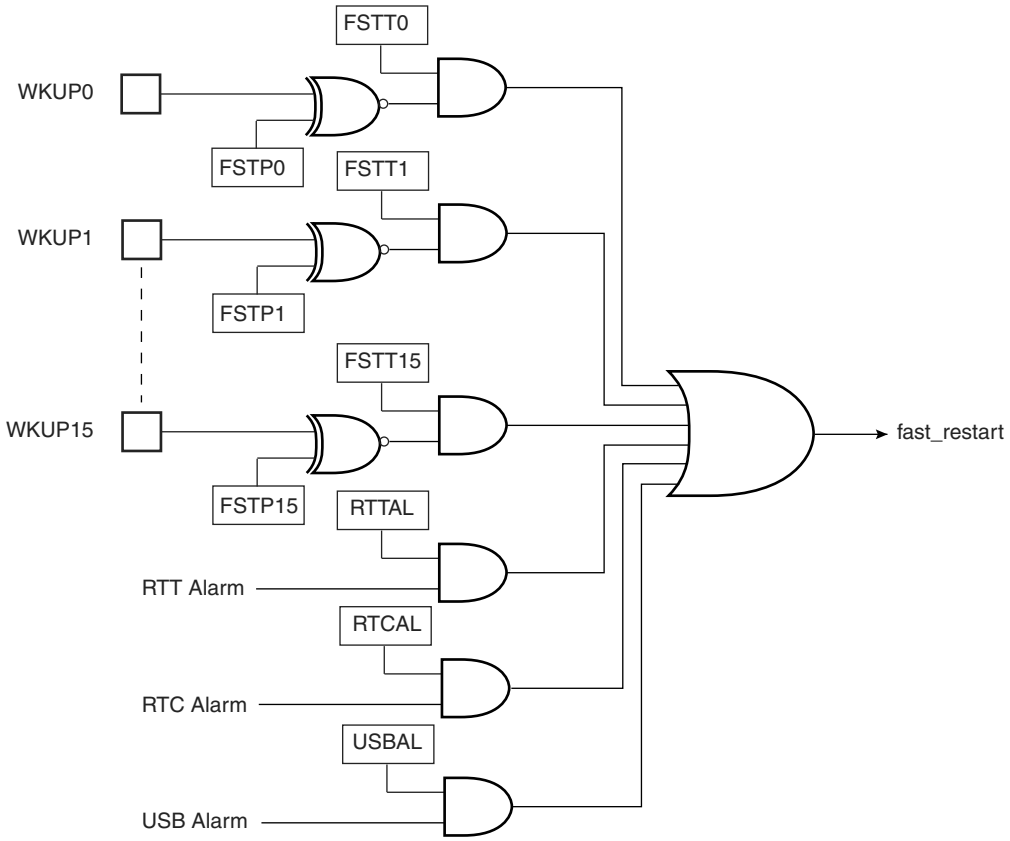


Table 7-4. Peripheral DMA Controller (Continued)

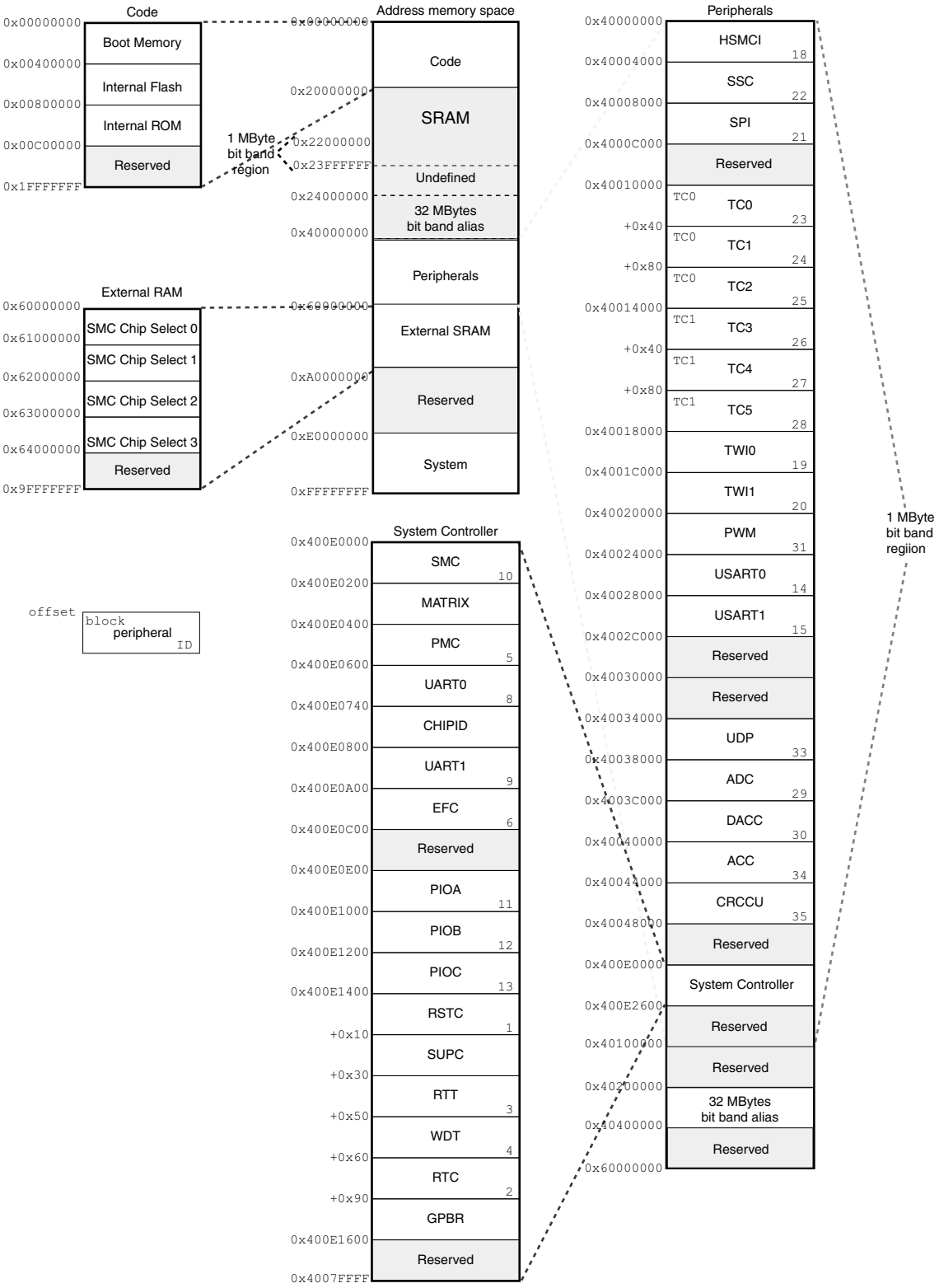
Instance Name	Channel T/R	100 & 64 Pins	48 Pins
USART1	Receive	x	x
USART0	Receive	x	x
ADC	Receive	x	x
SPI	Receive	x	x
SSC	Receive	x	x
HSMCI	Receive	x	N/A
PIOA	Receive	x	x

7.7 Debug and Test Features

- Debug access to all memory and registers in the system, including Cortex-M3 register bank when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE1149.1 JTAG Boundary-can on All Digital Pins

8. Product Mapping

Figure 8-1. SAM3S Product Mapping



9.1.3.11 GPNVM Bits

The SAM3S features two GPNVM bits that can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

Table 9-2. General Purpose Non-volatile Memory Bits

GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed via GPNVM.

A general-purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

Setting GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

9.2 External Memories

The SAM3S features an External Bus Interface to provide the interface to a wide range of external memories and to any parallel peripheral.

9.2.1 Static Memory Controller

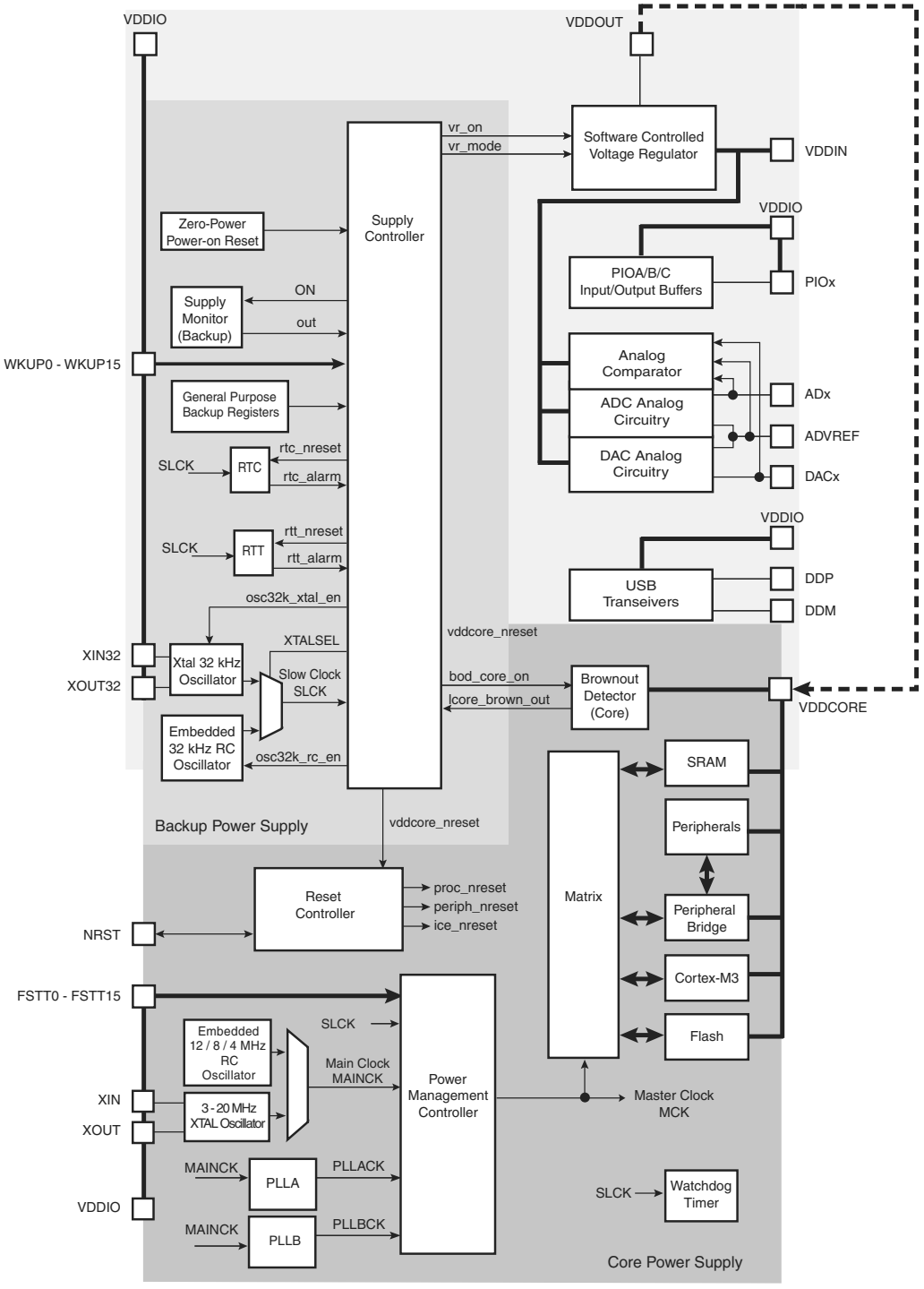
- 8-bit Data Bus
- Up to 24-bit Address Bus (up to 16 MBytes linear per chip select)
- Up to 4 chip selects, Configurable Assignment
- Multiple Access Modes supported
  - Chip Select, Write enable or Read enable Control Mode
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported
- Additional Logic for NAND Flash

10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc...

See the system controller block diagram in Figure 10-1 on page 34.

Figure 10-1. System Controller Block Diagram



FSTT0 - FSTT15 are possible Fast Startup Sources, generated by WKUP0-WKUP15 Pins, but are not physical pins.

10.1 System Controller and Peripheral Mapping

Please refer to Section 8-1 “SAM3S Product Mapping” on page 30.

All the peripherals are in the bit band region and are mapped in the bit band alias region.

10.2 Power-on-Reset, Brownout and Supply Monitor

The SAM3S embeds three features to monitor, warn and/or reset the chip:

• Power-on-Reset on VDDIO

• Brownout Detector on VDDCORE

• Supply Monitor on VDDIO

10.2.1 Power-on-Reset

The Power-on-Reset monitors VDDIO. It is always activated and monitors voltage at start up but also during power down. If VDDIO goes below the threshold voltage, the entire chip is reset. For more information, refer to the Electrical Characteristics section of the datasheet.

10.2.2 Brownout Detector on VDDCORE

The Brownout Detector monitors VDDCORE. It is active by default. It can be deactivated by software through the Supply Controller (SUPC_MR). It is especially recommended to disable it during low-power modes such as wait or sleep modes.

If VDDCORE goes below the threshold voltage, the reset of the core is asserted. For more information, refer to the Supply Controller (SUPC) and Electrical Characteristics sections of the datasheet.

10.2.3 Supply Monitor on VDDIO

The Supply Monitor monitors VDDIO. It is not active by default. It can be activated by software and is fully programmable with 16 steps for the threshold (between 1.9V to 3.4V). It is controlled by the Supply Controller (SUPC). A sample mode is possible. It allows to divide the supply monitor power consumption by a factor of up to 2048. For more information, refer to the SUPC and Electrical Characteristics sections of the datasheet.

10.3 Reset Controller

The Reset Controller is based on a Power-on-Reset cell, and a Supply Monitor on VDDCORE.

The Reset Controller is capable to return to the software the source of the last reset, either a general reset, a wake-up reset, a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin input/output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

The configuration of the Reset Controller is saved as supplied on VDDIO.

10.4 Supply Controller (SUPC)

The Supply Controller controls the power supplies of each section of the processor and the peripherals (via Voltage regulator control)

The Supply Controller has its own reset circuitry and is clocked by the 32 kHz Slow clock generator.

The reset circuitry is based on a zero-power power-on reset cell and a brownout detector cell. The zero-power power-on reset allows the Supply Controller to start properly, while the software-programmable brownout detector allows detection of either a battery discharge or main voltage loss.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

10.14 UART

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

10.15 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB and PIOC (100-pin version only) controlling a maximum of 79 I/O Lines
- Fully programmable through Set/Clear Registers

Table 10-2. PIO available according to pin count

Version	48 pin	64 pin	100 pin
PIOA	21	32	32
PIOB	13	15	15
PIOC	-	-	32

- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change, rising edge, falling edge, low level and level interrupt
  - Debouncing and Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up or pull-down on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3S. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 11-1. Peripheral Identifiers

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	SUPC	X		Supply Controller
1	RSTC	X		Reset Controller
2	RTC	X		Real Time Clock
3	RTT	X		Real Time Timer
4	WDT	X		Watchdog Timer
5	PMC	X		Power Management Controller
6	EEFC	X		Enhanced Embedded Flash Controller
7	-	-		Reserved
8	UART0	X	X	UART 0
9	UART1	X	X	UART 1
10	SMC	X	X	SMC
11	PIOA	X	X	Parallel I/O Controller A
12	PIOB	X	X	Parallel I/O Controller B
13	PIOC	X	X	Parallel I/O Controller C
14	USART0	X	X	USART 0
15	USART1	X	X	USART 1
16	-	-	-	Reserved
17	-	-	-	Reserved
18	HSMCI	X	X	High Speed Multimedia Card Interface
19	TWI0	X	X	Two Wire Interface 0
20	TWI1	X	X	Two Wire Interface 1
21	SPI	X	X	Serial Peripheral Interface
22	SSC	X	X	Synchronous Serial Controller
23	TC0	X	X	Timer/Counter 0
24	TC1	X	X	Timer/Counter 1
25	TC2	X	X	Timer/Counter 2
26	TC3	X	X	Timer/Counter 3
27	TC4	X	X	Timer/Counter 4
28	TC5	X	X	Timer/Counter 5
29	ADC	X	X	Analog-to-Digital Converter
30	DACC	X	X	Digital-to-Analog Converter
31	PWM	X	X	Pulse Width Modulation
32	CRCCU	X	X	CRC Calculation Unit
33	ACC	X	X	Analog Comparator
34	UDP	X	X	USB Device Port

11.2.1 PIO Controller A Multiplexing

Table 11-2. Multiplexing on PIO Controller A (PIOA)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PA0	PWMH0	TIOA0	A17	WKUP0		High drive
PA1	PWMH1	TIOB0	A18	WKUP1		High drive
PA2	PWMH2	SCK0	DATRG	WKUP2		High drive
PA3	TWD0	NPCS3				High drive
PA4	TWCK0	TCLK0		WKUP3		
PA5	RXD0	NPCS3		WKUP4		
PA6	TXD0	PCK0				
PA7	RTS0	PWMH3			XIN32	
PA8	CTS0	ADTRG		WKUP5	XOUT32	
PA9	URXD0	NPCS1	PWMFI0	WKUP6		
PA10	UTXD0	NPCS2				
PA11	NPCS0	PWMH0		WKUP7		
PA12	MISO	PWMH1				
PA13	MOSI	PWMH2				
PA14	SPCK	PWMH3		WKUP8		
PA15	TF	TIOA1	PWML3	WKUP14/PIODCEN1		
PA16	TK	TIOB1	PWML2	WKUP15/PIODCEN2		
PA17	TD	PCK1	PWMH3	AD0		
PA18	RD	PCK2	A14	AD1		
PA19	RK	PWML0	A15	AD2/WKUP9		
PA20	RF	PWML1	A16	AD3/WKUP10		
PA21	RXD1	PCK1		AD8		64/100-pin versions
PA22	TXD1	NPCS3	NCS2	AD9		64/100-pin versions
PA23	SCK1	PWMH0	A19	PIODCCLK		64/100-pin versions
PA24	RTS1	PWMH1	A20	PIODC0		64/100-pin versions
PA25	CTS1	PWMH2	A23	PIODC1		64/100-pin versions
PA26	DCD1	TIOA2	MCDA2	PIODC2		64/100-pin versions
PA27	DTR1	TIOB2	MCDA3	PIODC3		64/100-pin versions
PA28	DSR1	TCLK1	MCCDA	PIODC4		64/100-pin versions
PA29	RI1	TCLK2	MCCK	PIODC5		64/100-pin versions
PA30	PWML2	NPCS2	MCDA0	WKUP11/PIODC6		64/100-pin versions
PA31	NPCS1	PCK2	MCDA1	PIODC7		64/100-pin versions

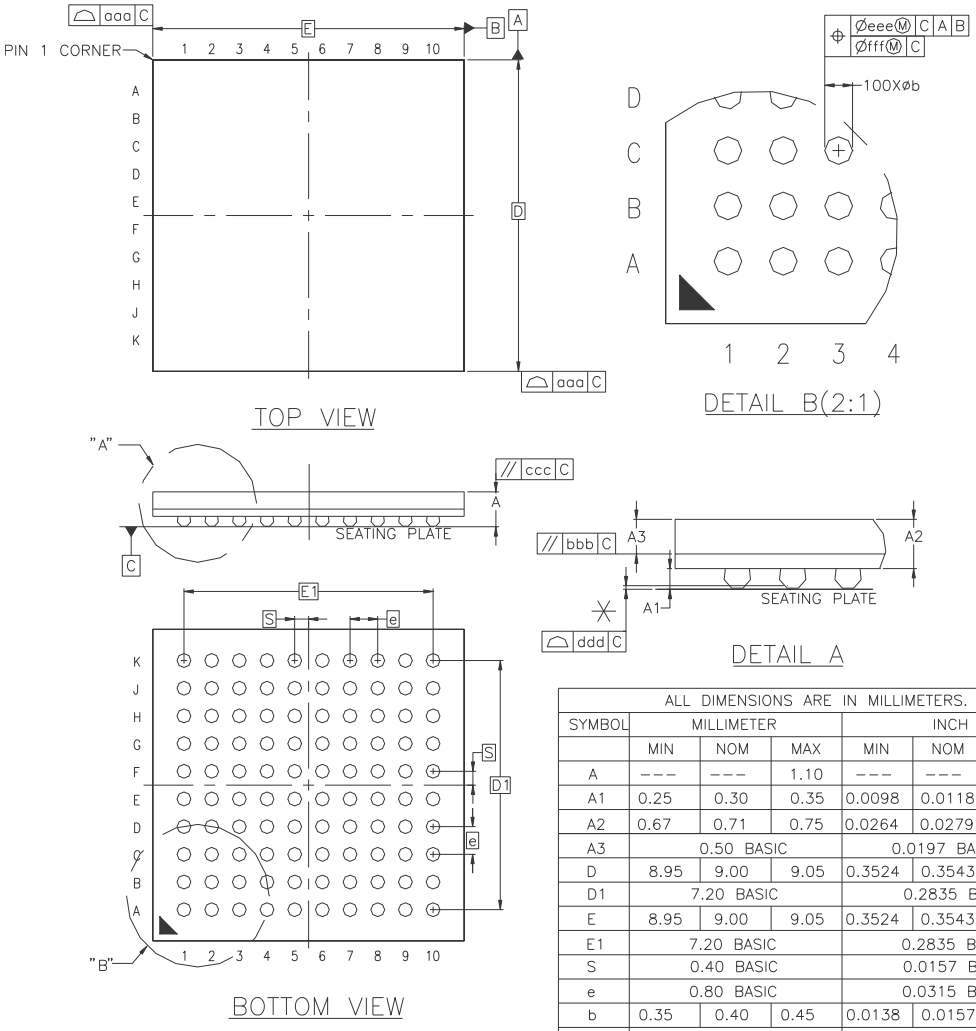
12.13 Analog Comparator

- One analog comparator
- High speed option vs. low power option
- Selectable input hysteresis:
  - 0, 20 mV, 50 mV
- Minus input selection:
  - DAC outputs
  - Temperature Sensor
  - ADVREF
  - AD0 to AD3 ADC channels
- Plus input selection:
  - All analog inputs
- output selection:
  - Internal signal
  - external pin
  - selectable inverter
- Interrupt on:
  - Rising edge, Falling edge, toggle

12.14 Cyclic Redundancy Check Calculation Unit (CRCCU)

- 32-bit cyclic redundancy check automatic calculation
- CRC calculation between two addresses of the memory

Figure 13-2. 100-ball TFBGA Package Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.0575
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.67	0.71	0.75	0.0264	0.0279	0.0295
A3	0.50 BASIC			0.0197 BASIC		
D	8.95	9.00	9.05	0.3524	0.3543	0.3563
D1	7.20 BASIC			0.2835 BASIC		
E	8.95	9.00	9.05	0.3524	0.3543	0.3563
E1	7.20 BASIC			0.2835 BASIC		
S	0.40 BASIC			0.0157 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
aaa	0.15			0.0059		
bbb	0.20			0.0079		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

Figure 13-3. 64- and 48-lead LQFP Package Drawing