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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	EBI/EMI, I²C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	79
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 15x10/12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3s1cb-cu

1. Features

- **Core**
  - **ARM® Cortex®-M3 revision 2.0 running at up to 64 MHz**
  - **Memory Protection Unit (MPU)**
  - **Thumb®-2 instruction set**
- **Pin-to-pin compatible with AT91SAM7S series (48- and 64-pin versions)**
- **Memories**
  - **From 64 to 256 Kbytes embedded Flash, 128-bit wide access, memory accelerator, single plane**
  - **From 16 to 48 Kbytes embedded SRAM**
  - **16 Kbytes ROM with embedded bootloader routines (UART, USB) and IAP routines**
  - **8-bit Static Memory Controller (SMC): SRAM, PSRAM, NOR and NAND Flash support**
  - **Memory Protection Unit (MPU)**
- **System**
  - **Embedded voltage regulator for single supply operation**
  - **Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe operation**
  - **Quartz or ceramic resonator oscillators: 3 to 20 MHz main power with Failure Detection and optional low power 32.768 kHz for RTC or device clock**
  - **High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz default frequency for device startup. In-application trimming access for frequency adjustment**
  - **Slow Clock Internal RC oscillator as permanent low-power mode device clock**
  - **Two PLLs up to 130 MHz for device clock and for USB**
  - **Temperature Sensor**
  - **Up to 22 peripheral DMA (PDC) channels**
- **Low Power Modes**
  - **Sleep and Backup modes, down to 1.8 µA in Backup mode**
  - **Ultra low power RTC**
- **Peripherals**
  - **USB 2.0 Device: 12 Mbps, 2668 byte FIFO, up to 8 bidirectional Endpoints. On-Chip Transceiver**
  - **Up to 2 USARTs with ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Mode**
  - **Two 2-wire UARTs**
  - **Up to 2 Two Wire Interface (I2C compatible), 1 SPI, 1 Serial Synchronous Controller (I2S), 1 High Speed Multimedia Card Interface (SDIO/SD Card/MMC)**
  - **Up to 6 Three-Channel 16-bit Timer/Counter with capture, waveform, compare and PWM mode. Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor**
  - **4-channel 16-bit PWM with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter for Motor Control**
  - **32-bit Real-time Timer and RTC with calendar and alarm features**
  - **Up to 15-channel, 1Msps ADC with differential input mode and programmable gain stage**
  - **One 2-channel 12-bit 1Msps DAC**
  - **One Analog Comparator with flexible input selection, Selectable input hysteresis**
  - **32-bit Cyclic Redundancy Check Calculation Unit (CRCCU)**
  - **Write Protected Registers**
- **I/O**
  - **Up to 79 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination**
  - **Three 32-bit Parallel Input/Output Controllers, Peripheral DMA assisted Parallel Capture Mode**
- **Packages**
  - **100-lead LQFP, 14 x 14 mm, pitch 0.5 mm/100-ball TFBGA, 9 x 9 mm, pitch 0.8 mm**
  - **64-lead LQFP, 10 x 10 mm, pitch 0.5 mm/64-pad QFN 9x9 mm, pitch 0.5 mm**
  - **48-lead LQFP, 7 x 7 mm, pitch 0.5 mm/48-pad QFN 7x7 mm, pitch 0.5 mm**

Figure 2-2. SAM3S 64-pin Version Block Diagram

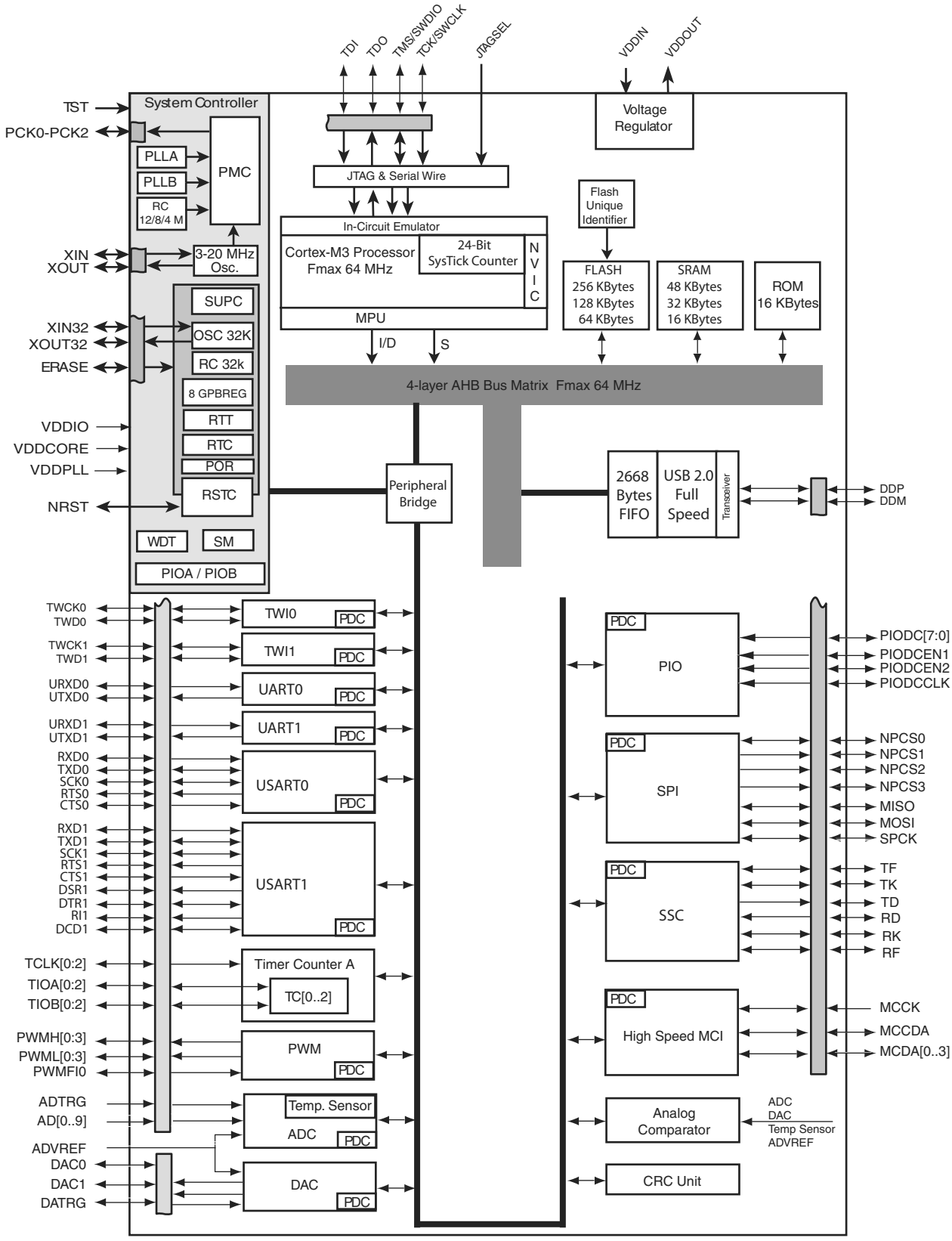
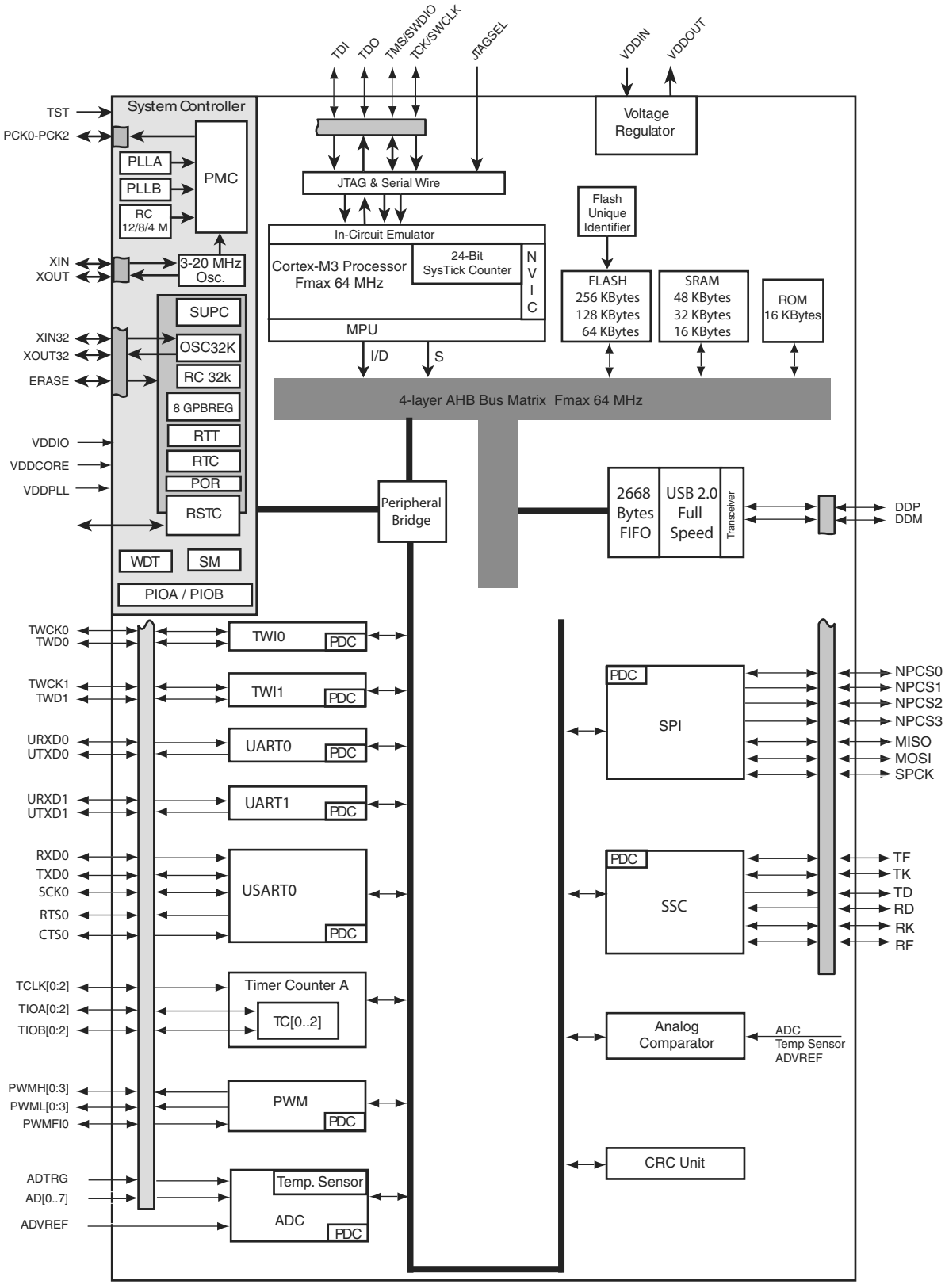


Figure 2-3. SAM3S 48-pin Version Block Diagram



4.2 SAM3S4/2/1B Package and Pinout

Figure 4-3. Orientation of the 64-pad QFN Package

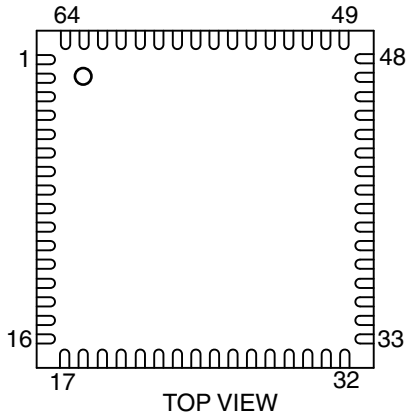


Figure 4-4. Orientation of the 64-lead LQFP Package

64

1

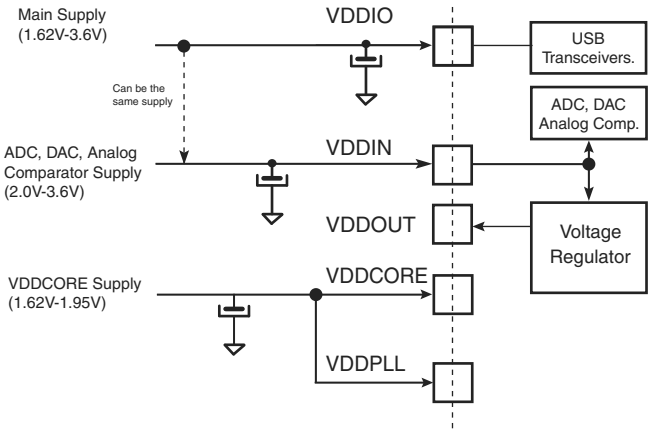
4.3.1 48-Lead LQFP and QFN Pinout

Table 4-4. 48-pin SAM3S4/2/1A Pinout

1	ADVREF	13	VDDIO	25	TDI/PB4	37	TDO/TRACESWO/ PB5
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	PB0/AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS/SWDIO/PB6
4	PB1/AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK/SWCLK/PB7
5	PB2/AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	PB3/AD7	18	VDDCORE	30	TST	42	ERASE/PB12
7	VDDIN	19	PA12/PGMD0	31	PA3	43	DDM/PB10
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	DDP/PB11
9	PA17/PGMD5/ AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT/PB8
10	PA18/PGMD6/ AD1	22	PA9/PGMM1	34	GND	46	XIN/PB9/PGMCK
11	PA19/PGMD7/ AD2	23	PA8/*XOUT32*/ PGMM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/*XIN32*/ PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

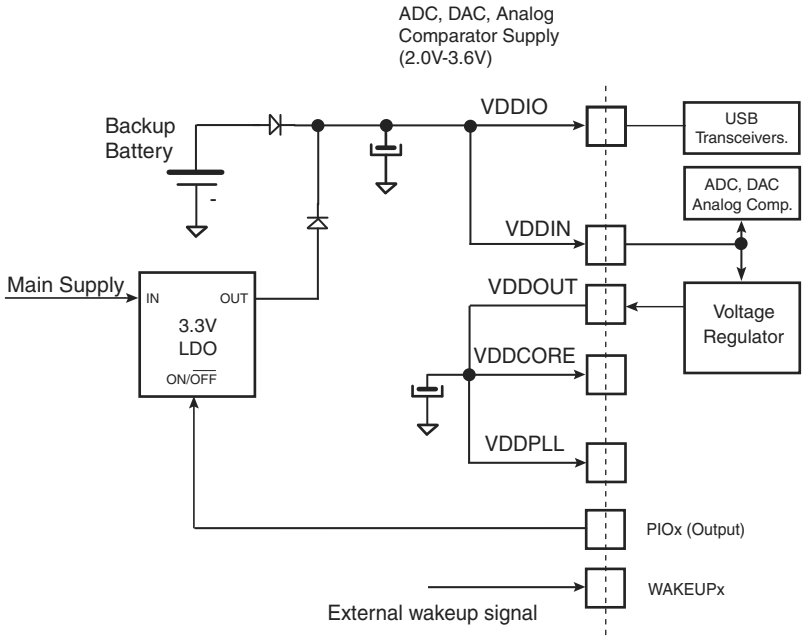
Figure 5-2. Core Externally Supplied



Note: For USB, VDDIO needs to be greater than 3.0V.
For ADC, VDDIN needs to be greater than 2.0V
For DAC, VDDIN needs to be greater than 2.4V.

Figure 5-3 below provides an example of the powering scheme when using a backup battery. Since the PIO state is preserved when in backup mode, any free PIO line can be used to switch off the external regulator by driving the PIO line at low level (PIO is input, pull-up enabled after backup reset). External wake-up of the system can be from a push button or any signal. See Section 5.6 “Wake-up Sources” for further details.

Figure 5-3. Backup Battery

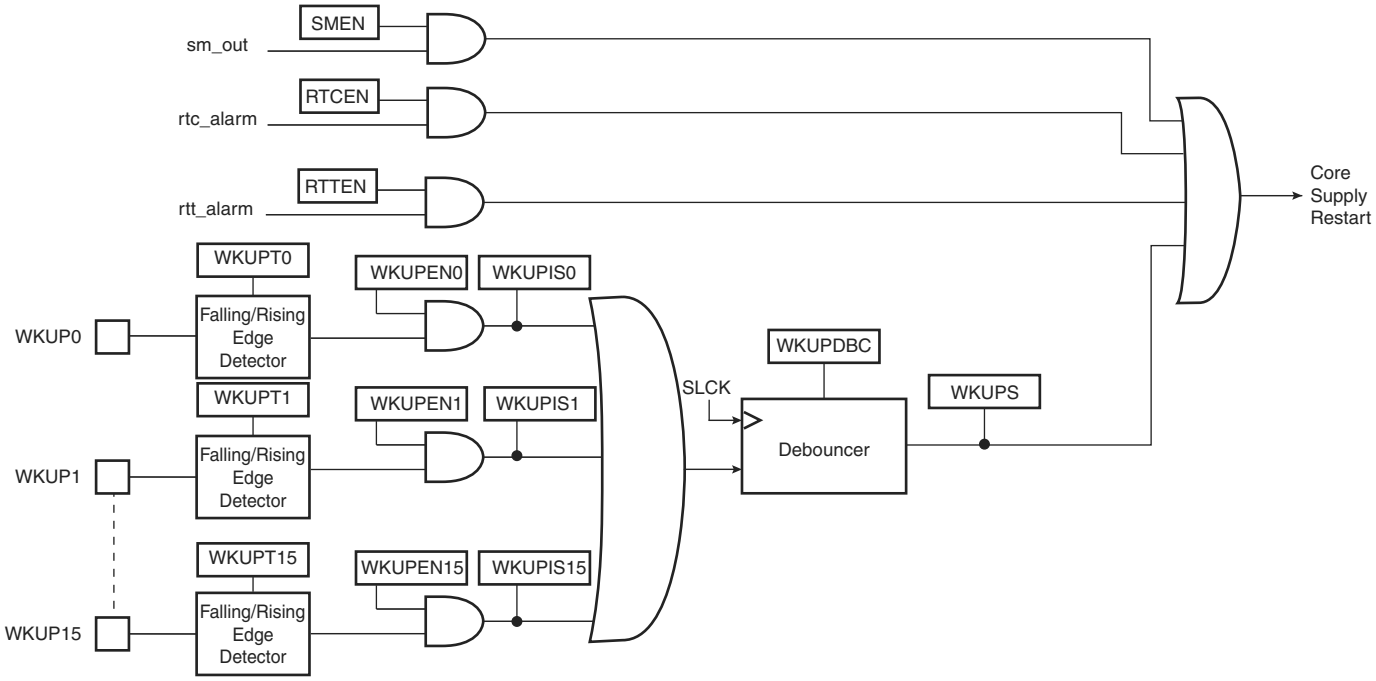


Note: The two diodes provide a “switchover circuit” (for illustration purpose) between the backup battery and the main supply when the system is put in backup mode.

5.6 Wake-up Sources

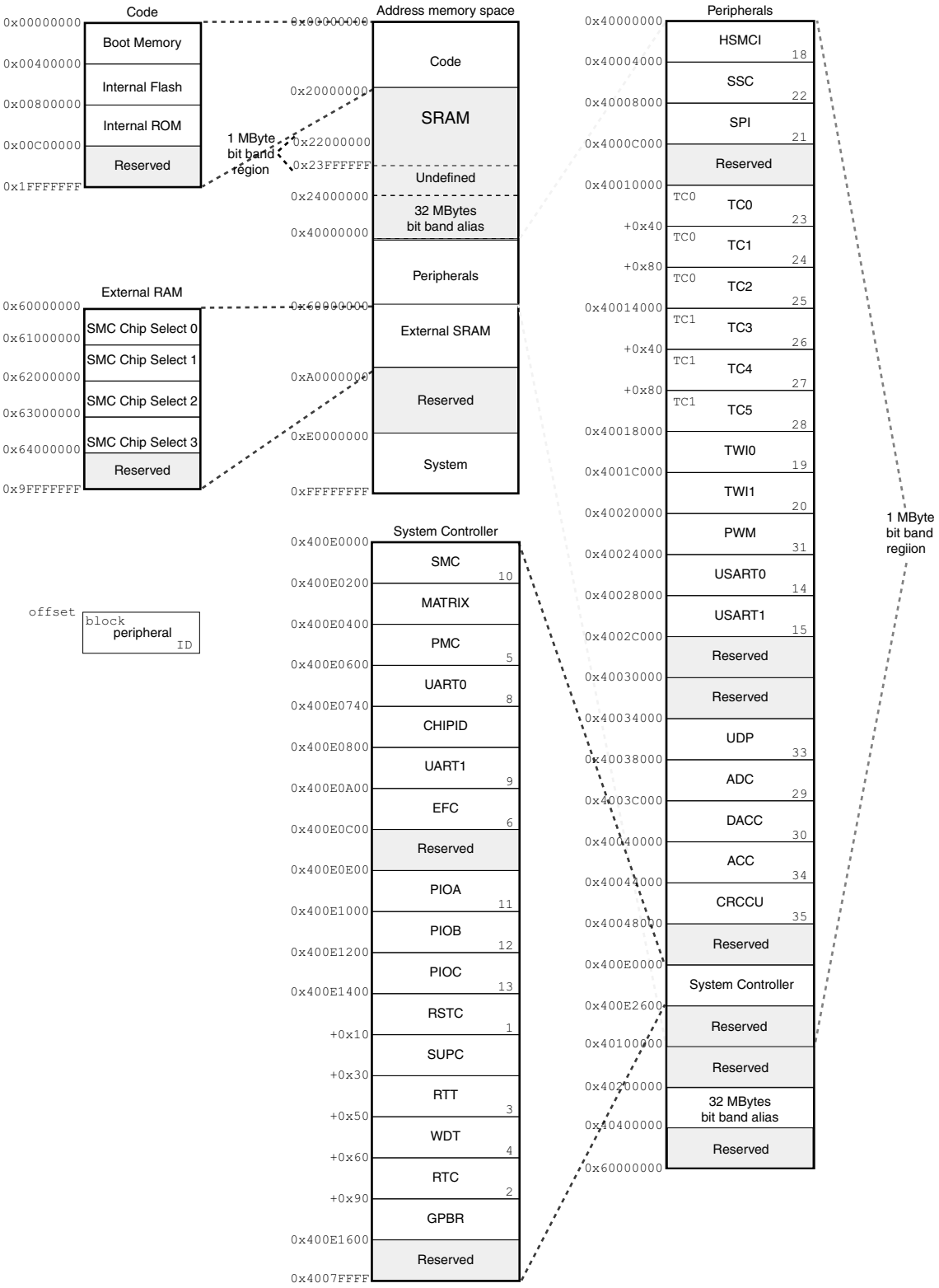
The wake-up events allow the device to exit the backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled.

Figure 5-4. Wake-up Source



8. Product Mapping

Figure 8-1. SAM3S Product Mapping



9.1.3.5 Lock Regions

Several lock bits used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 9-1. Number of Lock Bits

Product	Number of Lock Bits	Lock Region Size
ATSAM3S4	16	16 kbytes (64 pages)
ATSAM3S2	8	16 kbytes (64 pages)
ATSAM3S1	4	16 kbytes (64 pages)

If a locked-region's erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.6 Security Bit Feature

The SAM3S features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, SRAM, Core Registers and Internal Peripherals either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the command "Set General Purpose NVM Bit 0" of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash, SRAM, Core registers, Internal Peripherals are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.7 Calibration Bits

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.8 Unique Identifier

Each device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

9.1.3.9 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when TST is tied high and PA0 and PA1 are tied low.

9.1.3.10 SAM-BA® Boot

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART and USB.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

9.1.3.11 GPNVM Bits

The SAM3S features two GPNVM bits that can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

Table 9-2. General Purpose Non-volatile Memory Bits

GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed via GPNVM.

A general-purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

Setting GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

9.2 External Memories

The SAM3S features an External Bus Interface to provide the interface to a wide range of external memories and to any parallel peripheral.

9.2.1 Static Memory Controller

- 8-bit Data Bus
- Up to 24-bit Address Bus (up to 16 MBytes linear per chip select)
- Up to 4 chip selects, Configurable Assignment
- Multiple Access Modes supported
  - Chip Select, Write enable or Read enable Control Mode
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported
- Additional Logic for NAND Flash

10.1 System Controller and Peripheral Mapping

Please refer to Section 8-1 “SAM3S Product Mapping” on page 30.

All the peripherals are in the bit band region and are mapped in the bit band alias region.

10.2 Power-on-Reset, Brownout and Supply Monitor

The SAM3S embeds three features to monitor, warn and/or reset the chip:

• Power-on-Reset on VDDIO

• Brownout Detector on VDDCORE

• Supply Monitor on VDDIO

10.2.1 Power-on-Reset

The Power-on-Reset monitors VDDIO. It is always activated and monitors voltage at start up but also during power down. If VDDIO goes below the threshold voltage, the entire chip is reset. For more information, refer to the Electrical Characteristics section of the datasheet.

10.2.2 Brownout Detector on VDDCORE

The Brownout Detector monitors VDDCORE. It is active by default. It can be deactivated by software through the Supply Controller (SUPC_MR). It is especially recommended to disable it during low-power modes such as wait or sleep modes.

If VDDCORE goes below the threshold voltage, the reset of the core is asserted. For more information, refer to the Supply Controller (SUPC) and Electrical Characteristics sections of the datasheet.

10.2.3 Supply Monitor on VDDIO

The Supply Monitor monitors VDDIO. It is not active by default. It can be activated by software and is fully programmable with 16 steps for the threshold (between 1.9V to 3.4V). It is controlled by the Supply Controller (SUPC). A sample mode is possible. It allows to divide the supply monitor power consumption by a factor of up to 2048. For more information, refer to the SUPC and Electrical Characteristics sections of the datasheet.

10.3 Reset Controller

The Reset Controller is based on a Power-on-Reset cell, and a Supply Monitor on VDDCORE.

The Reset Controller is capable to return to the software the source of the last reset, either a general reset, a wake-up reset, a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin input/output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

The configuration of the Reset Controller is saved as supplied on VDDIO.

10.4 Supply Controller (SUPC)

The Supply Controller controls the power supplies of each section of the processor and the peripherals (via Voltage regulator control)

The Supply Controller has its own reset circuitry and is clocked by the 32 kHz Slow clock generator.

The reset circuitry is based on a zero-power power-on reset cell and a brownout detector cell. The zero-power power-on reset allows the Supply Controller to start properly, while the software-programmable brownout detector allows detection of either a battery discharge or main voltage loss.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3S. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 11-1. Peripheral Identifiers

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	SUPC	X		Supply Controller
1	RSTC	X		Reset Controller
2	RTC	X		Real Time Clock
3	RTT	X		Real Time Timer
4	WDT	X		Watchdog Timer
5	PMC	X		Power Management Controller
6	EEFC	X		Enhanced Embedded Flash Controller
7	-	-		Reserved
8	UART0	X	X	UART 0
9	UART1	X	X	UART 1
10	SMC	X	X	SMC
11	PIOA	X	X	Parallel I/O Controller A
12	PIOB	X	X	Parallel I/O Controller B
13	PIOC	X	X	Parallel I/O Controller C
14	USART0	X	X	USART 0
15	USART1	X	X	USART 1
16	-	-	-	Reserved
17	-	-	-	Reserved
18	HSMCI	X	X	High Speed Multimedia Card Interface
19	TWI0	X	X	Two Wire Interface 0
20	TWI1	X	X	Two Wire Interface 1
21	SPI	X	X	Serial Peripheral Interface
22	SSC	X	X	Synchronous Serial Controller
23	TC0	X	X	Timer/Counter 0
24	TC1	X	X	Timer/Counter 1
25	TC2	X	X	Timer/Counter 2
26	TC3	X	X	Timer/Counter 3
27	TC4	X	X	Timer/Counter 4
28	TC5	X	X	Timer/Counter 5
29	ADC	X	X	Analog-to-Digital Converter
30	DACC	X	X	Digital-to-Analog Converter
31	PWM	X	X	Pulse Width Modulation
32	CRCCU	X	X	CRC Calculation Unit
33	ACC	X	X	Analog Comparator
34	UDP	X	X	USB Device Port

11.2.2 PIO Controller B Multiplexing

Table 11-3. Multiplexing on PIO Controller B (PIOB)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PB0	PWMH0			AD4		
PB1	PWMH1			AD5		
PB2	URXD1	NPCS2		AD6/ WKUP12		
PB3	UTXD1	PCK2		AD7		
PB4	TWD1	PWMH2			TDI	
PB5	TWCK1	PWML0		WKUP13	TDO/TRACESWO	
PB6					TMS/SWDIO	
PB7					TCK/SWCLK	
PB8					XOUT	
PB9					XIN	
PB10					DDM	
PB11					DDP	
PB12	PWML1				ERASE	
PB13	PWML2	PCK0		DAC0		64/100-pin versions
PB14	NPCS1	PWMH3		DAC1		64/100-pin versions

11.2.3 PIO Controller C Multiplexing

Table 11-4. Multiplexing on PIO Controller C (PIOC)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PC0	D0	PWML0				100-pin version
PC1	D1	PWML1				100-pin version
PC2	D2	PWML2				100-pin version
PC3	D3	PWML3				100-pin version
PC4	D4	NPCS1				100-pin version
PC5	D5					100-pin version
PC6	D6					100-pin version
PC7	D7					100-pin version
PC8	NWE					100-pin version
PC9	NANDOE					100-pin version
PC10	NANDWE					100-pin version
PC11	NRD					100-pin version
PC12	NCS3			AD12		100-pin version
PC13	NWAIT	PWML0		AD10		100-pin version
PC14	NCS0					100-pin version
PC15	NCS1	PWML1		AD11		100-pin version
PC16	A21/NANDALE					100-pin version
PC17	A22/NANDCLE					100-pin version
PC18	A0	PWMH0				100-pin version
PC19	A1	PWMH1				100-pin version
PC20	A2	PWMH2				100-pin version
PC21	A3	PWMH3				100-pin version
PC22	A4	PWML3				100-pin version
PC23	A5	TIOA3				100-pin version
PC24	A6	TIOB3				100-pin version
PC25	A7	TCLK3				100-pin version
PC26	A8	TIOA4				100-pin version
PC27	A9	TIOB4				100-pin version
PC28	A10	TCLK4				100-pin version
PC29	A11	TIOA5		AD13		100-pin version
PC30	A12	TIOB5		AD14		100-pin version
PC31	A13	TCLK5				100-pin version

        - By 8 or by-16 over-sampling receiver frequency
        - Hardware handshaking RTS-CTS
        - Receiver time-out and transmitter timeguard
        - Optional Multi-drop Mode with address generation and detection
        - Optional Manchester Encoding
        - Full modem line support on USART1 (DCD-DSR-DTR-RI)
    - RS485 with driver control signal
    - ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
        - NACK handling, error counter with repetition and iteration limit
    - SPI Mode
        - Master or Slave
        - Serial Clock programmable Phase and Polarity
        - SPI Serial Clock (SCK) Frequency up to MCK/4
    - IrDA modulation and demodulation
        - Communication at up to 115.2 Kbps
    - Test Modes
        - Remote Loopback, Local Loopback, Automatic Echo

12.5 Synchronous Serial Controller (SSC)

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I^2S, TDM Buses, Magnetic Card Reader)
- Contains an independent receiver and transmitter and a common clock divider
- Offers configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

12.6 Timer Counter (TC)

- Six 16-bit Timer Counter Channels
- Wide range of functions including:
    - Frequency Measurement
    - Event Counting
    - Interval Measurement
    - Pulse Generation
    - Delay Timing
    - Pulse Width Modulation
    - Up/down Capabilities
- Each channel is user-configurable and contains:
    - Three external clock inputs
    - Five internal clock inputs
    - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels
- Quadrature decoder
    - Advanced line filtering
    - Position / revolution / speed
- 2-bit Gray Up/Down Counter for Stepper Motor

- Eight endpoints
  - Endpoint 0: 64 bytes
  - Endpoint 1 and 2: 64 bytes ping-pong
  - Endpoint 3: 64 bytes
  - Endpoint 4 and 5: 512 bytes ping-pong
  - Endpoint 6 and 7: 64 bytes ping-pong
  - Ping-pong Mode (two memory banks) for Isochronous and bulk endpoints
- Suspend/resume logic
- Integrated Pull-up on DDP
- Pull-down resistor on DDM and DDP when disabled

12.10 Analog-to-Digital Converter (ADC)

- up to 16 Channels,
- 10/12-bit resolution
- up to 1 MSample/s
- programmable sequence of conversion on each channel
- Integrated temperature sensor
- Single ended/differential conversion
- Programmable gain: 1, 2, 4

12.11 Digital-to-Analog Converter (DAC)

- Up to 2 channel 12-bit DAC
- Up to 2 mega-samples conversion rate in single channel mode
- Flexible conversion range
- Multiple trigger sources for each channel
- 2 Sample/Hold (S/H) outputs
- Built-in offset and gain calibration
- Possibility to drive output to ground
- Possibility to use as input to analog comparator or ADC (as an internal wire and without S/H stage)
- Two PDC channels
- Power reduction mode

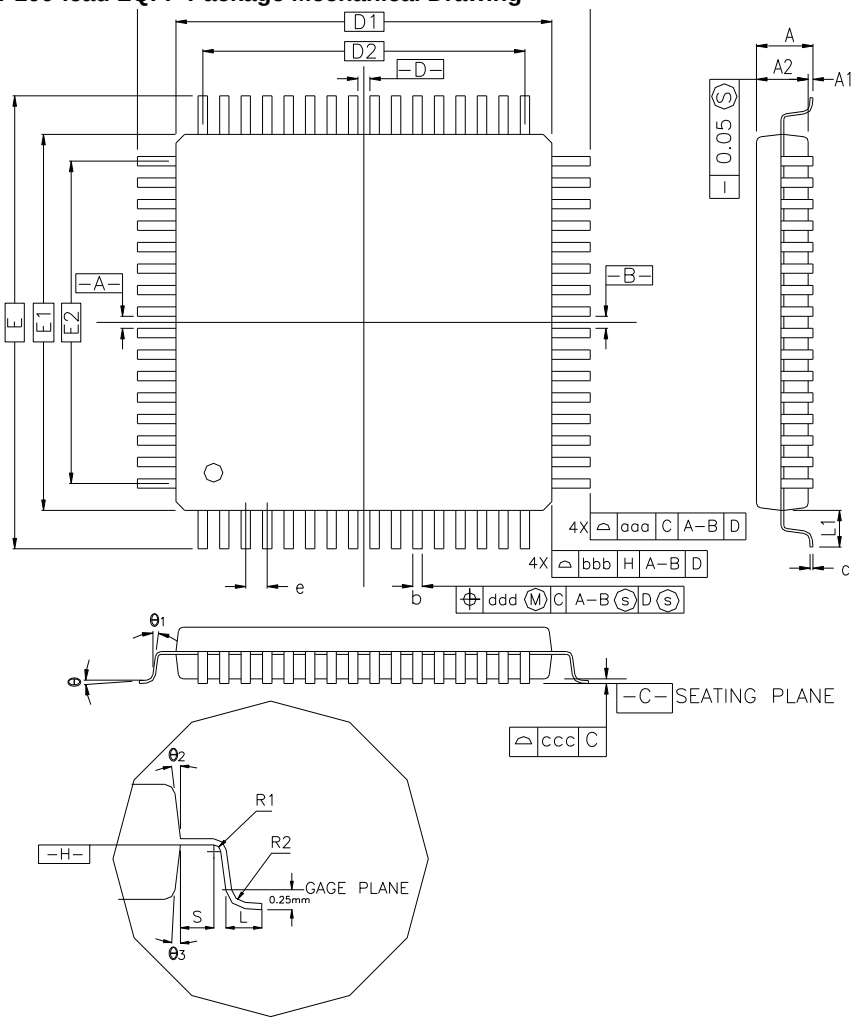
12.12 Static Memory Controller

- 16-Mbyte Address Space per Chip Select
- 8- bit Data Bus
- Word, Halfword, Byte Transfers
- Programmable Setup, Pulse And Hold Time for Read Signals per Chip Select
- Programmable Setup, Pulse And Hold Time for Write Signals per Chip Select
- Programmable Data Float Time per Chip Select
- External Wait Request
- Automatic Switch to Slow Clock Mode
- Asynchronous Read in Page Mode Supported: Page Size Ranges from 4 to 32 Bytes
- NAND FLASH additional logic supporting NAND Flash with Multiplexed Data/Address buses
- Hardware Configurable number of chip select from 1 to 4
- Programmable timing on a per chip select basis

13. Package Drawings

The SAM3S series devices are available in LQFP, QFN and TFBGA packages.

Figure 13-1. 100-lead LQFP Package Mechanical Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

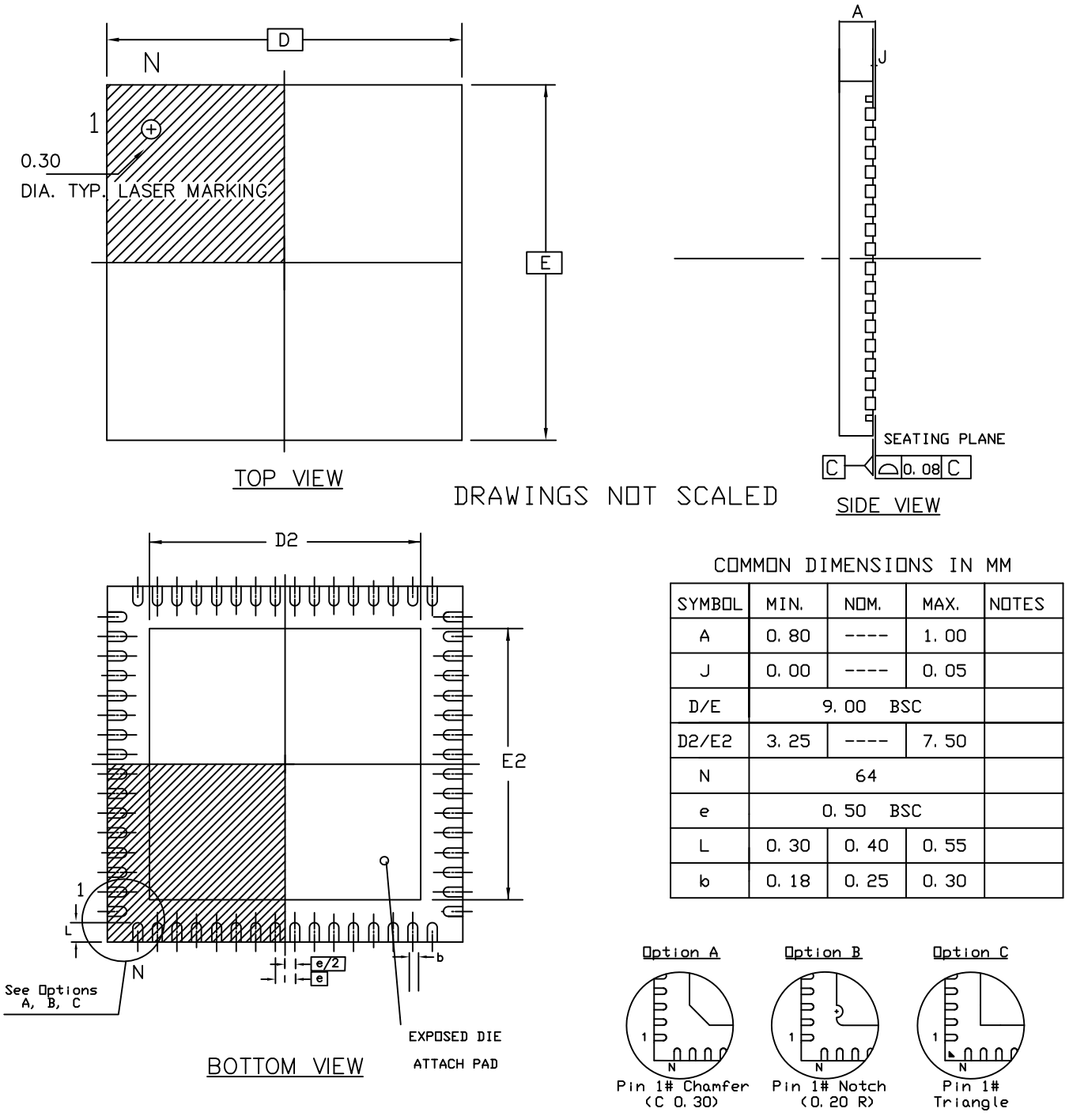
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	M
A	—	—	1.60	—	—	0
A_1	0.05	—	0.15	0.002	—	0
A_2	1.35	1.40	1.45	0.053	0.055	0
D	16.00 BSC.			0.630 BSC		
D_1	14.00 BSC.			0.551 BSC		
E	16.00 BSC.			0.630 BSC		
E_1	14.00 BSC.			0.551 BSC		
R_2	0.08	—	0.20	0.003	—	0
R_1	0.08	—	—	0.003	—	
θ	0°	3.5°	7°	0°	3.5°	
θ_1	0°	—	—	0°	—	
θ_2	11°	12°	13°	11°	12°	
θ_3	11°	12°	13°	11°	12°	
c	0.09	—	0.20	0.004	—	0
L	0.45	0.60	0.75	0.018	0.024	0
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	
b	0.17	0.20	0.27	0.007	0.008	0
e	0.50 BSC.			0.020 BSC.		
D2	12.00			0.472		
E2	12.00			0.472		
TOLERANCES OF FORM AND POSITIO						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Note : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026 for additional information.

Table 13-1. 48-lead LQFP Package Dimensions (in mm)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 13-5. 64-pad QFN Package Drawing



COMMON DIMENSIONS IN MM

SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	----	1.00	
J	0.00	----	0.05	
D/E	9.00 BSC			
D2/E2	3.25	----	7.50	
N	64			
e	0.50 BSC			
L	0.30	0.40	0.55	
b	0.18	0.25	0.30	

Revision History

Doc. Rev	Comments	Change Request Ref.
6500ES	Section 1. “Features”updated, “Low Power Modes” , Sleep and Backup modes, down to 1.8 µA in Backup mode	rfo
	Figure 8-1, "SAM3S Product Mapping", SRAM associated 1 MByte bit band region mapping changed: 0x22000000 to 0x23FFFFFF.	
	Document format updated, subsequently pagination changed	
	Section 14. “Ordering Information” Introduced MRL B for SAM3S1 parts..	8545
6500DS	Replace all mention to 100-ball LFBGA into 100-ball TFBGA.	8044
	Add table note 5 in Table 3-1, “Signal Description List”.	7632
	Add MOSCRCEN bit details in Section 5.5.2 “Wait Mode”.	7639
	Section 9.1.3.9 “Fast Flash Programming Interface” updated.	7668-7901
	Notes under Figure 5-1, "Single Supply" and Figure 5-2, "Core Externally Supplied" modified.	7887
	Cross-References (1) added for 64-pin packages in table Table 1-1, “Configuration Summary”.	8033
	Pin 22 value changed for PA23/PGMD11 in Table 4-1, “100-lead LQFP SAM3S4/2/1C Pinout”.	8093
	"High Frequency Asynchronous clocking mode" removed from Section 12.7 “Pulse Width Modulation Controller (PWM)”	8095
	“Write Protected Registers” added in “Description” , in Peripherals list.	8213
	ADC column values updated in Table 1-1, “Configuration Summary”.	rfo
6500CS	Missing PGMD8 to 15 added to Table 4-1, “100-lead LQFP SAM3S4/2/1C Pinout” and Table 4-2, “100-ball TFBGA SAM3S4/2/1C Pinout”.	rfo
	Section 5.7 “Fast Startup” updated.	
	Typo fixed on back page: ‘techincal’ --> ‘technical’.	7536
	Typos fixed in Section 1. “Features”.	7524
	Missing title added to Table 14-1.	
	PLLA input frequency range updated in Section 10.5 “Clock Generator”.	7494
	A sentence completed in Section 5.5.2 “Wait Mode”.	7492
	Last sentence removed from Section 9.1.3.10 “SAM-BA® Boot”.	7428
	‘three GPNVM bits’ replaced by ‘two GPNVM bits’ in Section 9.1.3.11 “GPNVM Bits”.	
	Leftover sentence removed from Section 4.1 “SAM3S4/2/1C Package and Pinout”.	7394
6500BS	“Packages” on page 2, package size or pitch updated.	
	Table 1-1, “Configuration Summary”, ADC column updated, footnote gives precision on reserved channel.	7214
	Table 4-2, “100-ball TFBGA SAM3S4/2/1C Pinout”, pinout information is available.	6981
	Figure 5-1, "Single Supply",Figure 5-2, "Core Externally Supplied" , updated notes below figures.	7201
	Figure 5-2, "Core Externally Supplied", Figure 5-3, "Backup Battery", ADC, DAC, Analog Comparator supply is 2.0V-3.6V.	7243/rfo
	Section 12.13 “Analog Comparator”, “Peripherals” on page 2, reference to “window function” removed.	7103
	Section 9.1.3.8 “Unique Identifier”, Each device integrates its own 128-bit unique identifier.	7307
6500AS	First issue	