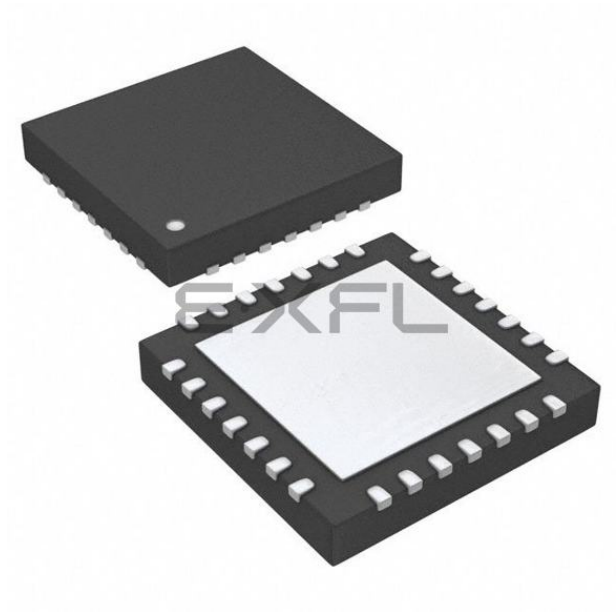

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f716-e-ml

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18-Pin Diagram

18-pin PDIP, SOIC

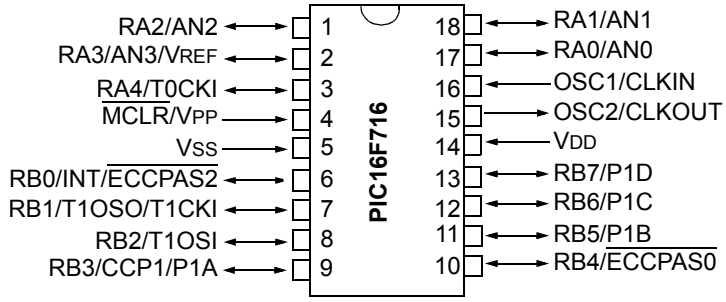


TABLE 1: 18-PIN PDIP, SOIC SUMMARY

I/O	Pin	Analog	ECCP	Timer	Interrupts	Pull-ups	Basic
RA0	17	AN0	—	—	—	—	—
RA1	18	AN1	—	—	—	—	—
RA2	1	AN2	—	—	—	—	—
RA3	2	AN3/VREF	—	—	—	—	—
RA4	3	—	—	T0CKI	—	—	—
RB0	6	—	$\overline{\text{ECCPAS2}}$	—	INT	Y	—
RB1	7	—	—	T1CKI	—	Y	—
RB2	8	—	—	T1OSI	—	Y	—
RB3	9	—	CCP1/P1A	—	—	Y	—
RB4	10	—	$\overline{\text{ECCPAS0}}$	—	IOC	Y	—
RB5	11	—	P1B	—	IOC	Y	—
RB6	12	—	P1C	—	IOC	Y	ICSPCLK
RB7	13	—	P1D	—	IOC	Y	ICSPDAT
—	14	—	—	—	—	—	VDD
—	5	—	—	—	—	—	VSS
—	4	—	—	—	—	—	$\overline{\text{MCLR}}$/VPP
—	16	—	—	—	—	—	OSC1/CLKIN
—	15	—	—	—	—	—	OSC2/CLKOUT

20-Pin Diagram

20-pin SSOP

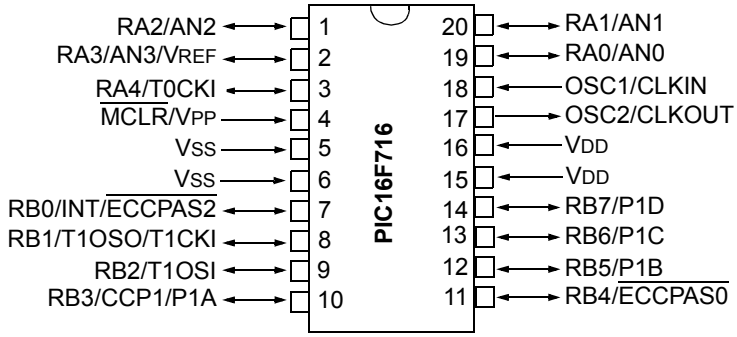


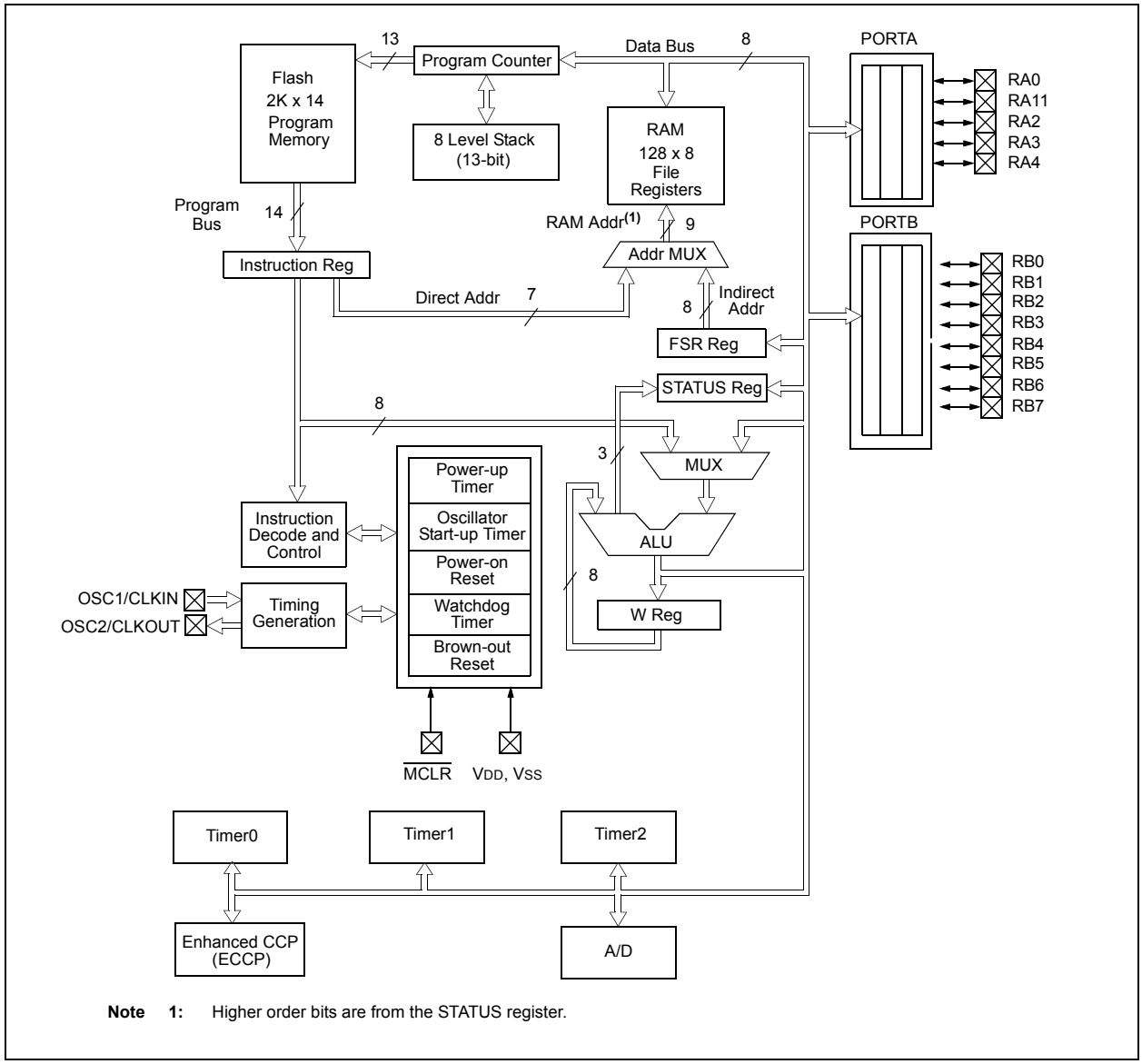
TABLE 2: 20-PIN SSOP SUMMARY

I/O	Pin	Analog	ECCP	Timer	Interrupts	Pull-ups	Basic
RA0	19	AN0	—	—	—	—	—
RA1	20	AN1	—	—	—	—	—
RA2	1	AN2	—	—	—	—	—
RA3	2	AN3/VREF	—	—	—	—	—
RA4	3	—	—	T0CKI	—	—	—
RB0	7	—	$\overline{\text{ECCPAS2}}$	—	INT	Y	—
RB1	8	—	—	T1CKI	—	Y	—
RB2	9	—	—	T1OSI	—	Y	—
RB3	10	—	CCP1/P1A	—	—	Y	—
RB4	11	—	$\overline{\text{ECCPAS0}}$	—	IOC	Y	—
RB5	12	—	P1B	—	IOC	Y	—
RB6	13	—	P1C	—	IOC	Y	ICSPCLK
RB7	14	—	P1D	—	IOC	Y	ICSPDAT
—	15	—	—	—	—	—	VDD
—	16	—	—	—	—	—	VDD
—	5	—	—	—	—	—	VSS
—	6	—	—	—	—	—	VSS
—	4	—	—	—	—	—	$\overline{\text{MCLR}}$/VPP
—	18	—	—	—	—	—	OSC1/CLKIN
—	17	—	—	—	—	—	OSC2/CLKOUT

1.0 DEVICE OVERVIEW

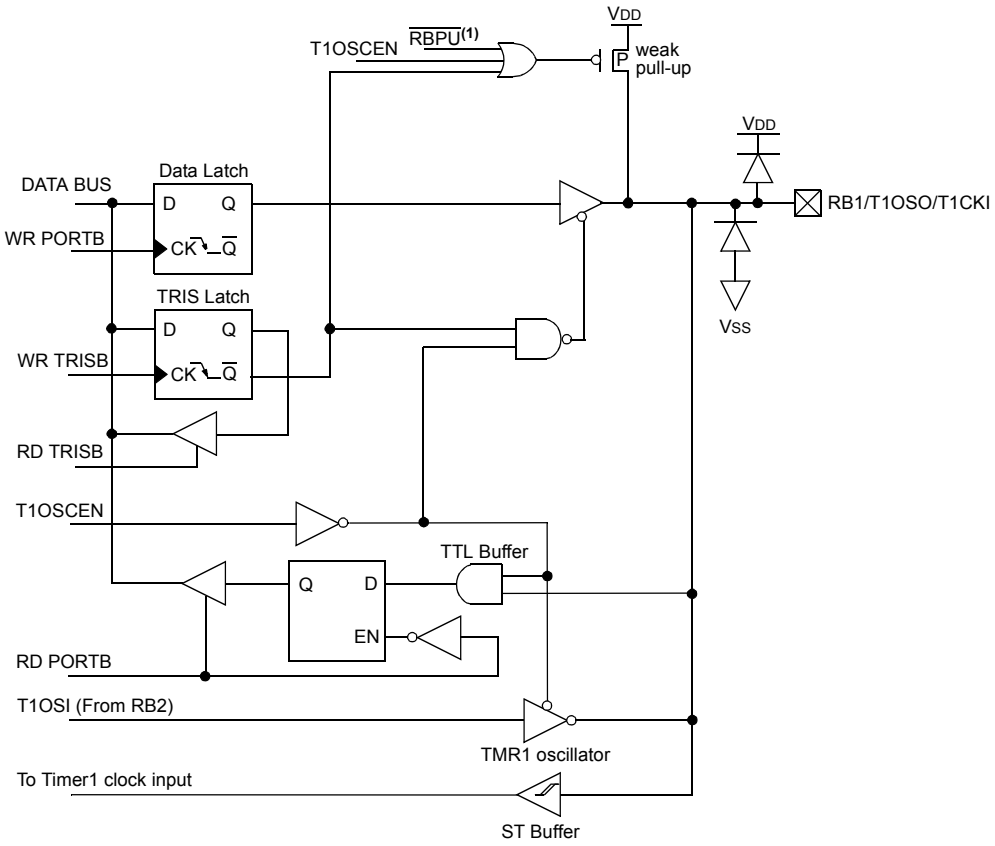
This document contains device specific information for the PIC16F716. Figure 1-1 is the block diagram for the PIC16F716 device. The pinouts are listed in Table 1-1.

FIGURE 1-1: PIC16F716 BLOCK DIAGRAM



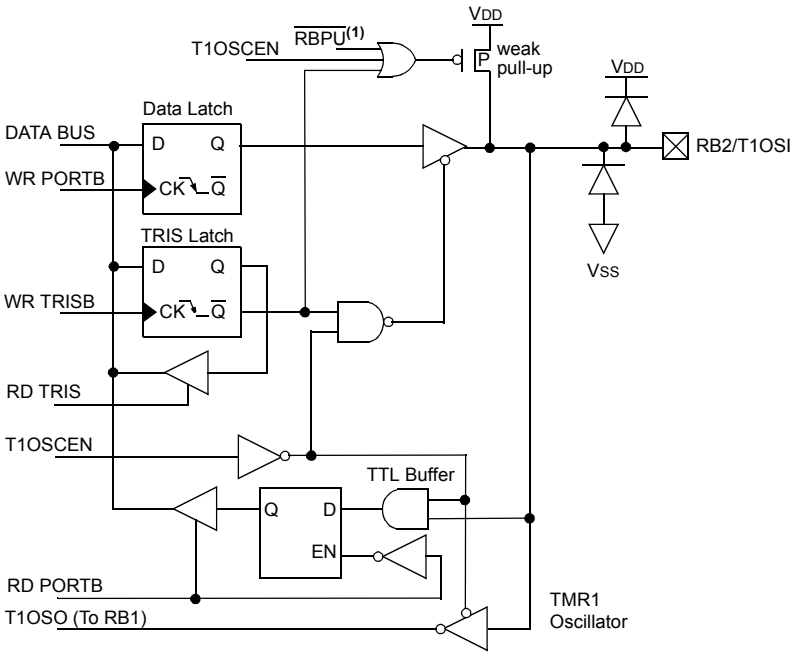
Note 1: Higher order bits are from the STATUS register.

FIGURE 3-4: BLOCK DIAGRAM OF RB1/T1OSO/T1CKI PIN



Note 1: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit (OPTION register).

FIGURE 3-5: BLOCK DIAGRAM OF RB2/T1OSI PIN



Note 1: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (OPTION register).

5.8 ECCP Capture/Compare Time Base

The ECCP module uses the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see **Section 8.0 "Enhanced Capture/Compare/PWM Module"**.

5.9 ECCP Special Event Trigger

If a ECCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The ECCP module may still be configured to generate a ECCP interrupt.

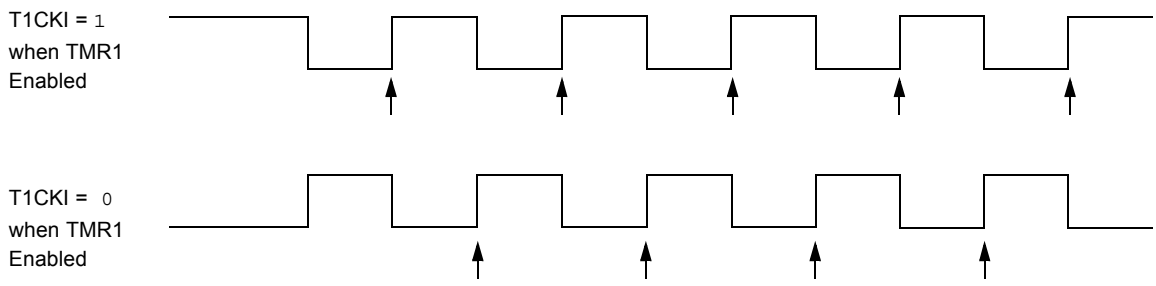
In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer1.

Timer1 should be synchronized to the FOSC to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the ECCP, the write will take precedence.

For more information, see **Section 8.0 "Enhanced Capture/Compare/PWM Module"**.

FIGURE 5-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

TABLE 7-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON	0000 0000	0000 0000
ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000
ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	—	ADIE	—	—	—	CCP1IE	TMR2IE	TMR1IE	-0-- -000	-0-- -000
PIR1	—	ADIF	—	—	—	CCP1IF	TMR2IF	TMR1IF	-0-- -000	-0-- -000
PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, – = unimplemented read as '0'. Shaded cells are not used for ADC module.

REGISTER 8-2: ECCPAS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPASE	ECCPAS2	—	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ECCPASE:** ECCP Auto-Shutdown Event Status bit
1 = A shutdown event has occurred; ECCP outputs are in shutdown state
0 = ECCP outputs are operating

bit 6 **ECCPAS2:** ECCP Auto-Shutdown bit 2
1 = RB0 (INT) pin low level ('0') causes shutdown
0 = RB0 (INT) pin has no effect on ECCP

bit 5 **Unimplemented**: Read as '0'

bit 4 **ECCPAS0:** ECCP Auto-Shutdown bit '0'
1 = RB4 pin low level ('0') causes shutdown
0 = RB4 pin has no effect on ECCP

bit 3-2 **PSSACn:** Pins P1A and P1C Shutdown State Control bits
00 = Drive pins P1A and P1C to '0'
01 = Drive pins P1A and P1C to '1'
1x = Pins P1A and P1C tri-state

bit 1-0 **PSSBDn:** Pins P1B and P1D Shutdown State Control bits
00 = Drive pins P1B and P1D to '0'
01 = Drive pins P1B and P1D to '1'
1x = Pins P1B and P1D tri-state

Note 1: The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.

2: Writing to the ECCPASE bit is disabled while an auto-shutdown condition persists.

3: Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart), the PWM signal will always restart at the beginning of the next PWM period.

9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

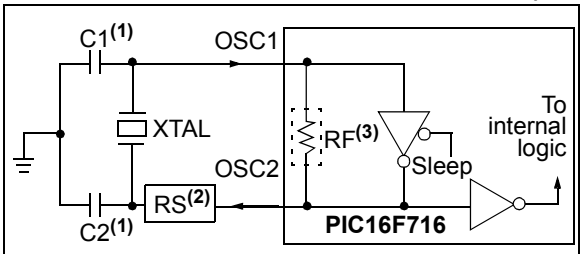
The PIC16F716 can be operated in four different oscillator modes. The user can program two Configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP – Low-power Crystal
- XT – Crystal/Resonator
- HS – High-speed Crystal/Resonator
- RC – Resistor/Capacitor

9.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 9-1). The PIC16F716 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 9-2).

FIGURE 9-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Table 9-1 and Table 9-2 for recommended values of C1 and C2.
2: A series resistor (RS) may be required.
3: RF varies with the crystal chosen.

FIGURE 9-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

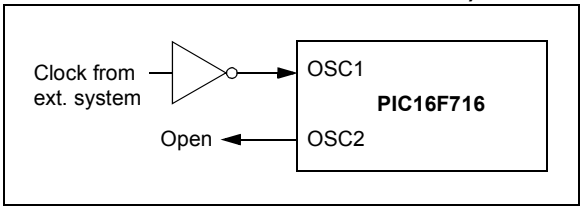


TABLE 9-1: CERAMIC RESONATORS

Ranges Tested:			
Mode	**Freq**	**OSC1 (C1)**	**OSC2 (C2)**
XT	455 kHz 2.0 MHz	68-100 pF 15-68 pF	68-100 pF 15-68 pF
HS	4.0 MHz 8.0 MHz 16.0 MHz	10-68 pF 15-68 pF 10-22 pF	10-68 pF 15-68 pF 10-22 pF

Note 1: These values are for design guidance only. See notes at bottom of page.

TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	15-33 pF	15-33 pF
	200 kHz	5-10 pF	5-10 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15-33 pF	15-33 pF
	4 MHz	15-33 pF	15-33 pF
HS	4 MHz	15-33 pF	15-33 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF

Note 1: These values are for design guidance only. See notes at bottom of page.

Note 1: Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
2: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
3: RS may be required to avoid overdriving crystals with low drive level specification.
4: When using an external clock for the OSC1 input, loading of the OSC2 pin must be kept to a minimum by leaving the OSC2 pin unconnected.

TABLE 9-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset (BOREN = 0)	000h	0001 1xxx	---- --0x
Power-on Reset (BOREN = 1)	000h	0001 1xxx	---- --01
$\overline{\text{MCLR}}$ Reset during normal operation	000h	000u uuuu	---- --uu
$\overline{\text{MCLR}}$ Reset during Sleep	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 1uuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --u0
Interrupt wake-up from Sleep	PC + 1(1)	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

10.0 INSTRUCTION SET SUMMARY

The PIC16F716 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type and one or more **operands,** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 10-1, while the various opcode fields are summarized in Table 10-1.

Table 10-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution time of 1 µs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

10.1 Read-Modify-Write Operations

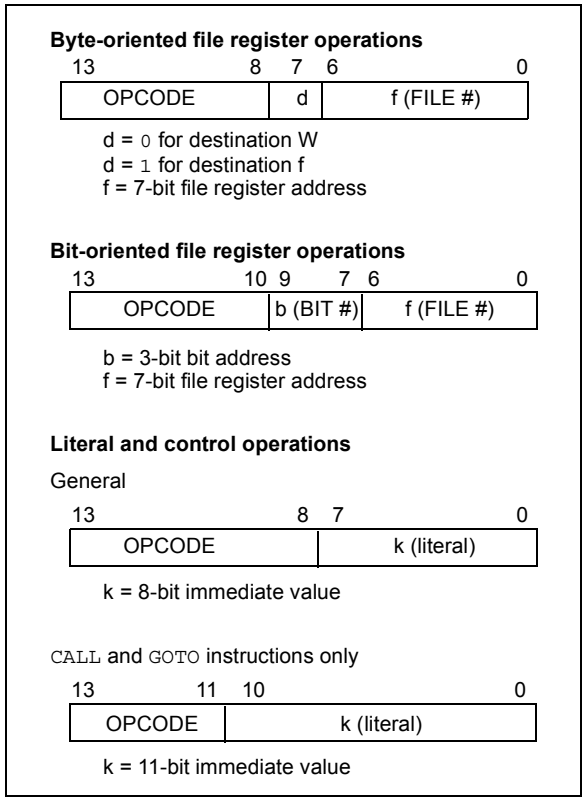
Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a CLRF PORTA instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended consequence of clearing the condition that set the RAIF flag.

TABLE 10-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
$\overline{TO}$	Time-out bit
C	Carry bit
DC	Digit carry bit
Z	Zero bit
$\overline{PD}$	Power-down bit

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS



NOTES:

12.5 AC (Timing) Characteristics

12.5.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created using one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 13-8: MAXIMUM IDD vs. VDD (EXTRC MODE)

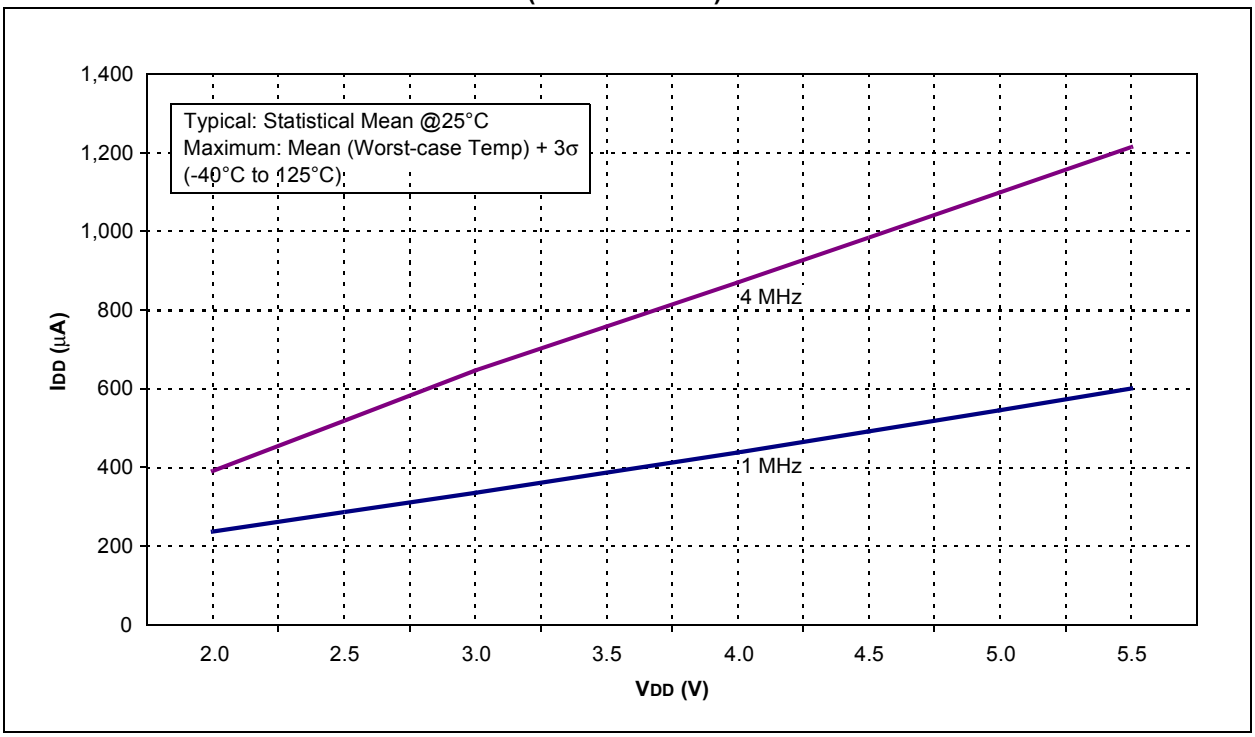


FIGURE 13-9: IDD vs. VDD (LP MODE)

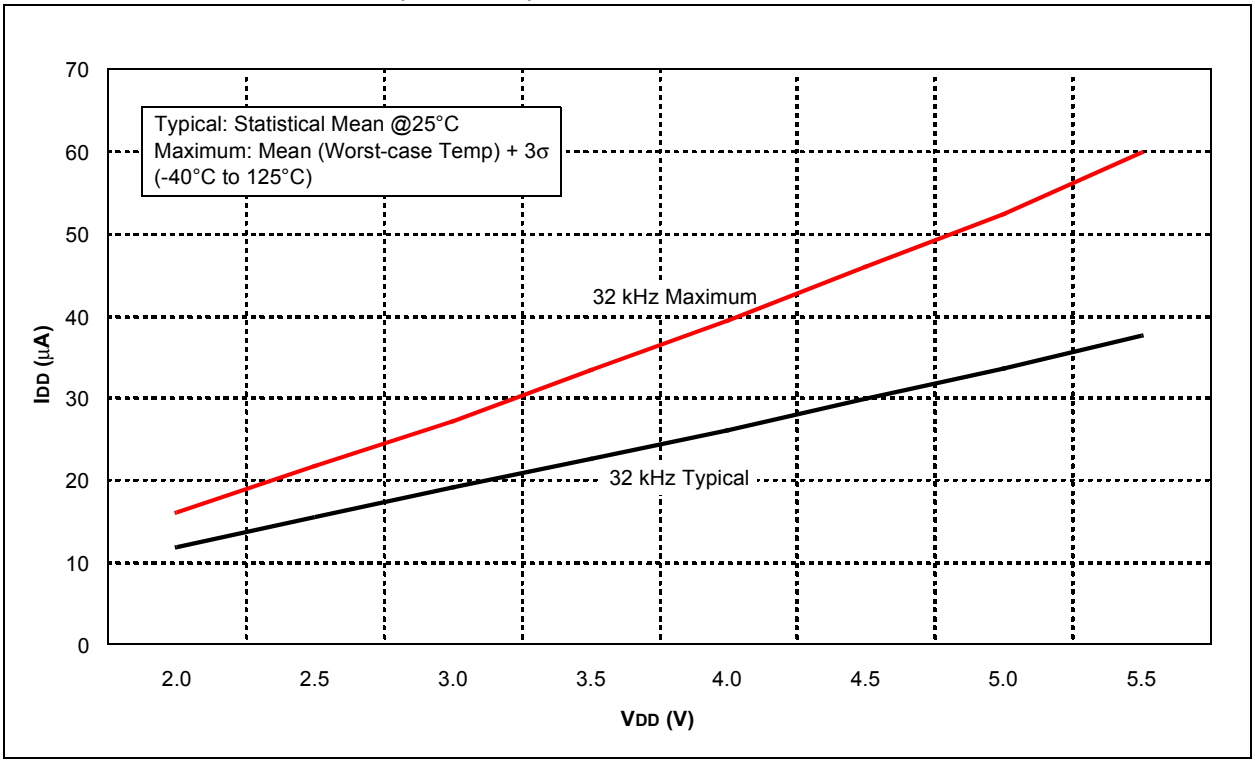


FIGURE 13-23: T1OSC IPD vs. VDD OVER TEMPERATURE (32 kHz)

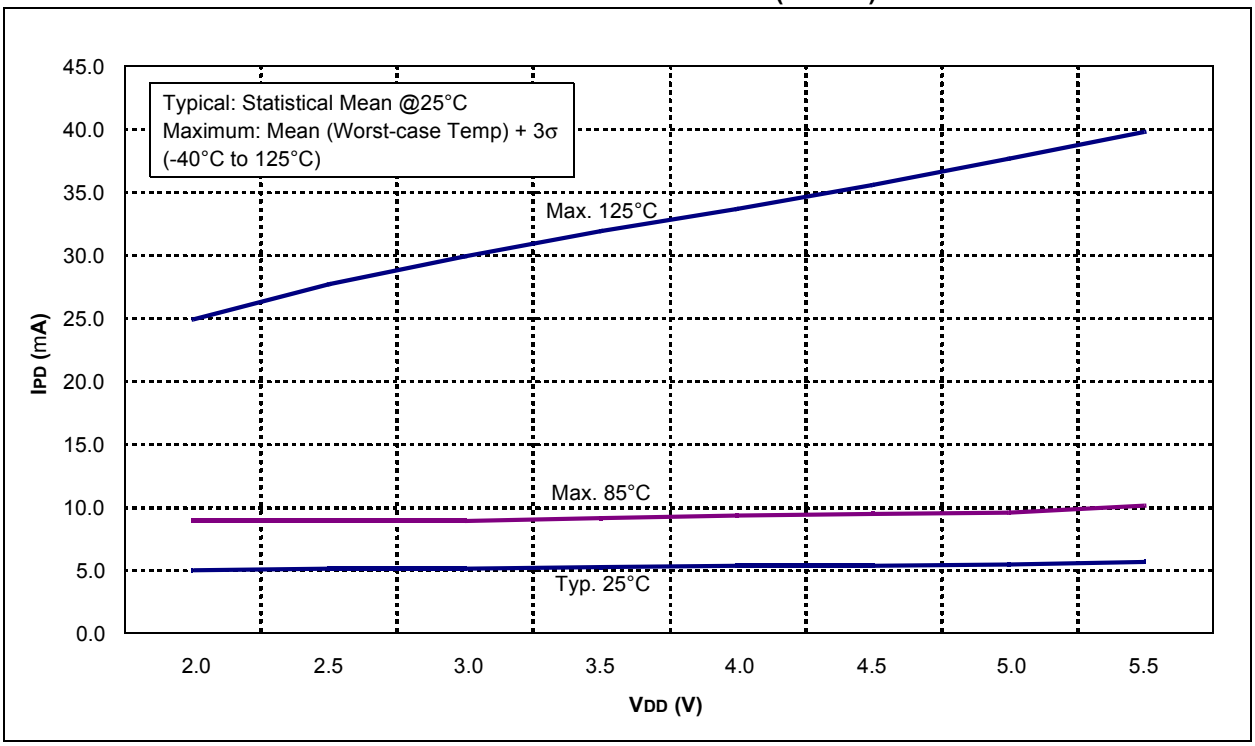
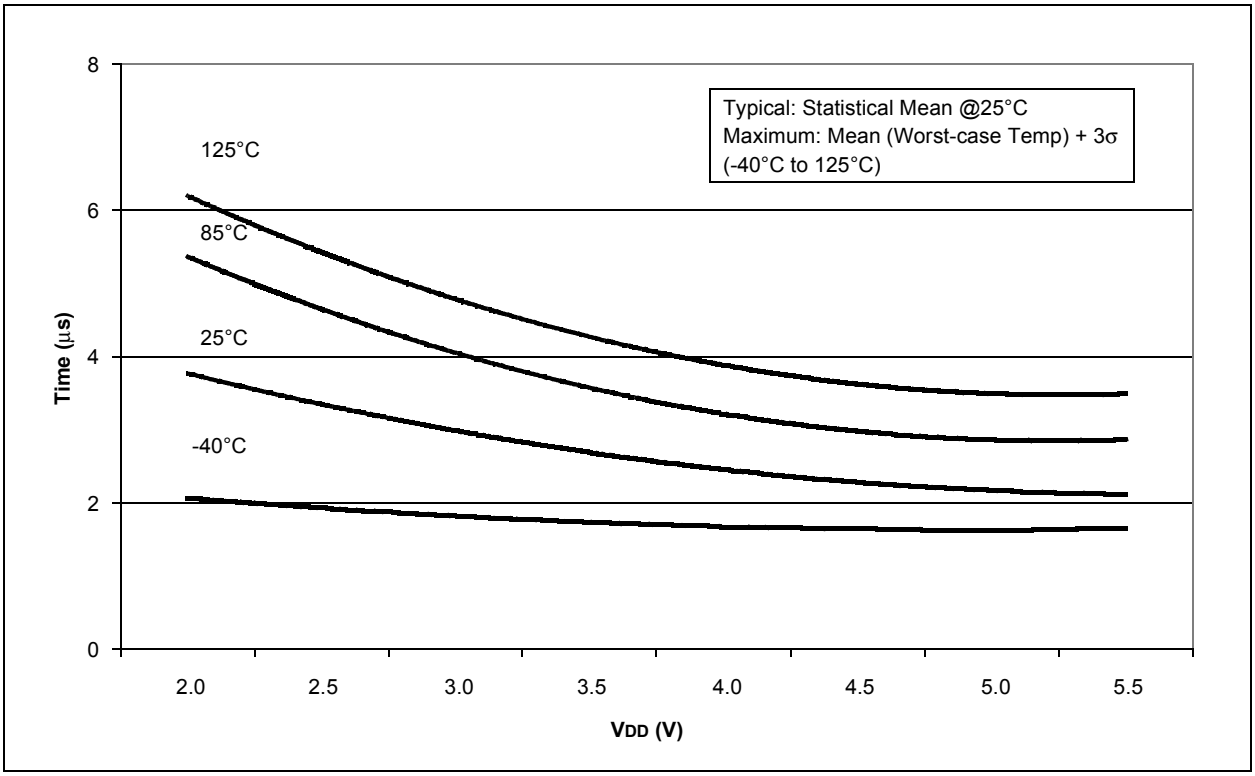


FIGURE 13-24: ADC CLOCK PERIOD vs. VDD OVER TEMPERATURE

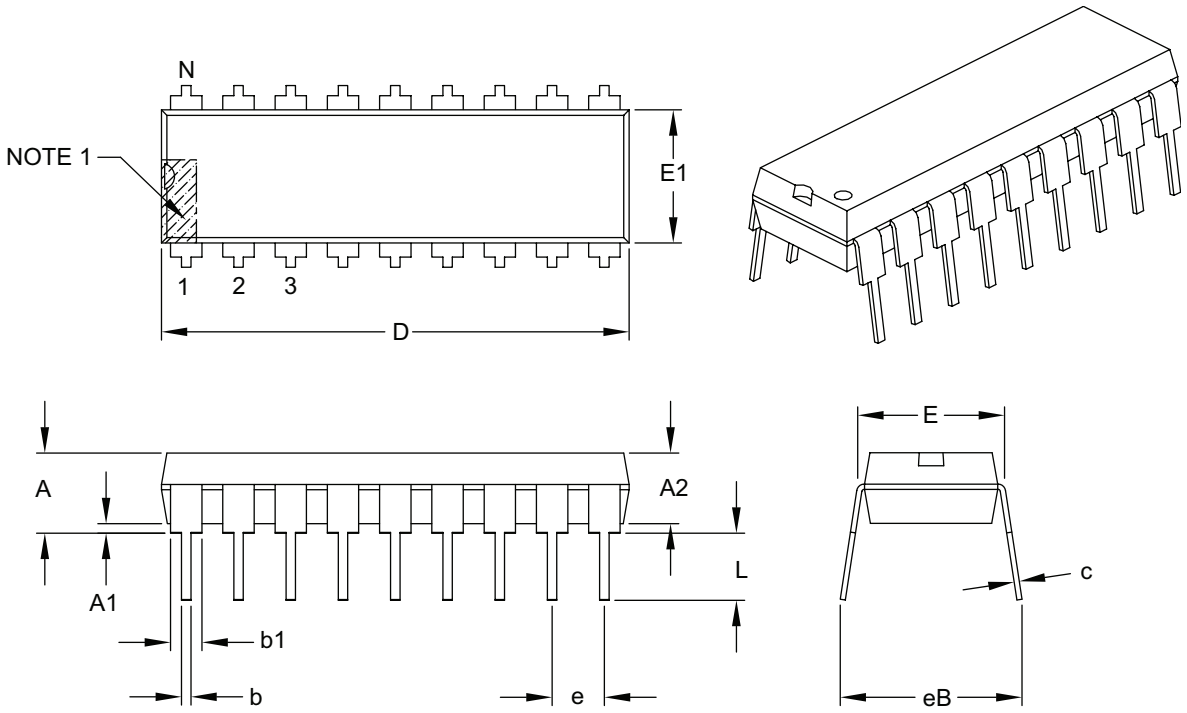


14.2 Package Details

The following sections give the technical details of the packages.

18-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		18	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.880	.900	.920
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.014
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-007B

APPENDIX A: REVISION HISTORY

Revision A (June 2003)

Original data sheet. However, the device described in this data sheet are upgrades to PIC16C716.

Revision B (February 2007)

Updated with current formats and added Characterization Data. Replaced Package Drawings.

APPENDIX B: CONVERSION CONSIDERATIONS

This is a Flash program memory version of the PIC16C716 device. Refer to the migration document, DS40059, for more information about differences between the PIC16F716 and PIC16C716.

APPENDIX C: MIGRATION FROM BASE-LINE TO MID-RANGE DEVICES

This section discusses how to migrate from a baseline device (i.e., PIC16C5X) to a mid-range device (i.e., PIC16F716).

The following are the list of modifications over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14-bits. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and register file (128 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. Bits PA2, PA1, PA0 are removed from STATUS register.
3. Data memory paging is redefined slightly. STATUS register is modified.
4. Four new instructions have been added: `RETURN, RETFIE, ADDLW`, and `SUBLW`. Two instructions `TRIS` and `OPTION` are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION_REG and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different Reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake-up from Sleep through interrupt is added.
11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt-on-change feature.
13. T0CKI pin is also a port pin (RA4) now.
14. FSR is made a full eight-bit register.
15. “In-circuit serial programming” is made possible. The user can program PIC16F716 devices using only five pins: V_{DD}, V_{SS}, $\overline{MCLR}/V_{PP}$, RB6 (clock) and RB7 (data in/out).
16. PCON STATUS register is added with a Power-on Reset Status bit ($\overline{POR}$).
17. Brown-out protection circuitry has been added. Controlled by Configuration Word bits BOREN and BORV. Brown-out Reset ensures the device is placed in a Reset condition if V_{DD} dips below a fixed setpoint.

To convert code written for PIC16C5X to PIC16F716, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for `CALL`, `GOTO`.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change Reset vector to 0000h

.

Note 1: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

2: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required.

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Device: PIC16F716 Literature Number: DS41206B

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