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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f716-e-ss

20-Pin Diagram

20-pin SSOP

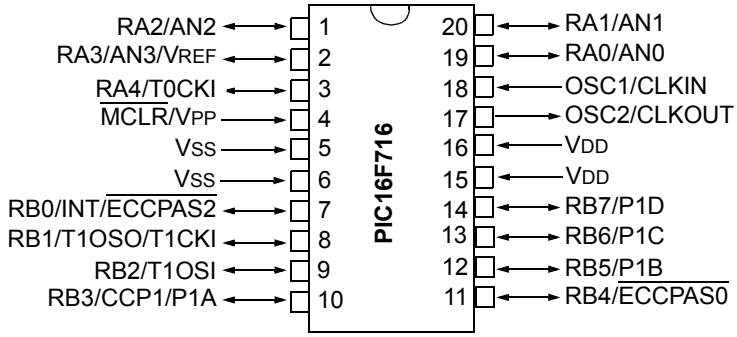


TABLE 2: 20-PIN SSOP SUMMARY

I/O	Pin	Analog	ECCP	Timer	Interrupts	Pull-ups	Basic
RA0	19	AN0	—	—	—	—	—
RA1	20	AN1	—	—	—	—	—
RA2	1	AN2	—	—	—	—	—
RA3	2	AN3/VREF	—	—	—	—	—
RA4	3	—	—	T0CKI	—	—	—
RB0	7	—	$\overline{\text{ECCPAS2}}$	—	INT	Y	—
RB1	8	—	—	T1CKI	—	Y	—
RB2	9	—	—	T1OSI	—	Y	—
RB3	10	—	CCP1/P1A	—	—	Y	—
RB4	11	—	$\overline{\text{ECCPAS0}}$	—	IOC	Y	—
RB5	12	—	P1B	—	IOC	Y	—
RB6	13	—	P1C	—	IOC	Y	ICSPCLK
RB7	14	—	P1D	—	IOC	Y	ICSPDAT
—	15	—	—	—	—	—	VDD
—	16	—	—	—	—	—	VDD
—	5	—	—	—	—	—	VSS
—	6	—	—	—	—	—	VSS
—	4	—	—	—	—	—	$\overline{\text{MCLR}}$/VPP
—	18	—	—	—	—	—	OSC1/CLKIN
—	17	—	—	—	—	—	OSC2/CLKOUT

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains the arithmetic status of the ALU, the Reset status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any Status bits, see the "Instruction Set Summary."

Note 1: The PIC16F716 does not use bits IRP and RP1 of the STATUS register. Maintain these bits clear to ensure upward compatibility with future products.

2: The C and DC bits operate as a $\overline{borrow}$ and $\overline{digit\ borrow}$ bit, respectively, in subtraction.

REGISTER 2-1: STATUS: STATUS REGISTER

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IRP:** This bit is reserved and should be maintained as '0'

bit 6 **RP1:** This bit is reserved and should be maintained as '0'

bit 5 **RP0:** Register Bank Select bit (used for direct addressing)
1 = Bank 1 (80h-FFh)
0 = Bank 0 (00h-7Fh)

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

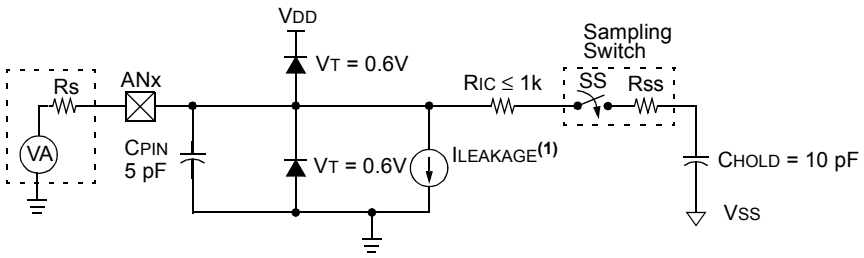
bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

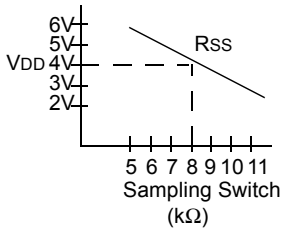
bit 1 **DC:** Digit Carry/$\overline{Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions), For $\overline{Borrow}$, the polarity is reversed.
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

FIGURE 7-2: ANALOG INPUT MODEL





Legend: CPIN = Input Capacitance
VT = Threshold Voltage
I LEAKAGE = Leakage current at the pin due to various junctions
RIC = Interconnect Resistance
SS = Sampling Switch
CHOLD = Sample/Hold Capacitance

Note 1: See **Section 12.0 "Electrical Characteristics"**.

FIGURE 7-3: ADC TRANSFER FUNCTION

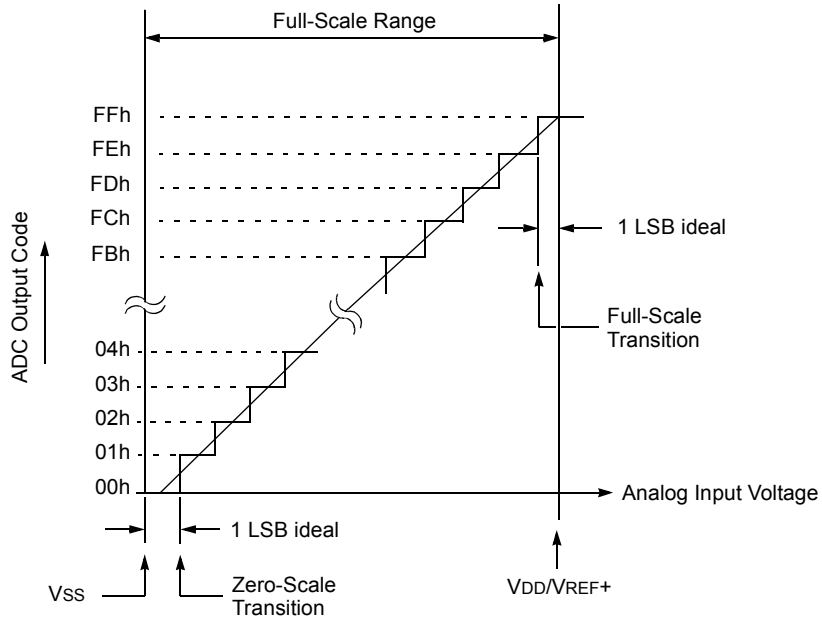


TABLE 7-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON	0000 0000	0000 0000
ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000
ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	—	ADIE	—	—	—	CCP1IE	TMR2IE	TMR1IE	-0-- -000	-0-- -000
PIR1	—	ADIF	—	—	—	CCP1IF	TMR2IF	TMR1IF	-0-- -000	-0-- -000
PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, – = unimplemented read as '0'. Shaded cells are not used for ADC module.

NOTES:

TABLE 8-3: REGISTERS ASSOCIATED WITH COMPARE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	xxxx xxxx
CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	xxxx xxxx
CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	—	ADIE	—	—	—	CCP1IE	TMR2IE	TMR1IE	-0-- -000	-0-- -000
PIR1	—	ADIF	—	—	—	CCP1IF	TMR2IF	TMR1IF	-0-- -000	-0-- -000
PR2	Timer2 Period Register								1111 1111	1111 1111
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	xxxx xxxx
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	xxxx xxxx
TMR2	Timer2 module's register								0000 0000	0000 0000
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Compare.

8.3.3 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 8-4.

EQUATION 8-4: PWM RESOLUTION

$$Resolution = \frac{log[4(PR2 + 1)]}{log(2)} \ bits$$

Note:	If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 8-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 8-5: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

9.0 SPECIAL FEATURES OF THE CPU

The PIC16F716 device has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection. These are:

- OSC Selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Sleep
- Code protection
- ID locations
- In-Circuit Serial Programming™ (ICSP™)

The PIC16F716 device has a Watchdog Timer, which can be shut off only through Configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay on power-up only and is designed to keep the part in Reset while the power supply stabilizes. With these two timers on-chip, most applications need no external Reset circuitry.

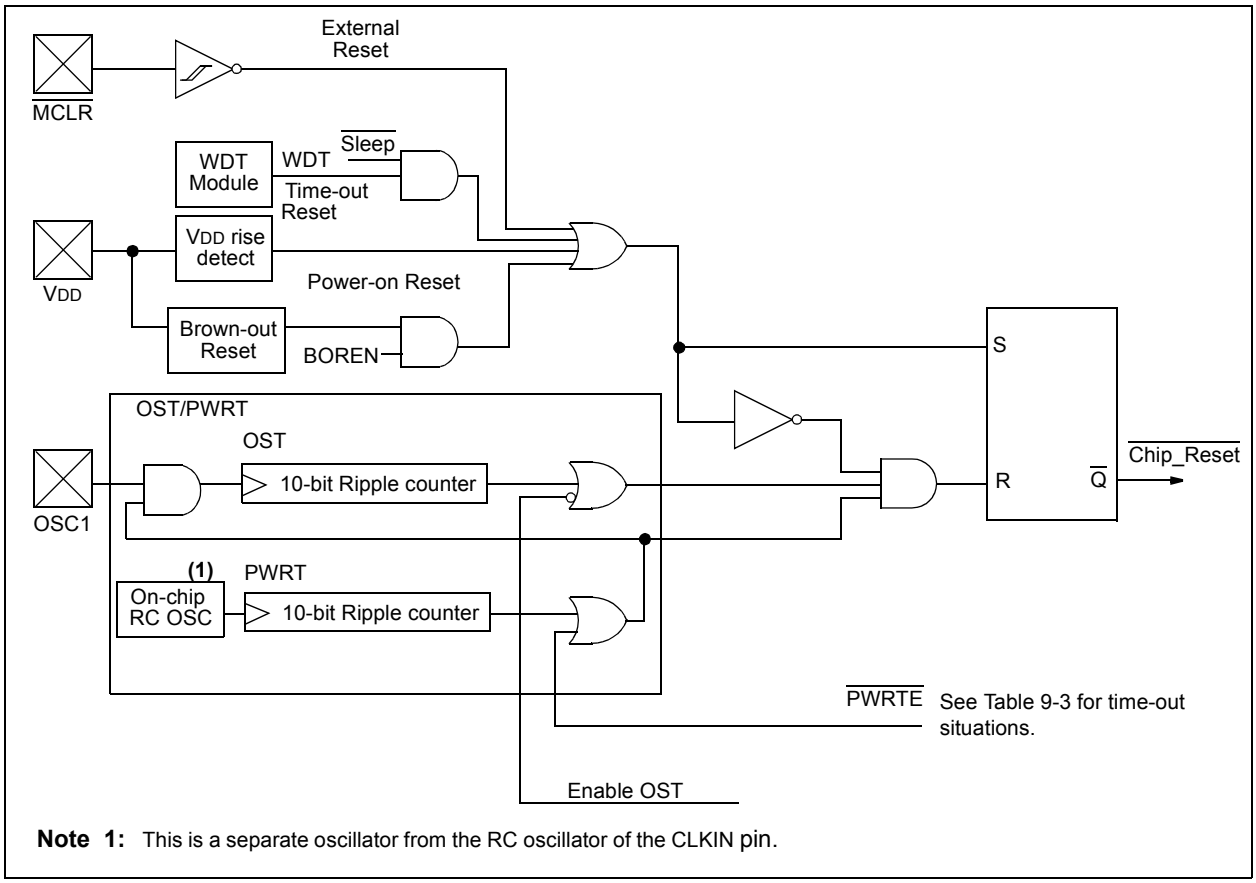
Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through external Reset, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of Configuration bits are used to select various options.

9.1 Configuration Bits

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming.

FIGURE 9-5: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin.

FIGURE 9-6: BROWN-OUT SITUATIONS ($\overline{PWRTE}$ = 0)

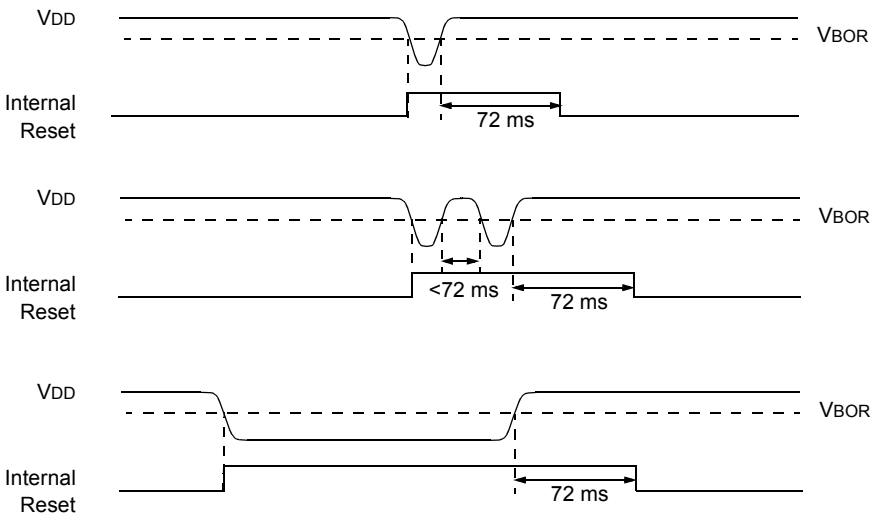
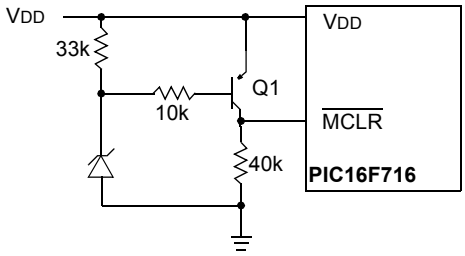
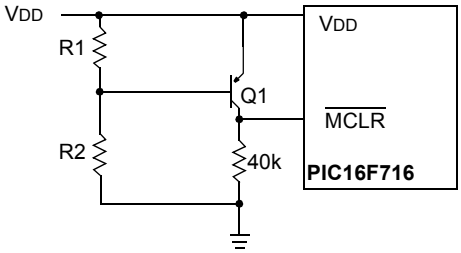


FIGURE 9-7: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



Note 1: This circuit will activate Reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.
2: Internal Brown-out Reset circuitry should be disabled when using this circuit.

FIGURE 9-8: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2

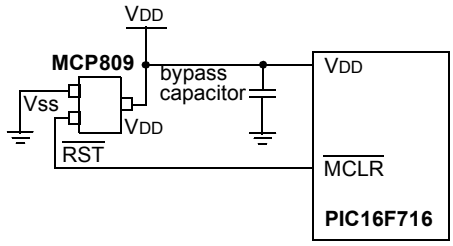


Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \times \frac{R1}{R1 + R2} = 0.7\ V$$

2: Internal Brown-out Reset should be disabled when using this circuit.
3: Resistors should be adjusted for the characteristics of the transistor.

FIGURE 9-9: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



Note 1: This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both high and low active Reset pins. There are 7 different trip point selections to accommodate 5V and 3V systems.

TABLE 9-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS OF THE PIC16F716

Register	Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets WDT Reset	Wake-up via WDT or Interrupt
W	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	N/A	N/A	N/A
TMR0	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	0000h	0000h	PC + 1(2)
STATUS	0001 1xxx	000q quuu(3)	uuuq quuu(3)
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA(4), (5), (6)	--xx 0000	--xx 0000	--uu uuuu
PORTB(4), (5)	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	---0 0000	---0 0000	---u uuuu
INTCON	0000 -00x	0000 -00u	uuuu -uuu(1)
PIR1	-0-- -000	-0-- -000	-u-- -uuu(1)
TMR1L	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	--00 0000	--uu uuuu	--uu uuuu
TMR2	0000 0000	0000 0000	uuuu uuuu
T2CON	-000 0000	-000 0000	-uuu uuuu
CCPR1L	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	0000 0000	0000 0000	uuuu uuuu
PWM1CON	0000 0000	0000 0000	uuuu uuuu
ECCPAS	00-0 0000	00-0 0000	u-uu uuuu
ADRES	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	0000 0000	0000 0000	uuuu uuuu
OPTION_REG	1111 1111	1111 1111	uuuu uuuu
TRISA	--11 1111	--11 1111	--uu uuuu
TRISB	1111 1111	1111 1111	uuuu uuuu
PIE1	-0-- -000	-0-- -000	-u-- -uuu
PCON	---- --qq	---- --uu	---- --uu
PR2	1111 1111	1111 1111	uuuu uuuu
ADCON1	---- -000	---- -000	---- -uuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 9-5 for Reset value for specific condition.

4: On any device Reset, these pins are configured as inputs.

5: This is the value that will be in the port output latch.

6: Output latches are unknown or unchanged. Analog inputs default to analog and read '0'.

FIGURE 9-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD})

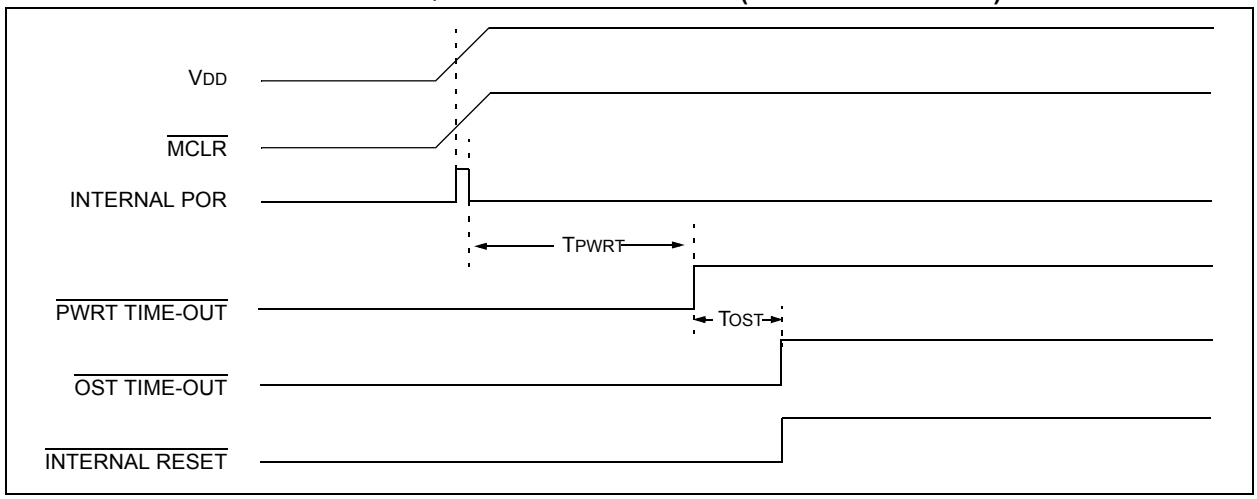


FIGURE 9-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD}): CASE 1

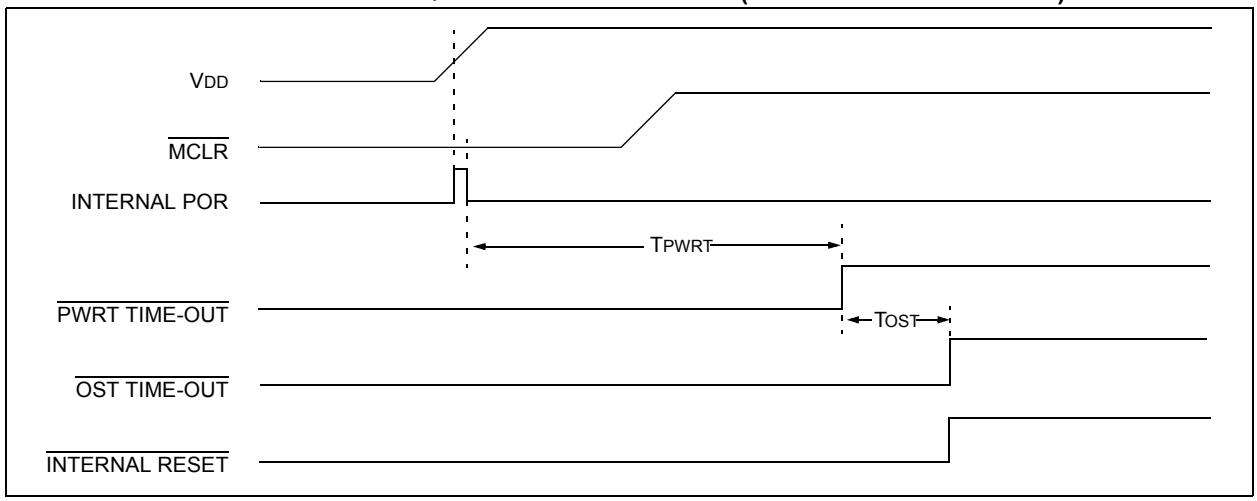
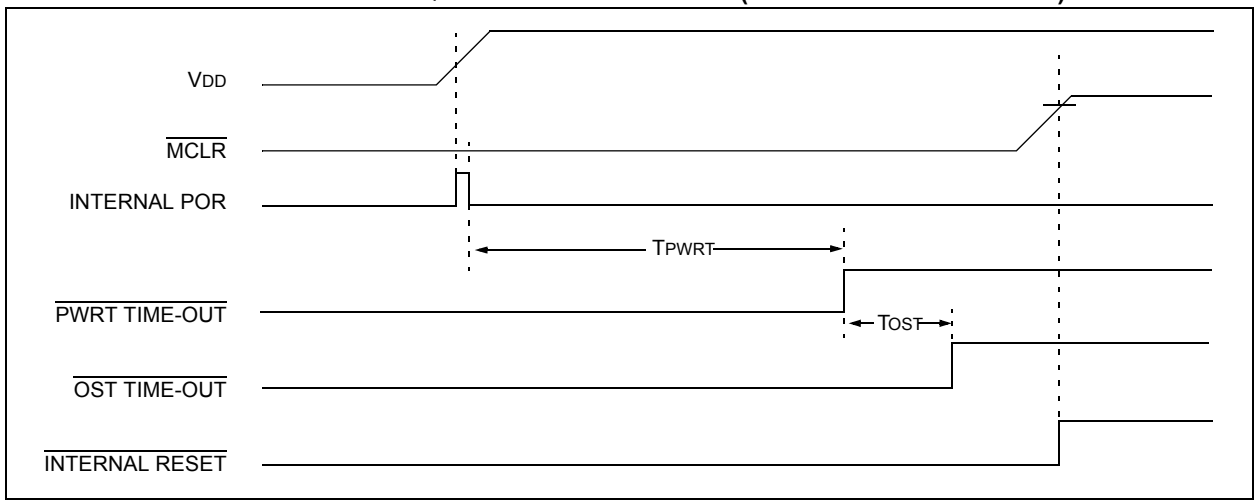


FIGURE 9-12: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD}): CASE 2



9.10.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered, either rising if bit INTEDG of the OPTION register is set, or falling if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF of the INTCON register is set. This interrupt can be disabled by clearing enable bit INTE of the INTCON register. Flag bit INTF must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from Sleep, if bit INTE was set prior to going into Sleep. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See **Section 9.13 "Power-down Mode (Sleep)"** for details on Sleep mode.

9.10.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set flag bit T0IF of the INTCON register. The interrupt can be enabled/disabled by setting/clearing enable bit T0IE of the INTCON register. (**Section 4.0 "Timer0 Module"**).

9.10.3 PORTB INTCON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF of the INTCON register. The interrupt can be enabled/disabled by setting/clearing enable bit RBIE of the INTCON register. (**Section 3.2 "PORTB and the TRISB Register"**).

9.11 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt, (i.e., W register and STATUS register). This will have to be implemented in firmware.

Example 9-1 stores and restores the W, STATUS, PCLATH and FSR registers. Context storage registers, W_TEMP, STATUS_TEMP, PCLATH_TEMP and FSR_TEMP, must be defined in Common RAM which are those addresses between 70h-7Fh in Bank 0 and between F0h-FFh in Bank 1.

The example:

a) Stores the W register.
b) Stores the STATUS register in Bank 0.
c) Stores the PCLATH register.
d) Stores the FSR register.
e) Executes the Interrupt Service Routine code (User-generated).
f) Restores all saved registers in reverse order from which they were stored.

EXAMPLE 9-1: SAVING STATUS, W, AND PCLATH REGISTERS IN RAM

```
MOVWF      W_TEMP           ;Copy W to TEMP register, could be bank one or zero
SWAPF      STATUS,W         ;Swap status to be saved into W
MOVWF      STATUS_TEMP      ;Save status to bank zero STATUS_TEMP register
MOVF       PCLATH, W        ;Only required if using pages 1, 2 and/or 3
MOVWF      PCLATH_TEMP      ;Save PCLATH into W
CLRF       PCLATH           ;Page zero, regardless of current page
BCF        STATUS, IRP      ;Return to Bank 0
MOVF       FSR, W           ;Copy FSR to W
MOVWF      FSR_TEMP         ;Copy FSR from W to FSR_TEMP
:
:(ISR)
:
MOVF       FSR_TEMP,W       ;Restore FSR
MOVWF      FSR              ;Move W into FSR
MOVF       PCLATH_TEMP, W   ;Restore PCLATH
MOVWF      PCLATH           ;Move W into PCLATH
SWAPF      STATUS_TEMP,W    ;Swap STATUS_TEMP register into W
MOVWF      STATUS           ;Move W into STATUS register
SWAPF      W_TEMP,F         ;Swap W_TEMP
SWAPF      W_TEMP,W         ;Swap W_TEMP into W
RETFIE                      ;Return from interrupt and enable GIE
```

9.12 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip, RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device have been stopped, for example, by execution of a SLEEP instruction.

During normal operation, a WDT time-out generates a device Reset (Watchdog Timer Reset). If the device is in Sleep mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

The WDT can be permanently disabled by clearing Configuration bit WDTE (**Section 9.1 "Configuration Bits"**).

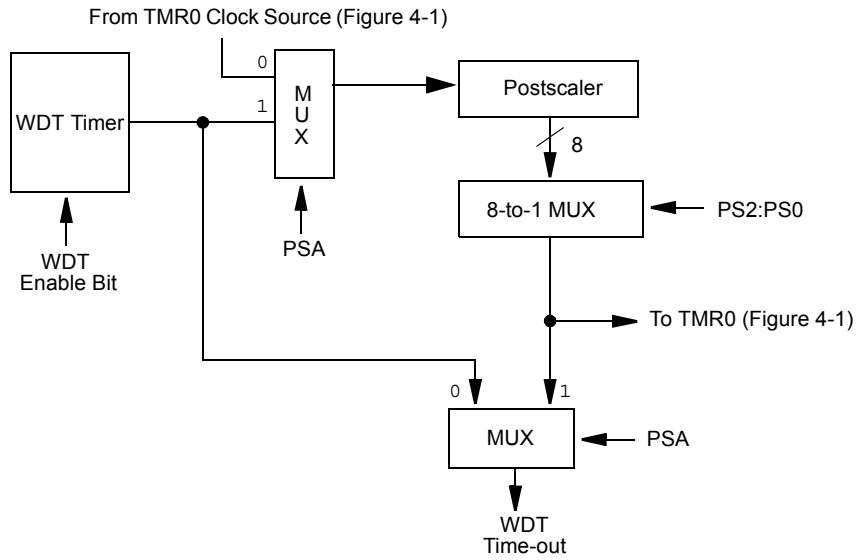
WDT time-out period values may be found in the Electrical Specifications section under TWDT (parameter #31). Values for the WDT prescaler (actually a postscaler, but shared with the Timer0 prescaler) may be assigned using the OPTION register.

Note:	The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device Reset condition.

.

Note:	When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

FIGURE 9-14: WATCHDOG TIMER BLOCK DIAGRAM



Note: PSA and PS2:PS0 are bits in the OPTION register.

TABLE 9-7: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CONFIG1(1)	BORV	BOREN	—	—	$\overline{PWRTE}$	WDTE	FOSC1	FOSC0	—	—
OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used the Watchdog Timer.
Note 1: See Configuration Word Register (Register 9-1) for operation of all register bits.

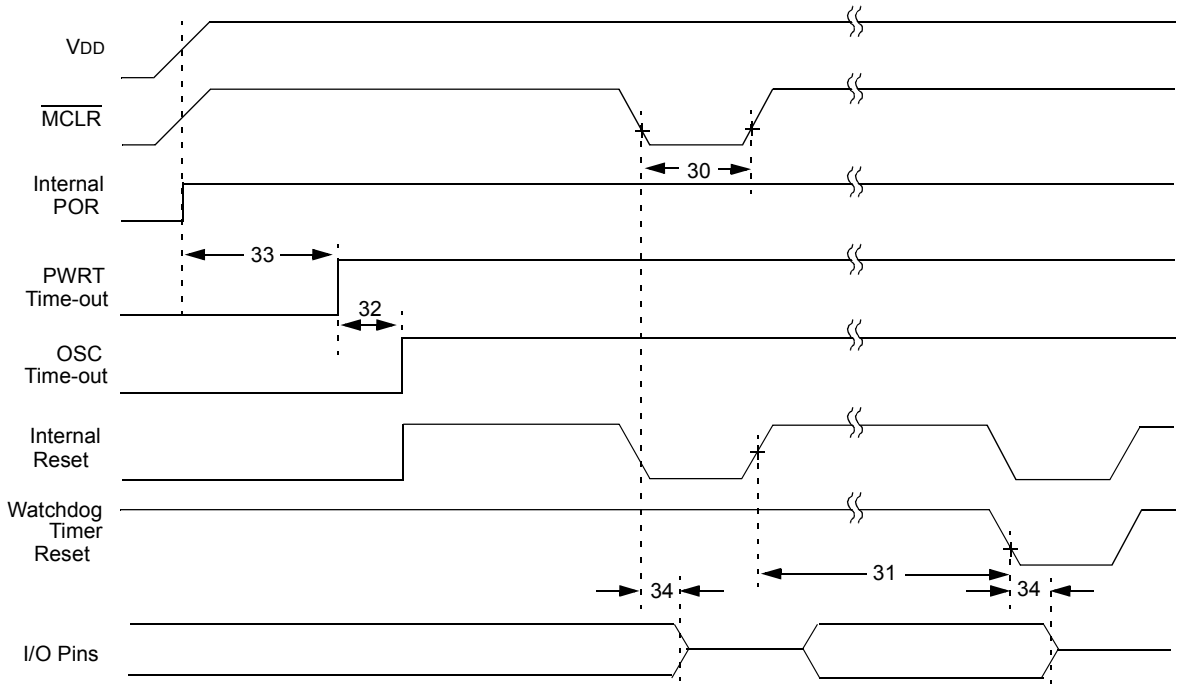
12.2 DC Characteristics: PIC16F716 (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C					
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**VDD**	**Conditions**
D001	VDD	**Supply Voltage**						
			2.0	—	5.5	V	—	
D010	IDD	**Supply Current**						
			—	14	17	µA	2.0	FOSC = 32 kHz LP Oscillator mode
			—	23	28	µA	3.0	
			—	45	63.7	µA	5.0	
D011			—	120	160	µA	2.0	FOSC = 1 MHz XT Oscillator mode
			—	180	250	µA	3.0	
			—	290	370	µA	5.0	
D012			—	220	300	µA	2.0	FOSC = 4 MHz XT Oscillator mode
			—	350	470	µA	3.0	
			—	600	780	µA	5.0	
D013			—	2.1	2.9	mA	4.5	FOSC = 20 MHz HS Oscillator mode
			—	2.5	3.3	mA	5.0	
D020	IPD	**Power-down Base Current**						
			—	0.1	0.8	µA	2.0	WDT, BOR and T1OSC: disabled
			—	0.1	0.85	µA	3.0	
			—	0.2	2.7	µA	5.0	
D021		**Peripheral Module Current(1)**						
			—	1	2.0	µA	2.0	WDT Current
			—	2	3.5	µA	3.0	
			—	9	13.5	µA	5.0	
D022			—	37	50	µA	3.0	BOR Current
			—	40	55	µA	4.5	
			—	45	60	µA	5.0	
D025			—	1.8	6	µA	2.0	T1OSC Current
			—	2.6	7.5	µA	3.0	
			—	3.0	9	µA	5.0	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral "Δ" current can be determined by subtracting the base IDD or IPD current from this limit.

FIGURE 12-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING(1)



Note 1: Refer to Figure 12-3 for load conditions.

FIGURE 12-7: BROWN-OUT RESET TIMING

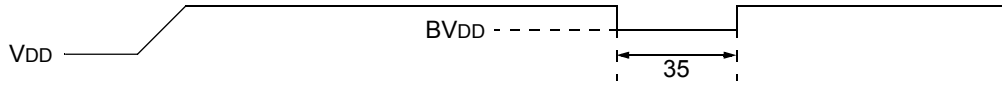


TABLE 12-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TMCL	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	µs	VDD = 5V, -40°C to +125°C
31*	TWDT	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
			TBD	TBD	TBD	ms	VDD = 5V, +85°C to +125°C
32	TOST	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	TPWRT	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +85°C
			TBD	TBD	TBD	ms	VDD = 5V, +85°C to +125°C
34	TIOZ	I/O high-impedance from $\overline{\text{MCLR}}$ Low or WDT Reset	—	—	2.1	µs	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	µs	VDD ≤ BVDD (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-17: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)

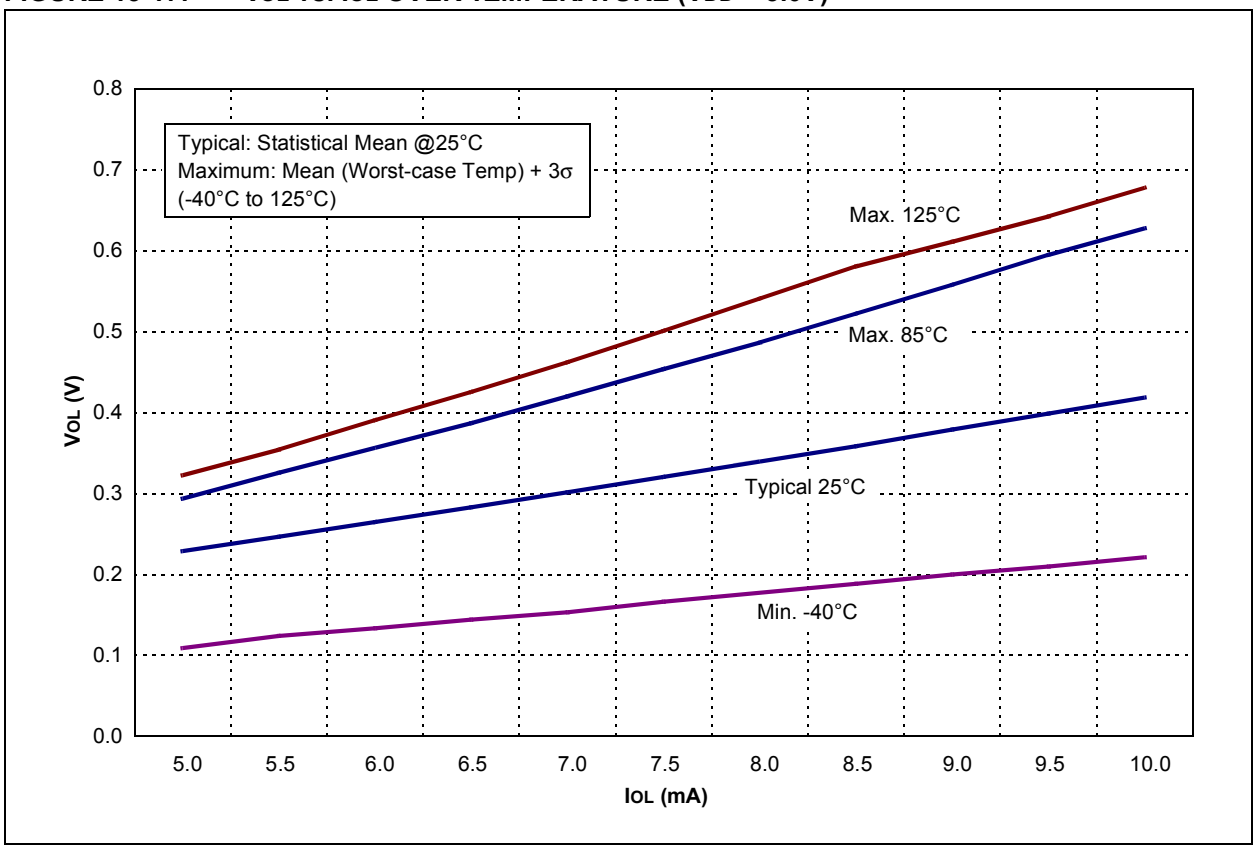


FIGURE 13-18: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)

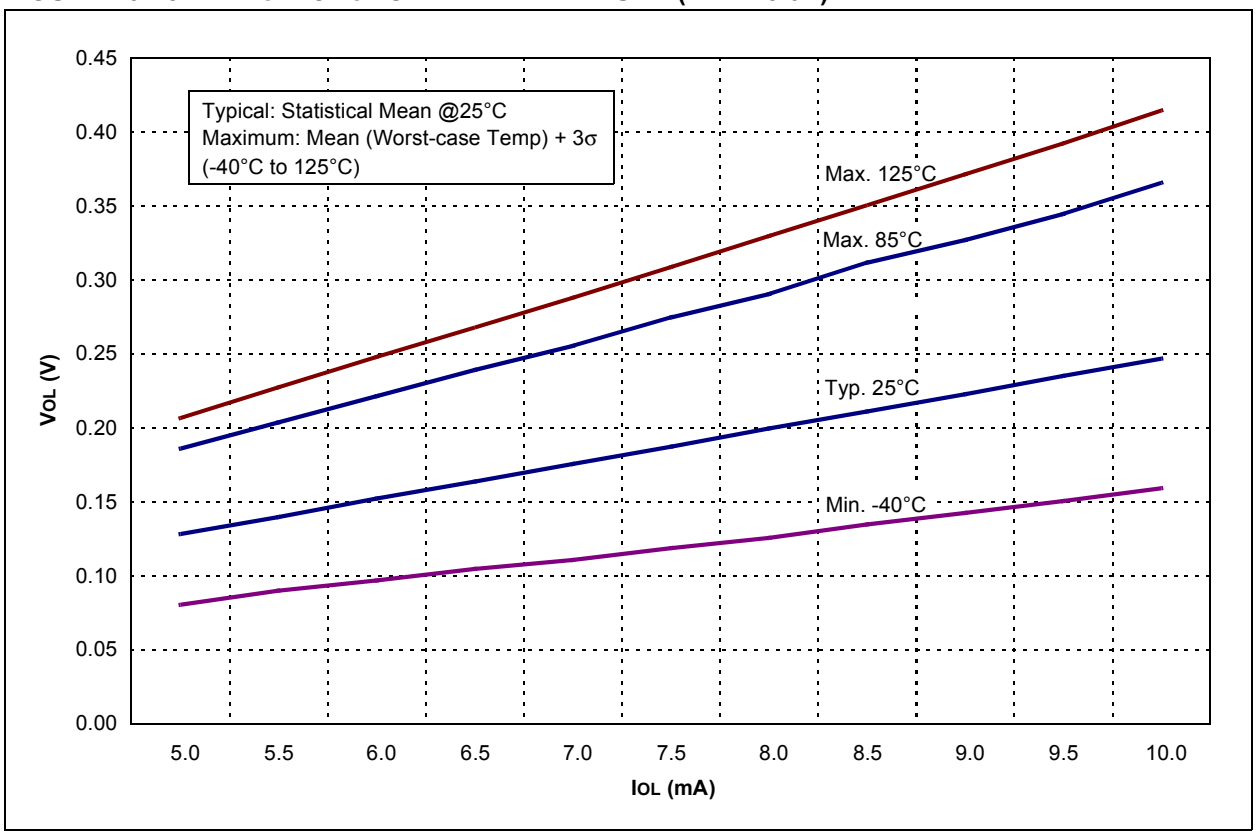


FIGURE 13-23: T1OSC IPD vs. VDD OVER TEMPERATURE (32 kHz)

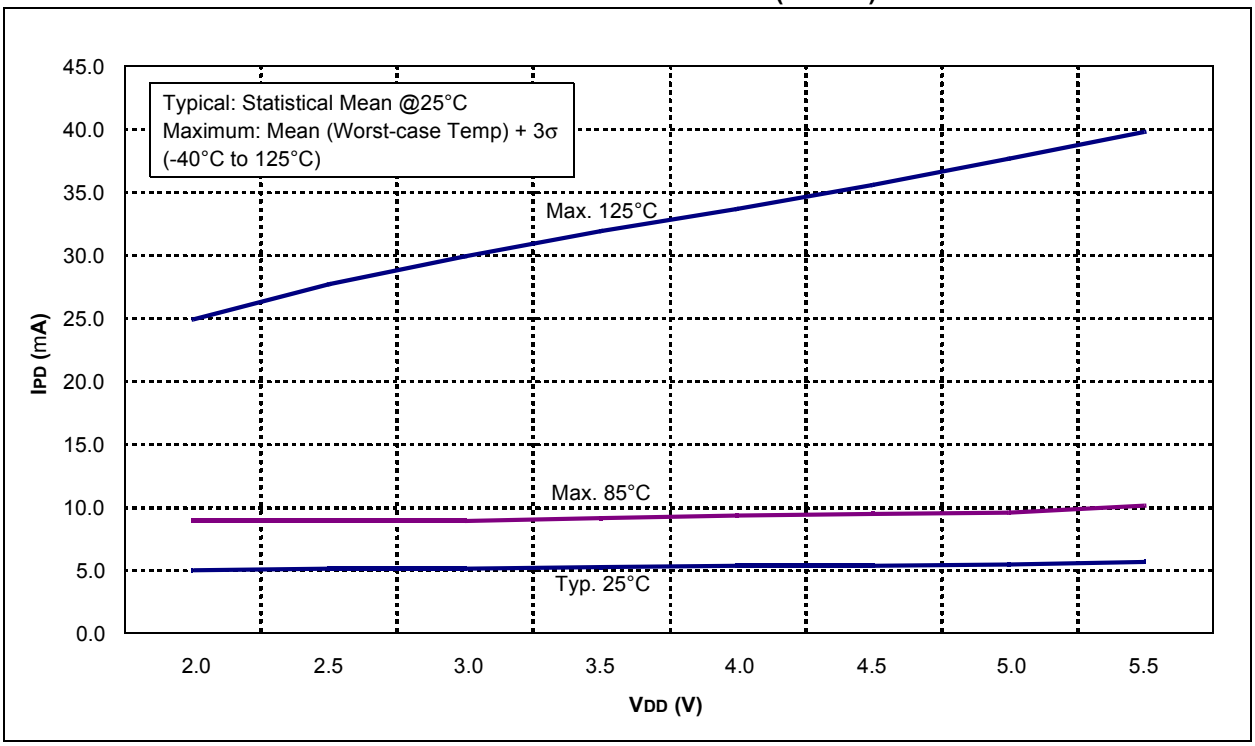
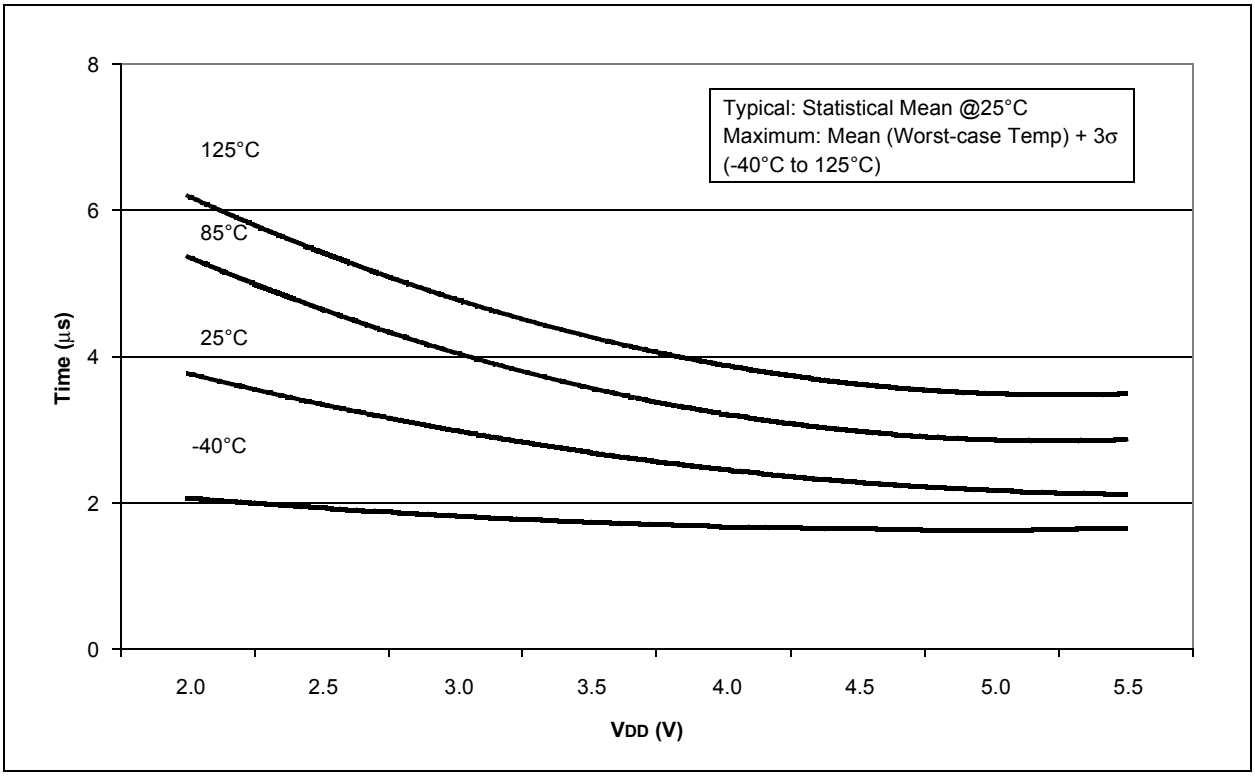


FIGURE 13-24: ADC CLOCK PERIOD vs. VDD OVER TEMPERATURE



PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC16F716[1], PIC16F716T[2]; VDD range 2.0V to 5.5V	
Temperature Range:	I = -40°C to +85°C	(Industrial)
	E = -40°C to +125°C	(Extended)
Package:	SO = SOIC	
	P = PDIP	
	SS = SSOP	
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16F716 - I/L 301 = Industrial temp., PDIP package, QTP pattern #301.

b) PIC16F716 - E/SO = Extended temp., SOIC package.

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range

2: T = in tape and reel SOIC and SSOP packages only.

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