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## What is "Embedded - Microcontrollers"?

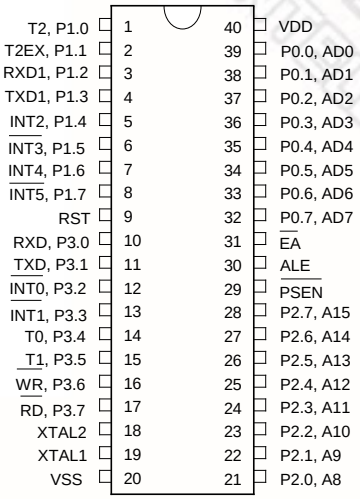
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

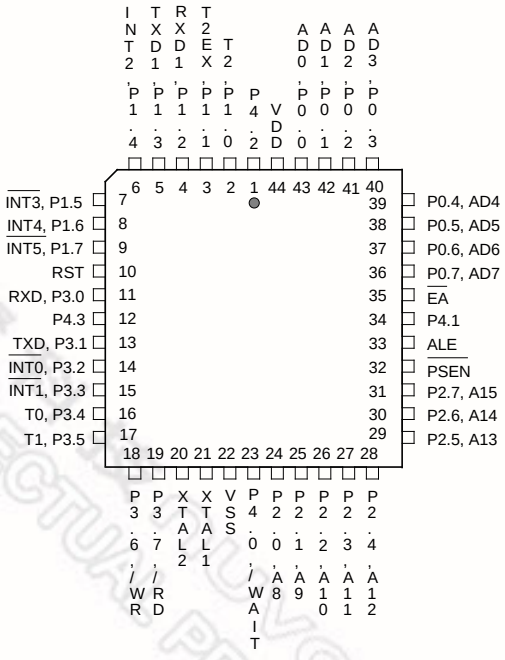
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 40MHz |
| Connectivity | EBI/EMI, Serial Port |
| Peripherals | POR, WDT |
| Number of I/O | 36 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-BQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w77c032a40fl |

## 3. PIN CONFIGURATIONS

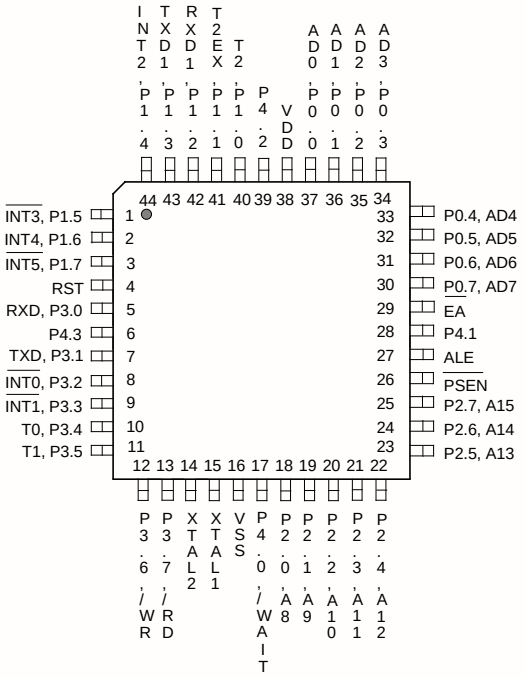
40-Pin DIP




44-Pin PLCC




44-Pin QFP



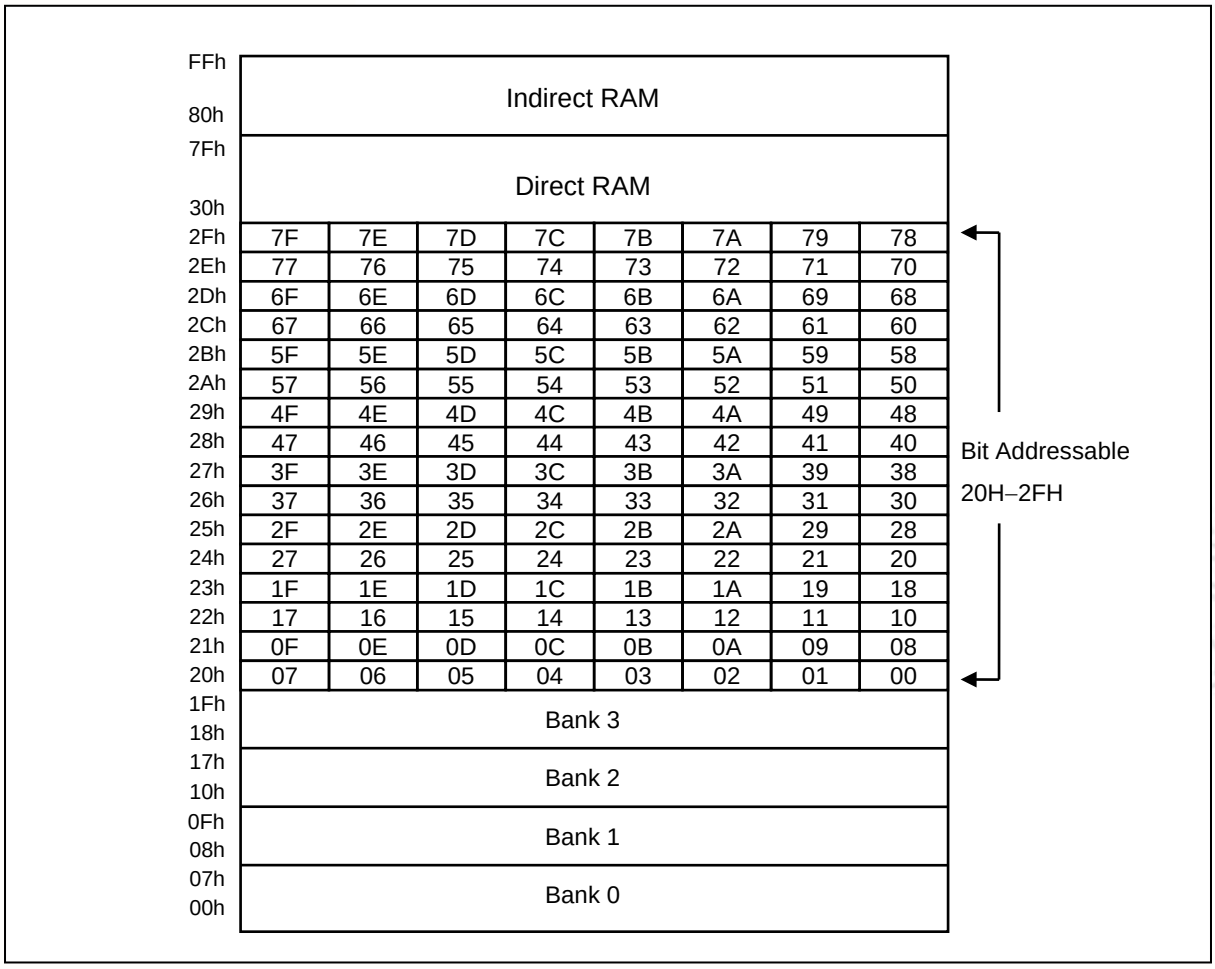



Figure 2. Scratchpad RAM / Register Addressing

MD2-0: Stretch MOVX select bits: These three bits are used to select the stretch value for the MOVX instruction. Using a variable MOVX length enables the user to access slower external memory devices or peripherals without the need for external circuits. The $\overline{RD}$ or $\overline{WR}$ strobe will be stretched by the selected interval. When accessing the on-chip SRAM, the MOVX instruction is always in 2 machine cycles regardless of the stretch setting. By default, the stretch has value of 1. If the user needs faster accessing, then a stretch value of 0 should be selected.

| MD2 | MD1 | MD0 | Stretch value | MOVX duration |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 2 machine cycles |
| 0 | 0 | 1 | 1 | 3 machine cycles *(Default)* |
| 0 | 1 | 0 | 2 | 4 machine cycles |
| 0 | 1 | 1 | 3 | 5 machine cycles |
| 1 | 0 | 0 | 4 | 6 machine cycles |
| 1 | 0 | 1 | 5 | 7 machine cycles |
| 1 | 1 | 0 | 6 | 8 machine cycles |
| 1 | 1 | 1 | 7 | 9 machine cycles |

**Port 1**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | P1.7 | P1.6 | P1.5 | P1.4 | P1.3 | P1.2 | P1.1 | P1.0 |

Mnemonic: P1 Address: 90h

P1.7-0: General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. Some pins also have alternate input or output functions. This alternate functions are described below:

P1.0: T2 External I/O for Timer/Counter 2
P1.1: T2EX Timer/Counter 2 Capture/Reload Trigger
P1.2: RXD1 Serial Port 1 Receive
P1.3: TXD1 Serial Port 1 Transmit
P1.4: INT2 External Interrupt 2
P1.5: $\overline{INT3}$ External Interrupt 3
P1.6: INT4 External Interrupt 4
P1.7: $\overline{INT5}$ External Interrupt 5

comparison. This register enables the Automatic Address Recognition feature of the Serial port 1. When all the bits of SADEN1 are 0, interrupt will occur for any incoming address.

**Serial Port Control 1**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SM0_1/FE_1 | SM1_1 | SM2_1 | REN_1 | TB8_1 | RB8_1 | TI_1 | RI_1 |

Mnemonic: SCON1 Address: C0h

SM0_1/FE_1: Serial port 1, Mode 0 bit or Framing Error Flag 1: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0_1 or as FE_1. the operation of SM0_1 is described below. When used as FE_1, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE_1 condition.

SM1_1: Serial port 1 Mode bit 1:

| SM0_1 | SM1_1 | Mode | Description | Length | Baud rate |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Synchronous | 8 | 4/12 Tclk |
| 0 | 1 | 1 | Asynchronous | 10 | variable |
| 1 | 0 | 2 | Asynchronous | 11 | 64/32 Tclk |
| 1 | 1 | 3 | Asynchronous | 11 | variable |

SM2_1: Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2_1 is set to 1, then RI_1 will not be activated if the received 9$^{th}$ data bit (RB8_1) is 0. In mode 1, if SM2_1 = 1, then RI_1 will not be activated if a valid stop bit was not received. In mode 0, the SM2_1 bit controls the serial port 1 clock. If set to 0, then the serial port 1 runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.

REN_1: Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.

TB8_1: This is the 9$^{th}$ bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.

RB8_1: In modes 2 and 3 this is the received 9$^{th}$ data bit. In mode 1, if SM2_1 = 0, RB8_1 is the stop bit that was received. In mode 0 it has no function.

TI_1: Transmit interrupt flag: This flag is set by hardware at the end of the 8$^{th}$ bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

RI_1: Receive interrupt flag: This flag is set by hardware at the end of the 8$^{th}$ bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2_1 apply to this bit. This bit can be cleared only by software

**Serial Data Buffer 1**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SBUF1.7 | SBUF1.6 | SBUF1.5 | SBUF1.4 | SBUF1.3 | SBUF1.2 | SBUF1.1 | SBUF1.0 |

Mnemonic: SBUF1 Address: C1h

SBUF1.7-0: Serial data of the serial port 1 is read from or written to this location. It actually consists of two separate 8-bit registers. One is the receive resister, and the other is the transmit

| RS1 | RS0 | Register bank | Address |
|---|---|---|---|
| 0 | 0 | 0 | 00-07h |
| 0 | 1 | 1 | 08-0Fh |
| 1 | 0 | 2 | 10-17h |
| 1 | 1 | 3 | 18-1Fh |

OV: Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.

F1: User Flag 1: General purpose flag that can be set or cleared by the user by software

P: Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

**Watchdog Control**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SMOD_1 | POR | - | - | WDIF | WTRF | EWT | RWT |

Mnemonic: WDCON Address: D8h

SMOD_1:This bit doubles the Serial Port 1 baud rate in mode 1, 2, and 3 when set to 1.

POR: Power-on reset flag. Hardware will set this flag on a power up condition. This flag can be read or written by software. A write by software is the only way to clear this bit once it is set.

WDIF: Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software.

WTRF: Watchdog Timer Reset Flag. Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the watchdog timer will have no affect on this bit.

EWT: Enable Watchdog timer Reset. Setting this bit will enable the Watchdog timer Reset function.

RWT: Reset Watchdog Timer. This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the RWT before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWT is set. This bit is self-clearing by hardware.

The WDCON SFR is set to a 0x0x0xx0b on an external reset. WTRF is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is set to 0 on a Power-on reset and unaffected by other resets.

All the bits in this SFR have unrestricted read access. POR, EWT, WDIF and RWT require Timed Access procedure to write. The remaining bits have unrestricted write accesses.

Table 3. Instruction Timing for W77C032, continued

| INSTRUCTION | HEX OP-CODE | BYTES | W77C032 MACHINE CYCLES | W77C032 CLOCK CYCLES | 8032 CLOCK CYCLES | W77C032 VS. 8032 SPEED RATIO |
|---|---|---|---|---|---|---|
| JNB bit, rel | 30 | 3 | 4 | 16 | 24 | 1.5 |
| JBC bit, rel | 10 | 3 | 4 | 16 | 24 | 1.5 |
| LCALL addr16 | 12 | 3 | 4 | 16 | 24 | 1.5 |
| LJMP addr16 | 02 | 3 | 4 | 16 | 24 | 1.5 |
| MUL AB | A4 | 1 | 5 | 20 | 48 | 2.4 |
| MOV A, R0 | E8 | 1 | 1 | 4 | 12 | 3 |
| MOV A, R1 | E9 | 1 | 1 | 4 | 12 | 3 |
| MOV A, R2 | EA | 1 | 1 | 4 | 12 | 3 |
| MOV A, R3 | EB | 1 | 1 | 4 | 12 | 3 |
| MOV A, R4 | EC | 1 | 1 | 4 | 12 | 3 |
| MOV A, R5 | ED | 1 | 1 | 4 | 12 | 3 |
| MOV A, R6 | EE | 1 | 1 | 4 | 12 | 3 |
| MOV A, R7 | EF | 1 | 1 | 4 | 12 | 3 |
| MOV A, @R0 | E6 | 1 | 1 | 4 | 12 | 3 |
| MOV A, @R1 | E7 | 1 | 1 | 4 | 12 | 3 |
| MOV A, direct | E5 | 2 | 2 | 8 | 12 | 1.5 |
| MOV A, #data | 74 | 2 | 2 | 8 | 12 | 1.5 |
| MOV R0, A | F8 | 1 | 1 | 4 | 12 | 3 |
| MOV R1, A | F9 | 1 | 1 | 4 | 12 | 3 |
| MOV R2, A | FA | 1 | 1 | 4 | 12 | 3 |
| MOV R3, A | FB | 1 | 1 | 4 | 12 | 3 |
| MOV R4, A | FC | 1 | 1 | 4 | 12 | 3 |
| MOV R5, A | FD | 1 | 1 | 4 | 12 | 3 |
| MOV R6, A | FE | 1 | 1 | 4 | 12 | 3 |
| MOV R7, A | FF | 1 | 1 | 4 | 12 | 3 |
| MOV R0, direct | A8 | 2 | 2 | 8 | 12 | 1.5 |
| MOV R1, direct | A9 | 2 | 2 | 8 | 12 | 1.5 |
| MOV R2, direct | AA | 2 | 2 | 8 | 12 | 1.5 |
| MOV R3, direct | AB | 2 | 2 | 8 | 12 | 1.5 |
| MOV R4, direct | AC | 2 | 2 | 8 | 12 | 1.5 |
| MOV R5, direct | AD | 2 | 2 | 8 | 12 | 1.5 |
| MOV R2, #data | 7A | 2 | 2 | 8 | 12 | 1.5 |
| MOV R3, #data | 7B | 2 | 2 | 8 | 12 | 1.5 |
| MOV R4, #data | 7C | 2 | 2 | 8 | 12 | 1.5 |
| MOV R5, #data | 7D | 2 | 2 | 8 | 12 | 1.5 |
| MOV R6, #data | 7E | 2 | 2 | 8 | 12 | 1.5 |
| MOV R7, #data | 7F | 2 | 2 | 8 | 12 | 1.5 |
| MOV @R0, A | F6 | 1 | 1 | 4 | 12 | 3 |
| MOV @R1, A | F7 | 1 | 1 | 4 | 12 | 3 |

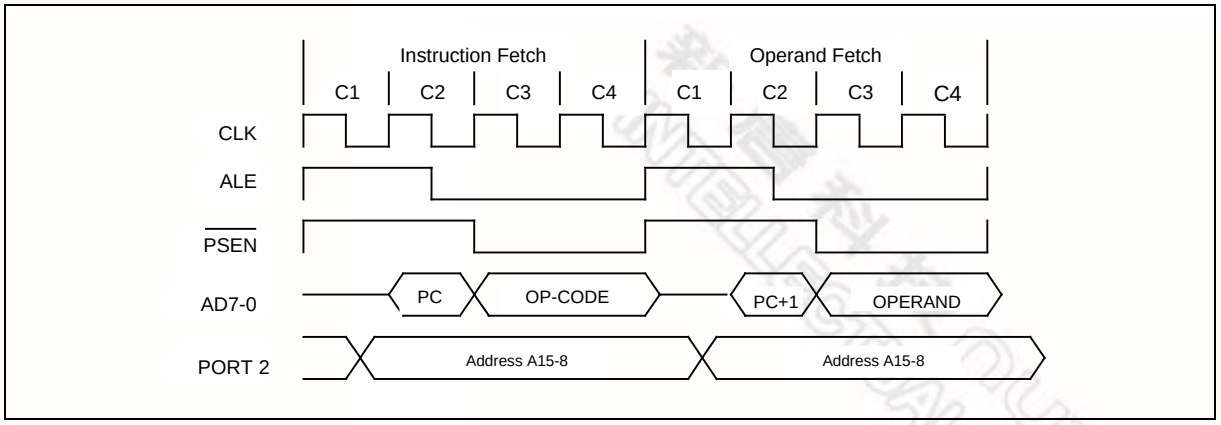



Figure 4: Two Cycle Instruction Timing

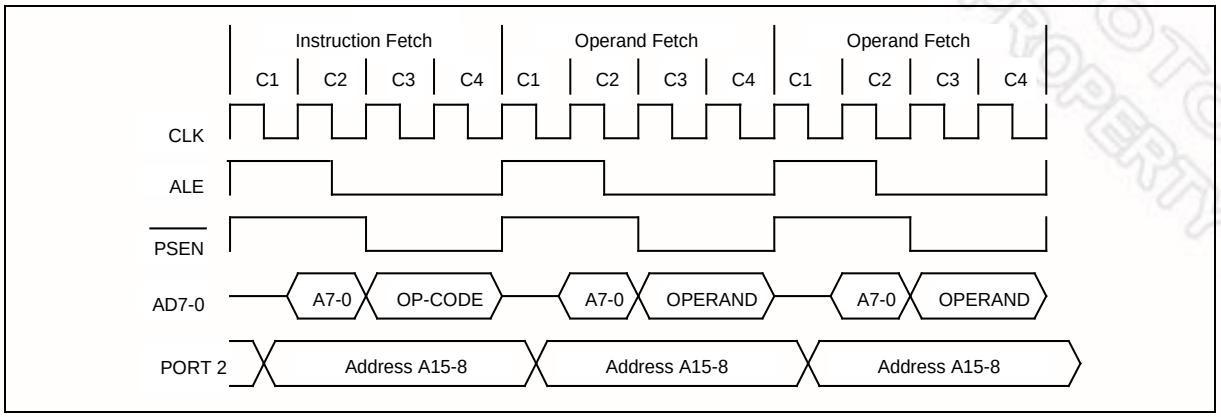



Figure 5: Three Cycle Instruction Timing

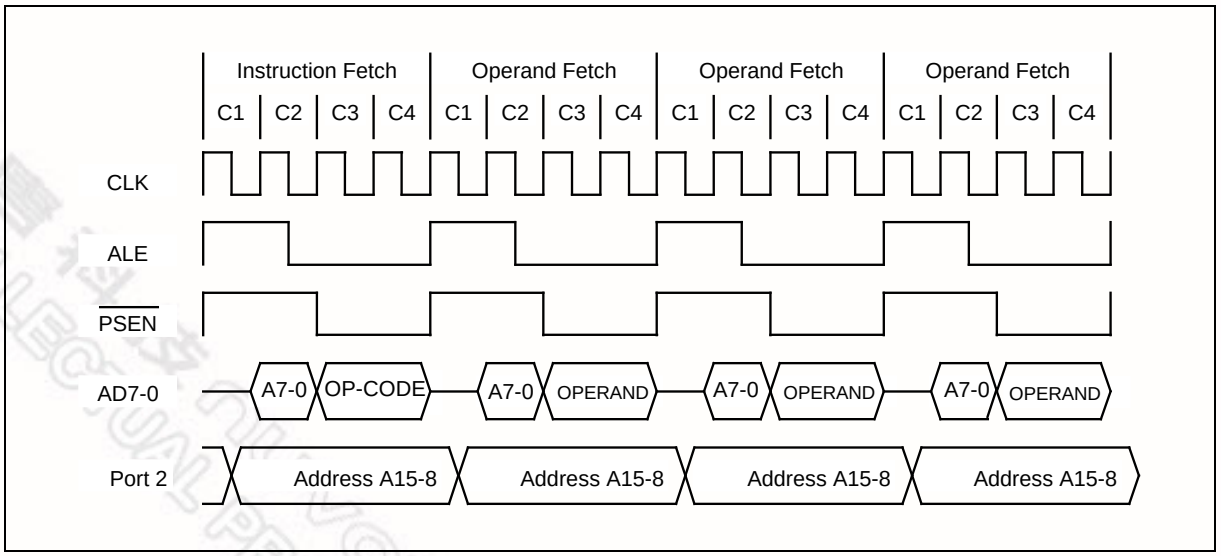



Figure 6: Four Cycle Instruction Timing

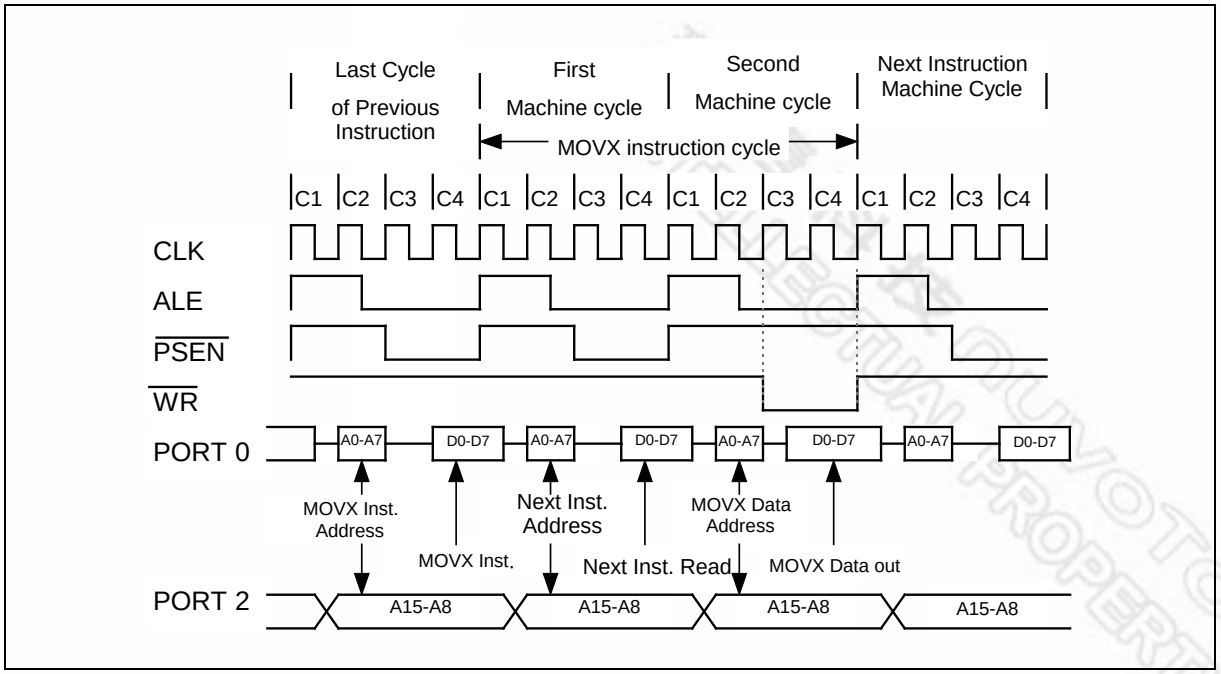



Figure 8: Data Memory Write with Stretch Value = 0

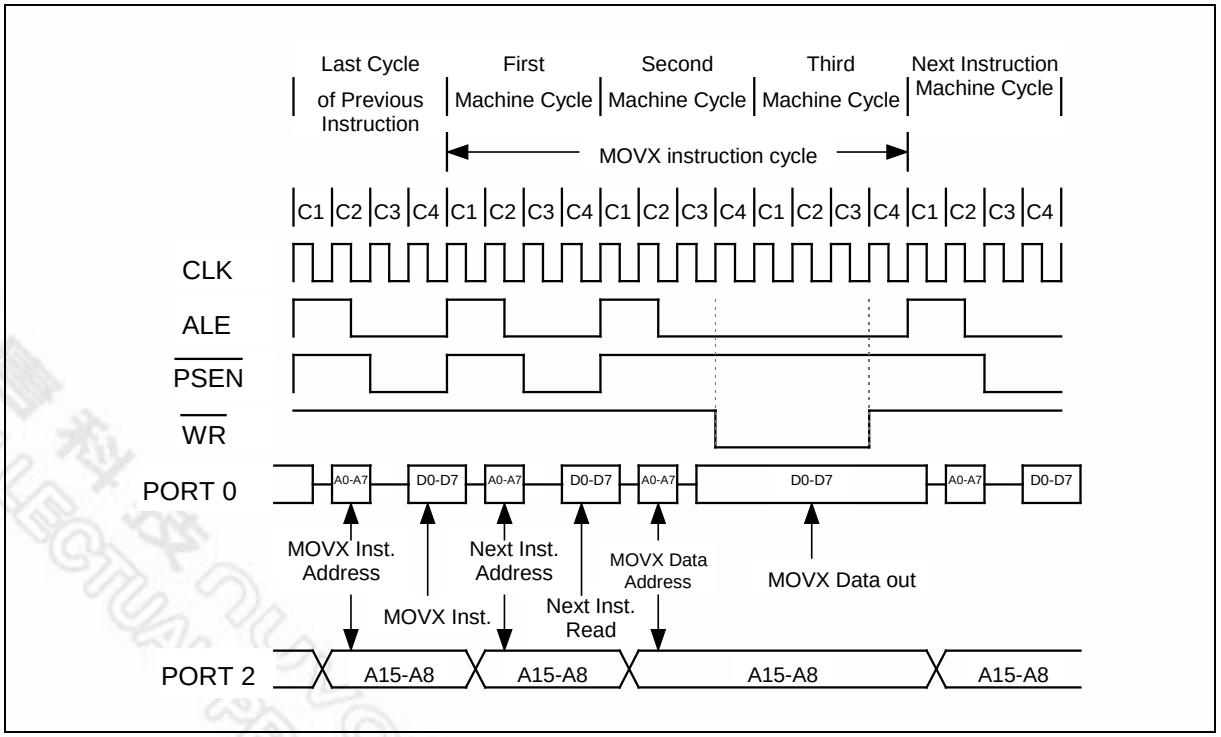



Figure 9: Dada Memory Write with Stretch Value = 1

## 10. RESET CONDITIONS

The user has several hardware related options for placing the W77C032 into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software. There are three ways of putting the device into reset state. They are External reset, Power on/fail reset and Watchdog reset.

### 10.1 External Reset

The device continuously samples the RST pin at state C4 of every machine cycle. Therefore the RST pin must be held for at least 2 machine cycles to ensure detection of a valid RST high. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as RST is 1. Even after RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition. However since the other two reset sources have flags, the external reset can be considered as the default reset if those two flags are cleared.

### 10.2 Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag is set. If the Watchdog reset is enabled and the watchdog timer is not cleared, then 512 clocks from the flag being set, the watchdog timer will generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h.

### 10.3 Reset State

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the $V_{DD}$ falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost. Hence it should be assumed that after a power on reset, POR = 1, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The port SFRs have FFh written into them which puts the port pins in a high state. Port 0 floats as it does not have on-chip pull-ups.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the W77C032 is performing a write to IE, IP, EIE or EIP and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine cycles. This includes 1 machine cycle to detect the interrupt, 2 machine cycles to complete the IE, IP, EIE or EIP access, 5 machine cycles to complete the MUL or DIV instruction and 4 machine cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine cycles and not more than 12 machine cycles. The maximum latency of 12 machine cycle is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine cycles which equals 96 machine cycles. This is a 50% reduction in terms of clock periods.

### 12.1.2 Mode 0

In Mode 0, the timer/counters act as a 8 bit counter with a 5 bit, divide by 32 pre-scale. In this mode we have a 13 bit timer/counter. The 13 bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock increments the count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When the count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set and either GATE = 0 or $\overline{INTx}$ = 1. When C/$\overline{T}$ is set to 0, then it will count clock cycles, and if C/$\overline{T}$ is set to 1, then it will count 1 to 0 transitions on T0 (P3.4) for timer 0 and T1 (P3.5) for timer 1. When the 13 bit count reaches 1FFFh the next count will cause it to roll-over to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupts will occur. Note that when used as a timer, the time-base may be either clock cycles/12 or clock cycles/4 as selected by the bits TxM of the CKCON SFR.

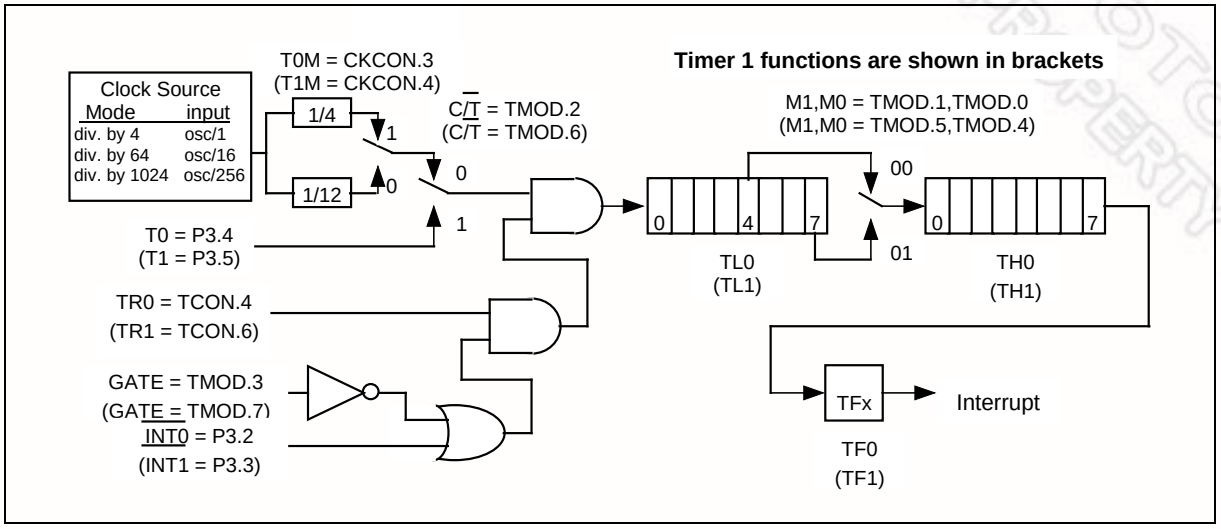



Figure 11: Timer/Counter Mode 0 & Mode 1

### 12.1.3 Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16 bit counter, rather than a 13 bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

### 12.1.4 Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as a 8 bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$ pins. As in the other two modes 0 and 1, mode 2 allows counting of either clock cycles (clock/12 or clock/4) or pulses on pin Tn.

## 12.2 Timer/Counter 2

Timer/Counter 2 is a 16 bit up/down counter which is configured by the T2MOD register and controlled by the T2CON register. Timer/Counter 2 is equipped with a capture/reload capability. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock, and in defining the operating mode. The clock source for Timer/Counter 2 may be selected for either the external T2 pin (C/$\overline{T2}$ = 1) or the crystal oscillator, which is divided by 12 or 4 (C/$\overline{T2}$ = 0). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

### 12.2.1 Capture Mode

The capture mode is enabled by setting the CP/$\overline{RL2}$ bit in the T2CON register to a 1. In the capture mode, Timer/Counter 2 serves as a 16 bit up counter. When the counter rolls over from FFFFh to 0000h, the TF2 bit is set, which will generate an interrupt request. If the EXEN2 bit is set, then a negative transition of T2EX pin will cause the value in the TL2 and TH2 register to be captured by the RCAP2L and RCAP2H registers. This action also causes the EXF2 bit in T2CON to be set, which will also generate an interrupt. Setting the T2CR bit (T2MOD.3), the W77C032 allows hardware to reset timer 2 automatically after the value of TL2 and TH2 have been captured.

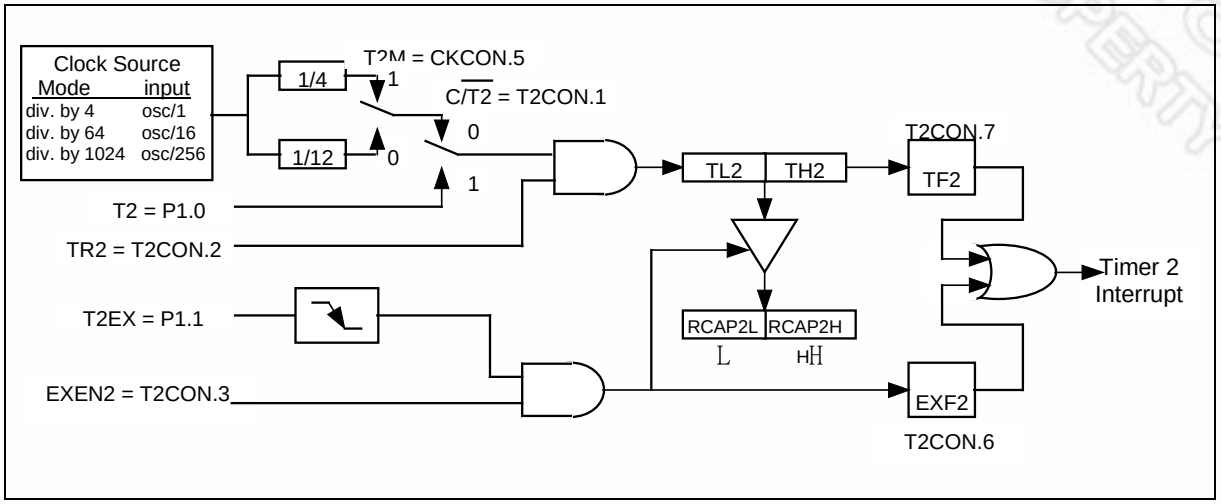



Figure 14. 16-Bit Capture Mode

### 12.2.2 Auto-reload Mode, Counting Up

The auto-reload mode as an up counter is enabled by clearing the CP/$\overline{RL2}$ bit in the T2CON register and clearing the DCEN bit in T2MOD register. In this mode, Timer/Counter 2 is a 16 bit up counter. When the counter rolls over from FFFFh, a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. The reload action also sets the TF2 bit. If the EXEN2 bit is set, then a negative transition of T2EX pin will also cause a reload. This action also sets the EXF2 bit in T2CON.

## 13. WATCHDOG TIMER

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the users software.

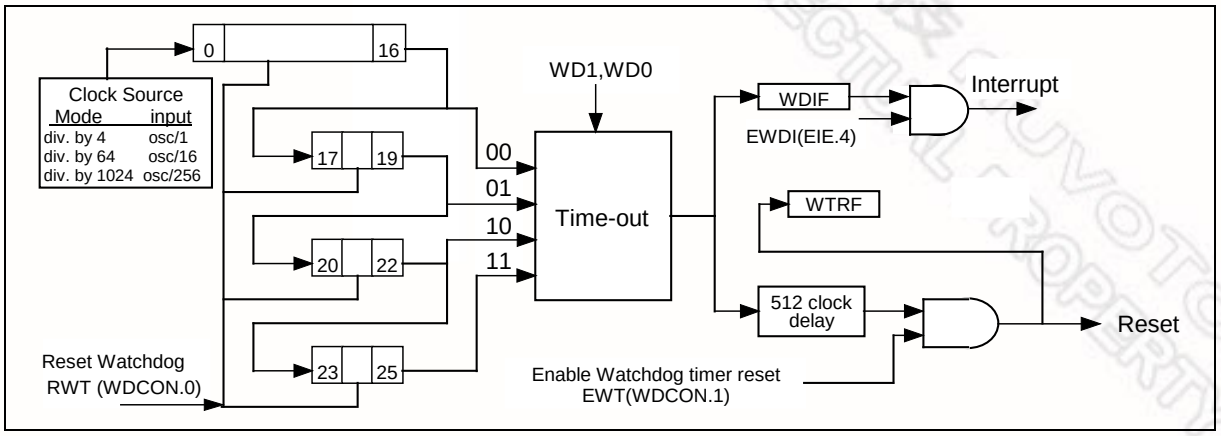



Figure 19. Watchdog Timer

The Watchdog timer should first be restarted by using RWT. This ensures that the timer starts from a known state. The RWT bit is used to restart the watchdog timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The watchdog timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (CKCON.7 and CKCON.6). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the watchdog timer waits for an additional 512 clock cycles. If the Watchdog Reset EWT (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no RWT, a system reset due to Watchdog timer will occur. This will last for two machine cycles, and the Watchdog timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the RWT allows software to restart the timer. The Watchdog timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the watchdog timer which will allow the code to run without any watchdog timer interrupts. Now the watchdog timer reset is enabled and the watchdog interrupt may be disabled,. If any errant code is executed now, then the reset watchdog timer instructions will not be executed at the required instants and watchdog reset will occur.

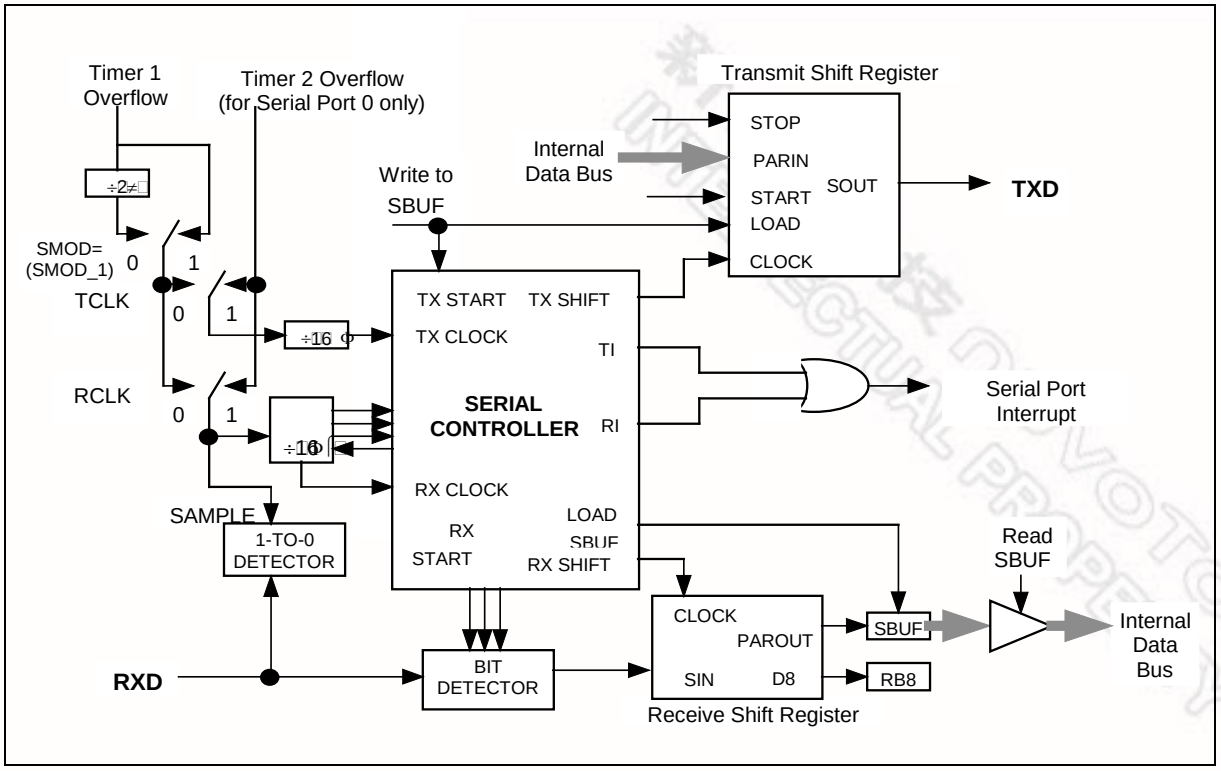



Figure 21: Serial Port Mode

**Mode 2**

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a programmable 9th bit (TB8) and a stop bit (0). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counter after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and

2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

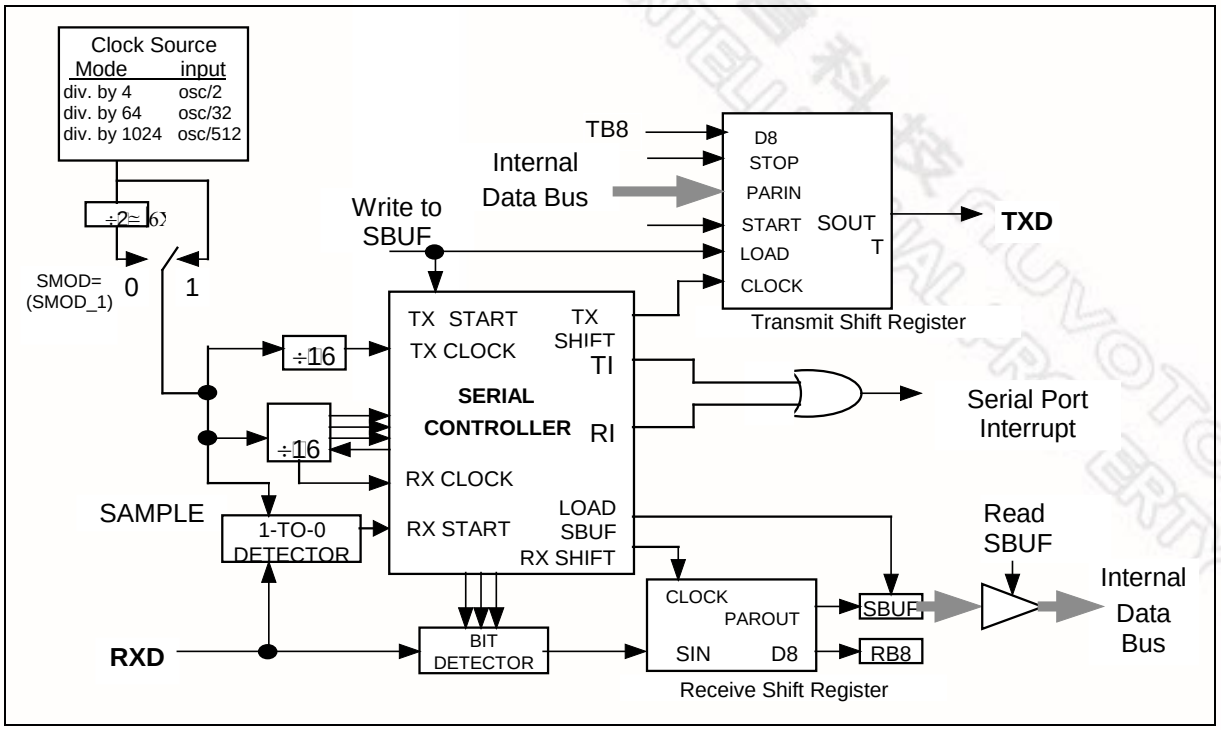



Figure 22. Serial Port Mode 2

### Mode 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

**Table 10. Serial Ports Modes**

| SM1 | SM0 | MODE | TYPE | BAUD CLOCK | FRAME SIZE | START BIT | STOP BIT | 9TH BIT FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Synch. | 4 or 12 TCLKs | 8 bits | No | No | None |
| 0 | 1 | 1 | Asynch. | Timer 1 or 2 | 10 bits | 1 | 1 | None |
| 1 | 0 | 2 | Asynch. | 32 or 64 TCLKs | 11 bits | 1 | 1 | 0, 1 |
| 1 | 1 | 3 | Asynch. | Timer 1 or 2 | 11 bits | 1 | 1 | 0, 1 |

Example 4: Invalid Access

```
MOV  TA, #0Aah   3 M/C
NOP              1 M/C
MOV  TA, #055h   3 M/C
SETB EWT         2 M/C
```

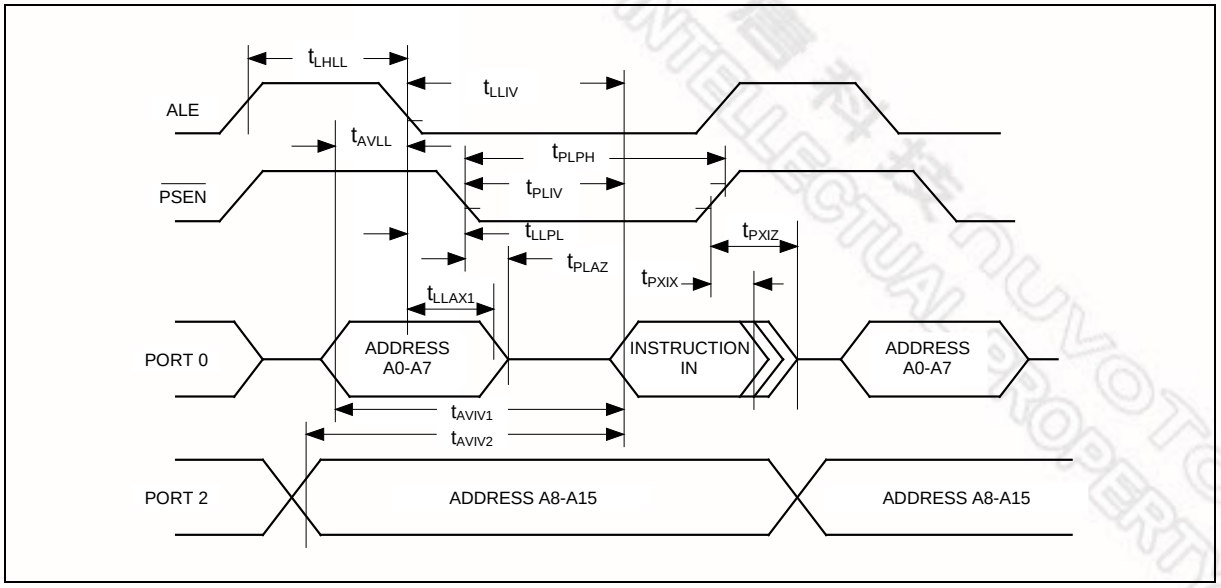
In the first two examples, the writing to the protected bits is done before the 3 machine cycle window closes. In Example 3, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 4, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window in not opened at all, and the write to the protected bit fails.

### 16.3.2 A.C. Specification

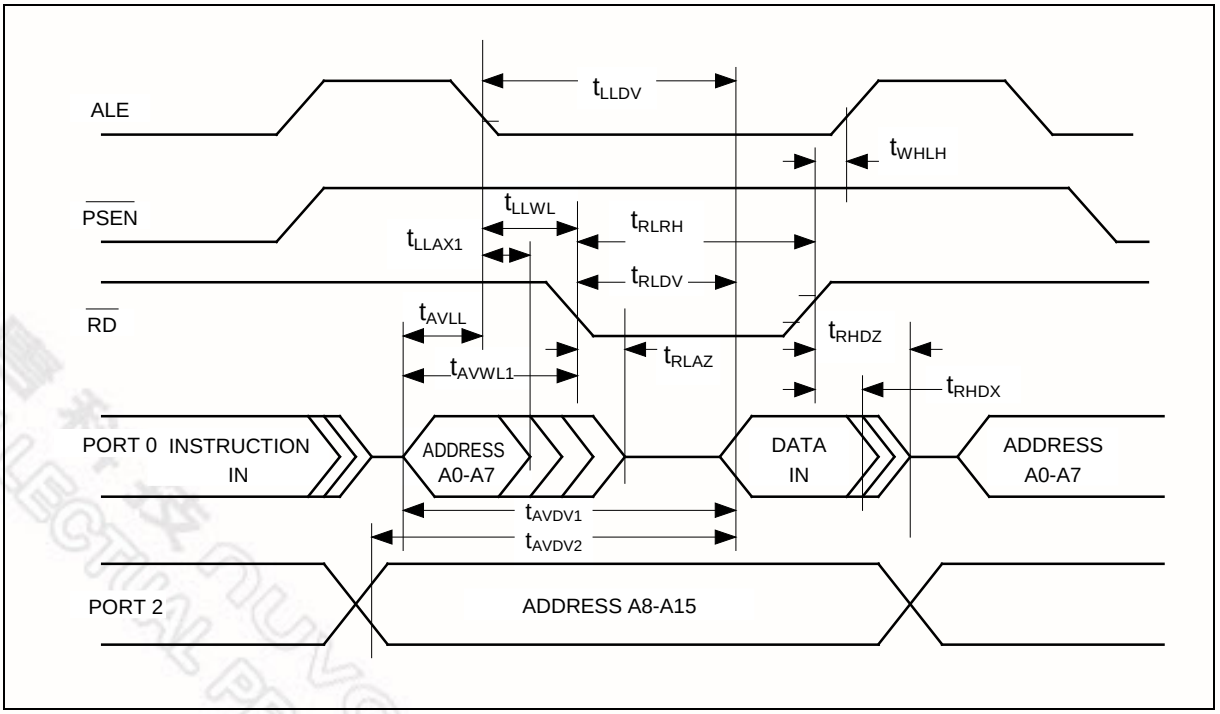
| PARAMETER | SYM. | VARIABLE CLOCK MIN. | VARIABLE CLOCK MAX. | UNITS |
|---|---|---|---|---|
| Oscillator Frequency | $1/t_{CLCL}$ | 0 | 40 | MHz |
| ALE Pulse Width | $t_{LHLL}$ | $1.5\ t_{CLCL} - 5$ | | nS |
| Address Valid to ALE Low | $t_{AVLL}$ | $0.5\ t_{CLCL} - 5$ | | nS |
| Address Hold After ALE Low | $t_{LLAX1}$ | $0.5\ t_{CLCL} - 5$ | | nS |
| Address Hold After ALE Low for MOVX Write | $t_{LLAX2}$ | $0.5\ t_{CLCL} - 5$ | | nS |
| ALE Low to Valid Instruction In | $t_{LLIV}$ | | $2.5\ t_{CLCL} - 20$ | nS |
| ALE Low to PSEN Low | $t_{LLPL}$ | $0.5\ t_{CLCL} - 5$ | | nS |
| $\overline{PSEN}$ Pulse Width | $t_{PLPH}$ | $2.0\ t_{CLCL} - 5$ | | nS |
| $\overline{PSEN}$ Low to Valid Instruction In | $t_{PLIV}$ | | $2.0\ t_{CLCL} - 20$ | nS |
| Input Instruction Hold After PSEN | $t_{PXIX}$ | 0 | | nS |
| Input Instruction Float After PSEN | $t_{PXIZ}$ | | $t_{CLCL} - 5$ | nS |
| Port 0 Address to Valid Instr. In | $t_{AVIV1}$ | | $3.0\ t_{CLCL} - 20$ | nS |
| Port 2 Address to Valid Instr. In | $t_{AVIV2}$ | | $3.5\ t_{CLCL} - 20$ | nS |
| $\overline{PSEN}$ Low to Address Float | $t_{PLAZ}$ | 0 | | nS |
| Data Hold After Read | $t_{RHDX}$ | 0 | | nS |
| Data Float After Read | $t_{RHDZ}$ | | $t_{CLCL} - 5$ | nS |
| $\overline{RD}$ Low to Address Float | $t_{RLAZ}$ | | $0.5\ t_{CLCL} - 5$ | nS |

## 17. TIMING WAVEFORMS

### 17.1 Program Memory Read Cycle




### 17.2 Data Memory Read Cycle



## 18.2 Expanded External Data Memory and Oscillator

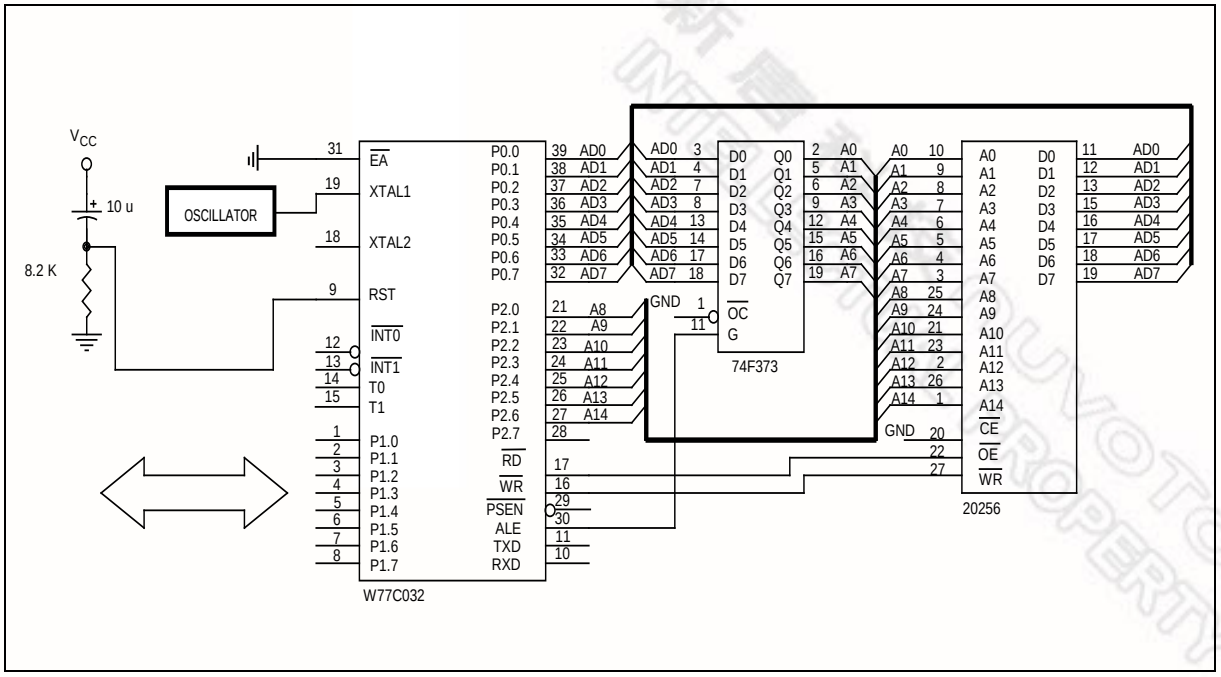
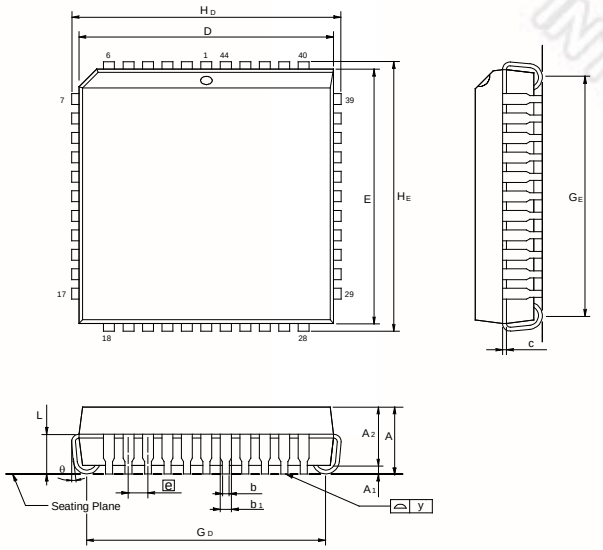



Figure B

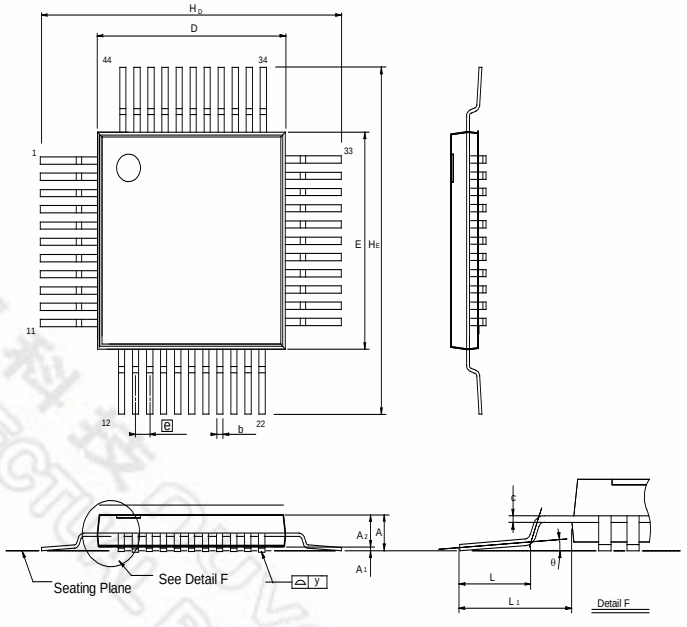
## 19.2 44-pin PLCC




| Symbol | Dimension in inches | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | — | — | 0.185 | — | — | 4.699 |
| $A_1$ | 0.020 | — | — | 0.508 | — | — |
| $A_2$ | 0.145 | 0.150 | 0.155 | 3.683 | 3.81 | 3.937 |
| $b_1$ | 0.026 | 0.028 | 0.032 | 0.66 | 0.711 | 0.813 |
| b | 0.016 | 0.018 | 0.022 | 0.406 | 0.457 | 0.559 |
| c | 0.008 | 0.010 | 0.014 | 0.203 | 0.254 | 0.356 |
| D | 0.648 | 0.653 | 0.658 | 16.46 | 16.59 | 16.71 |
| E | 0.648 | 0.653 | 0.658 | 16.46 | 16.59 | 16.71 |
| e | 0.050 BSC | | | 1.27 BSC | | |
| $G_D$ | 0.590 | 0.610 | 0.630 | 14.99 | 15.49 | 16.00 |
| $G_E$ | 0.590 | 0.610 | 0.630 | 14.99 | 15.49 | 16.00 |
| $H_D$ | 0.680 | 0.690 | 0.700 | 17.27 | 17.53 | 17.78 |
| $H_E$ | 0.680 | 0.690 | 0.700 | 17.27 | 17.53 | 17.78 |
| L | 0.090 | 0.100 | 0.110 | 2.296 | 2.54 | 2.794 |
| y | — | — | 0.004 | — | — | 0.10 |

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

## 19.3 44-pin QFP




| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | --- | --- | --- | --- | --- | --- |
| $A_1$ | 0.002 | 0.01 | 0.02 | 0.05 | 0.25 | 0.5 |
| $A_2$ | 0.075 | 0.081 | 0.087 | 1.90 | 2.05 | 2.20 |
| b | 0.01 | 0.014 | 0.018 | 0.25 | 0.35 | 0.45 |
| c | 0.004 | 0.006 | 0.010 | 0.101 | 0.152 | 0.254 |
| D | 0.390 | 0.394 | 0.398 | 9.9 | 10.00 | 10.1 |
| E | 0.390 | 0.394 | 0.398 | 9.9 | 10.00 | 10.1 |
| e | 0.025 | 0.031 | 0.036 | 0.635 | 0.80 | 0.952 |
| $H_D$ | 0.510 | 0.520 | 0.530 | 12.95 | 13.2 | 13.45 |
| $H_E$ | 0.510 | 0.520 | 0.530 | 12.95 | 13.2 | 13.45 |
| L | 0.025 | 0.031 | 0.037 | 0.65 | 0.8 | 0.95 |
| $L_1$ | 0.051 | 0.063 | 0.075 | 1.295 | 1.6 | 1.905 |
| y | — | — | 0.003 | — | — | 0.08 |
| θ | 0° | — | 7° | 0° | — | 7° |

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.