# Nuvoton Technology Corporation - W77C032A40PL Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 40MHz |
| Connectivity | EBI/EMI, Serial Port |
| Peripherals | POR, WDT |
| Number of I/O | 36 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w77c032a40pl |

## 1. GENERAL DESCRIPTION

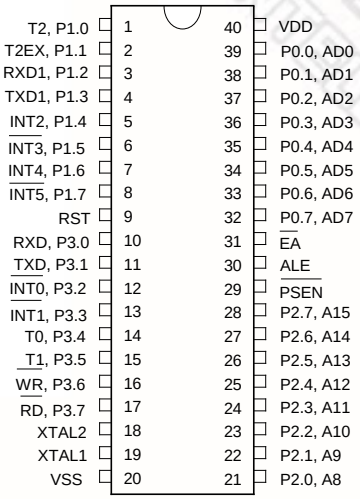
The W77C032 is a fast 8051 compatible microcontroller with a redesigned processor core without wasted clock and memory cycles. As a result, it executes every 8051 instruction faster than the original 8051 for the same crystal speed. Typically, the instruction executing time of W77C032 is 1.5 to 3 times faster then that of traditional 8051, depending on the type of instruction. In general, the overall performance is about 2.5 times better than the original for the same crystal speed. Giving the same throughput with lower clock speed, power consumption has been improved. Consequently, the W77C032 is a fully static CMOS design; it can also be operated at a lower crystal clock. The W77C032 provides operating voltage from 4.5V to 5.5V. All W77C032 types also support on-chip 1KB SRAM without external memory component and glue logic, saving more I/O pins for users application usage if they use on-chip SRAM instead of external SRAM.

## 2. FEATURES

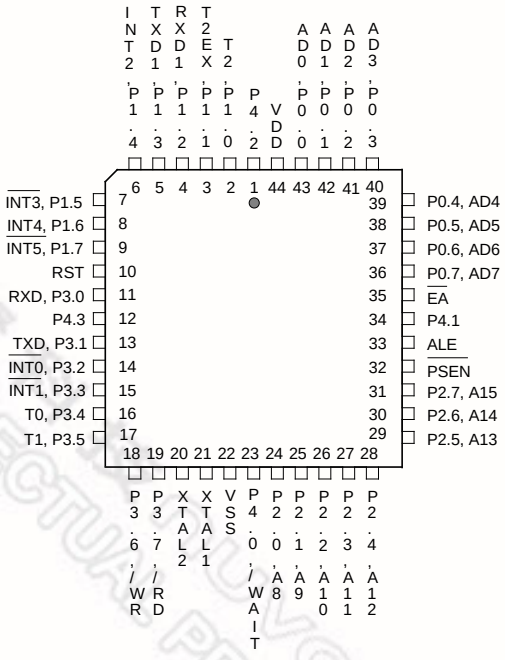
- 8-bit CMOS microcontroller
- High speed architecture of 4 clocks/machine cycle runs up to 40 MHz
- Pin compatible with standard 80C52
- Instruction-set compatible with MCS-51
- Four 8-bit I/O Ports
- One extra 4-bit I/O port and Wait State control signal (available on 44-pin PLCC/QFP package)
- Three 16-bit Timers
- 12 interrupt sources with two levels of priority
- On-chip oscillator and clock circuitry
- Two enhanced full duplex serial ports
- 256 bytes scratch-pad RAM
- 1KB on-chip SRAM for MOVX instruction
- Programmable Watchdog Timer
- Dual 16-bit Data Pointers
- Software programmable access cycle to external RAM/peripherals
- Packages:
  - Lead Free (RoHS) DIP 40: W77C032A40DL
  - Lead Free (RoHS) PLCC 44: W77C032A40PL
  - Lead Free (RoHS) PQFP 44: W77C032A40FL

## 3. PIN CONFIGURATIONS

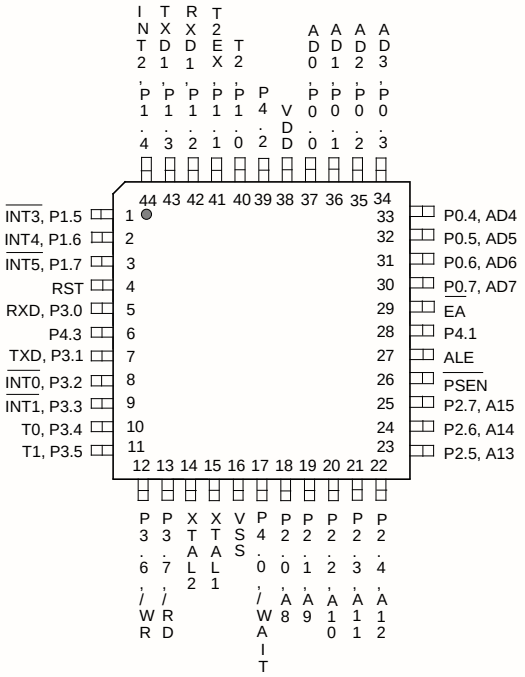
40-Pin DIP




44-Pin PLCC




44-Pin QFP



## 6. MEMORY ORGANIZATION

The W77C032 separates the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

### 6.1 Program Memory

The Program Memory on the W77C032 can be up to 64Kbytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

### 6.2 Data Memory

The W77C032 can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. Unlike the 8051 derivatives, the W77C032 contains on-chip 1K bytes MOVX SRAM of Data Memory, which can only be accessed by MOVX instructions. These 1K bytes of SRAM are between address 0000H and 03FFH. Access to the on-chip MOVX SRAM is optional under software control. When enabled by software, any MOVX instruction that uses this area will go to the on-chip RAM. MOVX addresses greater than 03FFH automatically go to external memory through Port 0 and 2. When disabled, the 1KB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000H and FFFFH goes to the expanded bus on Port 0 and 2. This is the default condition. In addition, the W77C032 has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small. In the event that larger data contents are present, two selections can be used. One is on-chip MOVX SRAM, the other is the external Data Memory. The on-chip MOVX SRAM can only be accessed by a MOVX instruction, the same as that for external Data Memory. However, the on-chip RAM has the fastest access times.

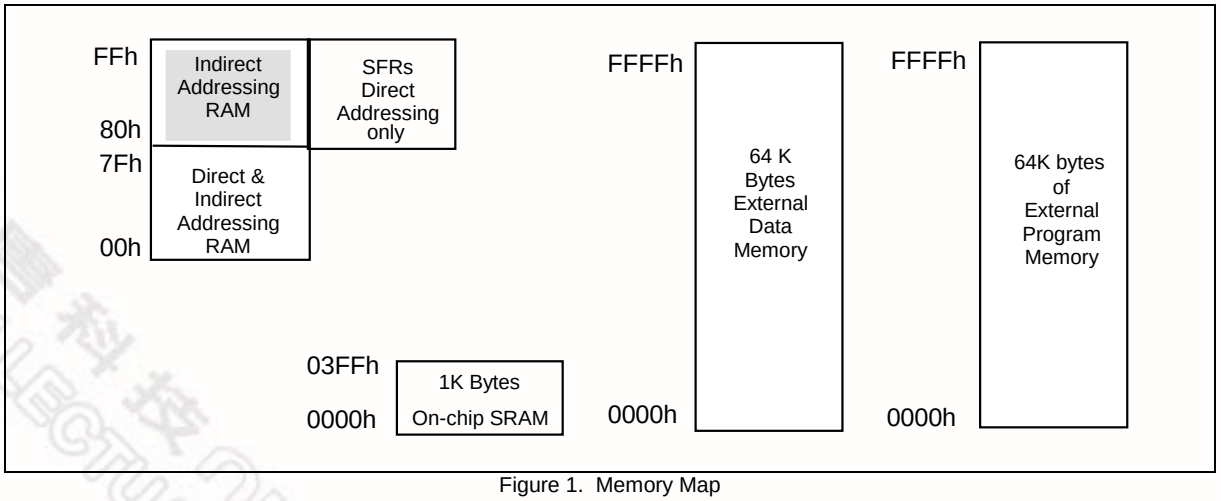



Figure 1. Memory Map

IE0: Interrupt 0 edge detect: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.

IT0: Interrupt 0 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

**Timer Mode Control**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | GATE | C/$\overline{T}$ | M1 | M0 | GATE | C/$\overline{T}$ | M1 | M0 |
| | TIMER1 | | | | TIMER0 | | | |

Mnemonic: TMOD Address: 89h

GATE: Gating control: When this bit is set, Timer/counter x is enabled only while $\overline{INTx}$ pin is high and TRx control bit is set. When cleared, Timer x is enabled whenever TRx control bit is set.

C/$\overline{T}$: Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the Tx pin.

M1, M0: Mode Select bits:

| M1 | M0 | Mode |
|---|---|---|
| 0 | 0 | Mode 0: 8-bits with 5-bit prescale. |
| 0 | 1 | Mode 1: 16-bits, no prescale. |
| 1 | 0 | Mode 2: 8-bits with auto-reload from THx |
| 1 | 1 | Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is a 8-bit timer only controlled by Timer 1 control bits. (Timer 1) Timer/counter is stopped. |

**Timer 0 LSB**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TL0.7 | TL0.6 | TL0.5 | TL0.4 | TL0.3 | TL0.2 | TL0.1 | TL0.0 |

Mnemonic: TL0 Address: 8Ah

TL0.7-0: Timer 0 LSB

MD2-0: Stretch MOVX select bits: These three bits are used to select the stretch value for the MOVX instruction. Using a variable MOVX length enables the user to access slower external memory devices or peripherals without the need for external circuits. The $\overline{RD}$ or $\overline{WR}$ strobe will be stretched by the selected interval. When accessing the on-chip SRAM, the MOVX instruction is always in 2 machine cycles regardless of the stretch setting. By default, the stretch has value of 1. If the user needs faster accessing, then a stretch value of 0 should be selected.

| MD2 | MD1 | MD0 | Stretch value | MOVX duration |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 2 machine cycles |
| 0 | 0 | 1 | 1 | 3 machine cycles *(Default)* |
| 0 | 1 | 0 | 2 | 4 machine cycles |
| 0 | 1 | 1 | 3 | 5 machine cycles |
| 1 | 0 | 0 | 4 | 6 machine cycles |
| 1 | 0 | 1 | 5 | 7 machine cycles |
| 1 | 1 | 0 | 6 | 8 machine cycles |
| 1 | 1 | 1 | 7 | 9 machine cycles |

**Port 1**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | P1.7 | P1.6 | P1.5 | P1.4 | P1.3 | P1.2 | P1.1 | P1.0 |

Mnemonic: P1 Address: 90h

P1.7-0: General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. Some pins also have alternate input or output functions. This alternate functions are described below:

P1.0: T2 External I/O for Timer/Counter 2
P1.1: T2EX Timer/Counter 2 Capture/Reload Trigger
P1.2: RXD1 Serial Port 1 Receive
P1.3: TXD1 Serial Port 1 Transmit
P1.4: INT2 External Interrupt 2
P1.5: $\overline{INT3}$ External Interrupt 3
P1.6: INT4 External Interrupt 4
P1.7: $\overline{INT5}$ External Interrupt 5

## 7.1 External Interrupt Flag

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | IE5 | IE4 | IE3 | IE2 | XT/RG | $\overline{\text{RGMD}}$ | RGSL | BGS |

Mnemonic: EXIF Address: 91h

IE5: External Interrupt 5 flag. Set by hardware when a falling edge is detected on $\overline{\text{INT5}}$.

IE4: External Interrupt 4 flag. Set by hardware when a rising edge is detected on INT4.

IE3: External Interrupt 3 flag. Set by hardware when a falling edge is detected on $\overline{\text{INT5}}$.

IE2: External Interrupt 2 flag. Set by hardware when a rising edge is detected on INT2.

XT/$\overline{\text{RG}}$ RG: Crystal/RC Oscillator Select. Setting this bit selects crystal or external clock as system clock source. Clearing this bit selects the on-chip RC oscillator as clock source. XTUP(STATUS.4) must be set to 1 and XTOFF (PMR.3) must be cleared before this bit can be set. Attempts to set this bit without obeying these conditions will be ignored. This bit is set to 1 after a power-on reset and unchanged by other forms of reset.

RGMD: RC Mode Status. This bit indicates the current clock source of microcontroller. When cleared, CPU is operating from the external crystal or oscillator. When set, CPU is operating from the on-chip RC oscillator. This bit is cleared to 0 after a power-on reset and unchanged by other forms of reset.

RGSL: RC Oscillator Select. This bit selects the clock source following a resume from Power Down Mode. Setting this bit allows device operating from RC oscillator when a resume from Power Down Mode. When this bit is cleared, the device will hold operation until the crystal oscillator has warmed-up following a resume from Power Down Mode. This bit is cleared to 0 after a power-on reset and unchanged by other forms of reset.

**Serial Port Control**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SM0/FE | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |

Mnemonic: SCON Address: 98h

SM0/FE: Serial port 0, Mode 0 bit or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.

SM1: Serial port Mode bit 1:

| SM0 | SM1 | Mode | Description | Length | Baud rate |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Synchronous | 8 | 4/12 Tclk |
| 0 | 1 | 1 | Asynchronous | 10 | variable |
| 1 | 0 | 2 | Asynchronous | 11 | 64/32 Tclk |
| 1 | 1 | 3 | Asynchronous | 11 | variable |

SM2: Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.

REN: Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.

TB8: This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.

RB8: In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.

TI: Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

RI: Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software

**Serial Data Buffer**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SBUF.7 | SBUF.6 | SBUF.5 | SBUF.4 | SBUF.3 | SBUF.2 | SBUF.1 | SBUF.0 |

Mnemonic: SBUF Address: 99h

SBUF.7-0: Serial data on the serial port 0 is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

**Port 2**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | P2.7 | P2.6 | P2.5 | P2.4 | P2.3 | P2.2 | P2.1 | P2.0 |

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.

**Port 4**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | - | - | - | P4.3 | P4.2 | P4.1 | P4.0 |

Mnemonic: P4 Address: A5h

P4.3-0: Port 4 is a bi-directional I/O port with internal pull-ups.

P3.7-0: General purpose I/O port. Each pin also has an alternate input or output function. The alternate functions are described below.

| | | |
|---|---|---|
| P3.7 | $\overline{RD}$ | Strobe for read from external RAM |
| P3.6 | $\overline{WR}$ | Strobe for write to external RAM |
| P3.5 | T1 | Timer/counter 1 external count input |
| P3.4 | T0 | Timer/counter 0 external count input |
| P3.3 | $\overline{INT1}$ | External interrupt 1 |
| P3.2 | $\overline{INT0}$ | External interrupt 0 |
| P3.1 | TxD | Serial port 0 output |
| P3.0 | RxD | Serial port 0 input |

**Interrupt Priority**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | PS1 | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

Mnemonic: IP Address: B8h

IP.7: This bit is un-implemented and will read high.
PS1: This bit defines the Serial port 1 interrupt priority. PS = 1 sets it to higher priority level.
PT2: This bit defines the Timer 2 interrupt priority. PT2 = 1 sets it to higher priority level.
PS: This bit defines the Serial port 0 interrupt priority. PS = 1 sets it to higher priority level.
PT1: This bit defines the Timer 1 interrupt priority. PT1 = 1 sets it to higher priority level.
PX1: This bit defines the External interrupt 1 priority. PX1 = 1 sets it to higher priority level.
PT0: This bit defines the Timer 0 interrupt priority. PT0 = 1 sets it to higher priority level.
PX0: This bit defines the External interrupt 0 priority. PX0 = 1 sets it to higher priority level.

**Slave Address Mask Enable**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |

Mnemonic: SADEN Address: B9h

SADEN: This register enables the Automatic Address Recognition feature of the Serial port 0. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN.n is 0, then the bit becomes a “don’t care” in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 0. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

**Slave Address Mask Enable 1**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |

Mnemonic: SADEN1 Address: Bah

SADEN1: This register enables the Automatic Address Recognition feature of the Serial port 1. When a bit in the SADEN1 is set to 1, the same bit location in SADDR1 will be compared with the incoming serial data. When SADEN1.n is 0, then the bit becomes a “don’t care” in the

comparison. This register enables the Automatic Address Recognition feature of the Serial port 1. When all the bits of SADEN1 are 0, interrupt will occur for any incoming address.

**Serial Port Control 1**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SM0_1/FE_1 | SM1_1 | SM2_1 | REN_1 | TB8_1 | RB8_1 | TI_1 | RI_1 |

Mnemonic: SCON1 Address: C0h

SM0_1/FE_1: Serial port 1, Mode 0 bit or Framing Error Flag 1: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0_1 or as FE_1. the operation of SM0_1 is described below. When used as FE_1, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE_1 condition.

SM1_1: Serial port 1 Mode bit 1:

| SM0_1 | SM1_1 | Mode | Description | Length | Baud rate |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Synchronous | 8 | 4/12 Tclk |
| 0 | 1 | 1 | Asynchronous | 10 | variable |
| 1 | 0 | 2 | Asynchronous | 11 | 64/32 Tclk |
| 1 | 1 | 3 | Asynchronous | 11 | variable |

SM2_1: Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2_1 is set to 1, then RI_1 will not be activated if the received 9$^{th}$ data bit (RB8_1) is 0. In mode 1, if SM2_1 = 1, then RI_1 will not be activated if a valid stop bit was not received. In mode 0, the SM2_1 bit controls the serial port 1 clock. If set to 0, then the serial port 1 runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.

REN_1: Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.

TB8_1: This is the 9$^{th}$ bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.

RB8_1: In modes 2 and 3 this is the received 9$^{th}$ data bit. In mode 1, if SM2_1 = 0, RB8_1 is the stop bit that was received. In mode 0 it has no function.

TI_1: Transmit interrupt flag: This flag is set by hardware at the end of the 8$^{th}$ bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

RI_1: Receive interrupt flag: This flag is set by hardware at the end of the 8$^{th}$ bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2_1 apply to this bit. This bit can be cleared only by software

**Serial Data Buffer 1**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SBUF1.7 | SBUF1.6 | SBUF1.5 | SBUF1.4 | SBUF1.3 | SBUF1.2 | SBUF1.1 | SBUF1.0 |

Mnemonic: SBUF1 Address: C1h

SBUF1.7-0: Serial data of the serial port 1 is read from or written to this location. It actually consists of two separate 8-bit registers. One is the receive resister, and the other is the transmit

**Status Register**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | HIP | LIP | XTUP | SPTA1 | SPRA1 | SPTA0 | SPRA0 |

Mnemonic: STATUS Address: C5h

HIP: High Priority Interrupt Status. When set, it indicates that software is servicing a high priority interrupt. This bit will be cleared when the program executes the corresponding RETI instruction.

LIP: Low Priority Interrupt Status. When set, it indicates that software is servicing a low priority interrupt. This bit will be cleared when the program executes the corresponding RETI instruction.

XTUP: Crystal Oscillator Warm-up Status. When set, this bit indicates CPU has detected clock to be ready. Each time the crystal oscillator is restarted by exit from power down mode or the XTOFF bit is set, hardware will clear this bit. This bit is set to 1 after a power-on reset. When this bit is cleared, it prevents software from setting the XT/$\overline{RG}$ bit to enable CPU operation from crystal oscillator.

SPTA1: Serial Port 1 Transmit Activity. This bit is set during serial port 1 is currently transmitting data. It is cleared when TI_1 bit is set by hardware. Changing the Clock Divide Control bits CD0, CD1 will be ignored when this bit is set to 1 and SWB = 1.

SPRA1: Serial Port 1 Receive Activity. This bit is set during serial port 1 is currently receiving a data. It is cleared when RI_1 bit is set by hardware. Changing the Clock Divide Control bits CD0, CD1 will be ignored when this bit is set to 1 and SWB = 1.

SPTA0: Serial Port 0 Transmit Activity. This bit is set during serial port 0 is currently transmitting data. It is cleared when TI bit is set by hardware. Changing the Clock Divide Control bits CD0, CD1 will be ignored when this bit is set to 1 and SWB = 1.

SPRA0: Serial Port 0 Receive Activity. This bit is set during serial port 0 is currently receiving a data. It is cleared when RI bit is set by hardware. Changing the Clock Divide Control bits CD0, CD1 will be ignored when this bit is set to 1 and SWB = 1.

**Timed Access**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TA.7 | TA.6 | TA.5 | TA.4 | TA.3 | TA.2 | TA.1 | TA.0 |

Mnemonic: TA Address: C7h

TA: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

**Timer 2 Control**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/$\overline{T2}$ | CP/$\overline{RL2}$ |

Mnemonic: T2CON Address: C8h

TF2: Timer 2 overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in down count mode. It can be set only if RCLK and TCLK are both 0. It is cleared only by software. Software can also set or clear this bit.

| RS1 | RS0 | Register bank | Address |
|---|---|---|---|
| 0 | 0 | 0 | 00-07h |
| 0 | 1 | 1 | 08-0Fh |
| 1 | 0 | 2 | 10-17h |
| 1 | 1 | 3 | 18-1Fh |

OV: Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.

F1: User Flag 1: General purpose flag that can be set or cleared by the user by software

P: Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

**Watchdog Control**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SMOD_1 | POR | - | - | WDIF | WTRF | EWT | RWT |

Mnemonic: WDCON Address: D8h

SMOD_1:This bit doubles the Serial Port 1 baud rate in mode 1, 2, and 3 when set to 1.

POR: Power-on reset flag. Hardware will set this flag on a power up condition. This flag can be read or written by software. A write by software is the only way to clear this bit once it is set.

WDIF: Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software.

WTRF: Watchdog Timer Reset Flag. Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the watchdog timer will have no affect on this bit.

EWT: Enable Watchdog timer Reset. Setting this bit will enable the Watchdog timer Reset function.

RWT: Reset Watchdog Timer. This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the RWT before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWT is set. This bit is self-clearing by hardware.

The WDCON SFR is set to a 0x0x0xx0b on an external reset. WTRF is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is set to 0 on a Power-on reset and unaffected by other resets.

All the bits in this SFR have unrestricted read access. POR, EWT, WDIF and RWT require Timed Access procedure to write. The remaining bits have unrestricted write accesses.

Table 3. Instruction Timing for W77C032, continued

| INSTRUCTION | HEX OP-CODE | BYTES | W77C032 MACHINE CYCLES | W77C032 CLOCK CYCLES | 8032 CLOCK CYCLES | W77C032 VS. 8032 SPEED RATIO |
|---|---|---|---|---|---|---|
| MOV @R0, direct | A6 | 2 | 2 | 8 | 12 | 1.5 |
| MOV @R1, direct | A7 | 2 | 2 | 8 | 12 | 1.5 |
| MOV @R0, #data | 76 | 2 | 2 | 8 | 12 | 1.5 |
| MOV @R1, #data | 77 | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, A | F5 | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, R0 | 88 | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, R1 | 89 | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, R2 | 8A | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, R3 | 8B | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, R4 | 8C | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, R5 | 8D | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, R6 | 8E | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, R7 | 8F | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, @R0 | 86 | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, @R1 | 87 | 2 | 2 | 8 | 12 | 1.5 |
| MOV direct, direct | 85 | 3 | 3 | 12 | 24 | 2 |
| MOV direct, #data | 75 | 3 | 3 | 12 | 24 | 2 |
| MOV DPTR, #data 16 | 90 | 3 | 3 | 12 | 24 | 2 |
| MOVC A, @A+DPTR | 93 | 1 | 2 | 8 | 24 | 3 |
| MOVC A, @A+PC | 83 | 1 | 2 | 8 | 24 | 3 |
| MOVX A, @R0 | E2 | 1 | 2 – 9 | 8 – 36 | 24 | 3 – 0.66 |
| MOVX A, @R1 | E3 | 1 | 2 – 9 | 8 – 36 | 24 | 3 – 0.66 |
| MOVX A, @DPTR | E0 | 1 | 2 – 9 | 8 – 36 | 24 | 3 – 0.66 |
| MOVX @R0, A | F2 | 1 | 2 – 9 | 8 – 36 | 24 | 3 – 0.66 |
| MOVX @R1, A | F3 | 1 | 2 – 9 | 8 – 36 | 24 | 3 – 0.66 |
| MOVX @DPTR, A | F0 | 1 | 2 – 9 | 8 – 36 | 24 | 3 – 0.66 |
| MOV C, bit | A2 | 2 | 2 | 8 | 12 | 1.5 |
| MOV bit, C | 92 | 2 | 2 | 8 | 24 | 3 |
| ORL A, R0 | 48 | 1 | 1 | 4 | 12 | 3 |
| ORL A, R1 | 49 | 1 | 1 | 4 | 12 | 3 |
| ORL A, R2 | 4A | 1 | 1 | 4 | 12 | 3 |
| ORL A, R3 | 4B | 1 | 1 | 4 | 12 | 3 |
| ORL A, R4 | 4C | 1 | 1 | 4 | 12 | 3 |
| ORL A, R5 | 4D | 1 | 1 | 4 | 12 | 3 |
| ORL A, R6 | 4E | 1 | 1 | 4 | 12 | 3 |
| ORL A, R7 | 4F | 1 | 1 | 4 | 12 | 3 |
| ORL A, @R0 | 46 | 1 | 1 | 4 | 12 | 3 |
| ORL A, @R1 | 47 | 1 | 1 | 4 | 12 | 3 |

The selection of instruction rate is going to take effect after a delay of one instruction cycle. Switching to divide by 64 or 1024 mode must first go from divide by 4 mode. This means software can not switch directly between clock/64 and clock/1024 mode. The CPU has to return clock/4 mode first, then go to clock/64 or clock/1024 mode.

The W77C032 allows the user to use internal RC oscillator instead of external crystal. Setting the XT/$\overline{RG}$ bit (EXIF.3) selects the crystal or RC oscillator as the clock source. When invoking RC oscillator in Economy mode, software may set the XTOFF bit to turn off the crystal amplifier for saving power. The CPU would run at the clock rate of approximately 2–4 MHz divided by 4, 64 or 1024. The RC oscillator is not precise so that can not be invoked to the operation which needs the accurate time-base such as serial communication. The RGMD(EXIF.2) indicates current clock source. When switching the clock source, CPU needs one instruction cycle delay to take effect new setting. If crystal amplifier is disabled and RC oscillator is present clock source, software must first clear the XTOFF bit to turn on crystal amplifier before switch to crystal operation. Hardware will set the XTUP bit (STATUS.4) once the crystal is warm-up and ready for use. It is unable to set XT/$\overline{RG}$ bit to 1 if XTUP = 0.

In Economy mode, the serial port can not receive/transmit data correctly because the baud rate is changed. In some systems, the external interrupts may require the fastest process such that the reducing of operating speed is restricted. In order to solve these dilemmas, the W77C032 offers a switchback feature which allows the CPU back to clock/4 mode immediately when triggered by serial operation or external interrupts. The switchback feature is enabled by setting the SWB bit (PMR.5). A serial port reception/transmission or qualified external interrupt which is enabled and acknowledged without block conditions will cause CPU to return to divide by 4 mode. For the serial port reception, a switchback is generated by a falling edge associated with start bit if the serial port reception is enabled. When a serial port transmission, an instruction which writes a byte of data to serial port buffer will cause a switchback to ensure the correct transmission. The switchback feature is unaffected by serial port interrupt flags. After a switchback is generated, the software can manually return the CPU to Economy mode. Note that the modification of clock control bits CD0 and CD1 will be ignored during serial port transmit/receive when switchback is enabled. The Watchdog timer reset, power-on/fail reset or external reset will force the CPU to return to divide by 4 mode.

## 9.3 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. In this state the ALE and $\overline{PSEN}$ pins are pulled low. The port pins output the values held by their respective SFRs.

The W77C032 will exit the Power Down mode with a reset or by an external interrupt pin enabled as level detect. An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode.

The W77C032 can be woken from the Power Down mode by forcing an external interrupt pin activated, provided the corresponding interrupt is enabled, while the global enable(EA) bit is set and the external input has been set to a level detect mode. If these conditions are met, then the low level on the external pin re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after the one which put the device into Power Down mode and continues from there. When RGSL(EXIF.1) bit is set to 1, the CPU will use the internal RC oscillator instead of crystal to exit Power Down mode. The microcontroller will automatically switch from RC oscillator to crystal after clock is stable. The RC oscillator runs at approximately 2–4 MHz. Using RC oscillator to exit from Power Down mode saves the time for waiting crystal start-up. It is useful in the low power system which usually be awakened from a short operation then returns to Power Down mode.

**Table 5. Status of external pins during Idle and Power Down**

| MODE | PROGRAM MEMORY | ALE | $\overline{\text{PSEN}}$ | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power Down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power Down | External | 0 | 0 | Float | Data | Data | Data |

## 11.2 Priority Level Structure

There are two priority levels for the interrupts, high and low. The interrupt source can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown below; the interrupts are numbered starting from the highest priority to the lowest.

**Table 7. Priority structure of interrupts**

| SOURCE | FLAG | PRIORITY LEVEL |
|---|---|---|
| External Interrupt 0 | IE0 | 1 (highest) |
| Timer 0 Overflow | TF0 | 2 |
| External Interrupt 1 | IE1 | 3 |
| Timer 1 Overflow | TF1 | 4 |
| Serial Port | RI + TI | 5 |
| Timer 2 Overflow | TF2 + EXF2 | 6 |
| Serial Port 1 | RI_1 + TI_1 | 7 |
| External Interrupt 2 | IE2 | 8 |
| External Interrupt 3 | IE3 | 9 |
| External Interrupt 4 | IE4 | 10 |
| External Interrupt 5 | IE5 | 11 |
| Watchdog Timer | WDIF | 12 (lowest) |

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are

1. An interrupt of equal or higher priority is not currently being serviced.
2. The current polling cycle is the last machine cycle of the instruction currently being executed.
3. The current instruction does not involve a write to IP, IE, EIP or EIE registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

## 12. PROGRAMMABLE TIMERS/COUNTERS

The W77C032 has three 16-bit programmable timer/counters and one programmable Watchdog timer. The Watchdog timer is operationally quite different from the other two timers.

### 12.1 Timer/Counters 0 & 1

The W77C032 has two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a “Timer”, the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the “Counter” mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the “Timer” or “Counter” mode, the count register will be updated at C3. Therefore, in the “Timer” mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The “Timer” or “Counter” function is selected by the “C/$\overline{T}$” bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

#### 12.1.1 Time-base Selection

The W77C032 gives the user two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on the W77C032 and the standard 8051 can be matched. This is the default mode of operation of the W77C032 timers. The user also has the option to count in the turbo mode, where the timers will increment at the rate of 1/4 clock speed. This will straight-away increase the counting speed three times. This selection is done by the T0M and T1M bits in CKCON SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits to 1 if the timers are to operate in turbo mode.

## 12.2 Timer/Counter 2

Timer/Counter 2 is a 16 bit up/down counter which is configured by the T2MOD register and controlled by the T2CON register. Timer/Counter 2 is equipped with a capture/reload capability. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock, and in defining the operating mode. The clock source for Timer/Counter 2 may be selected for either the external T2 pin (C/$\overline{T2}$ = 1) or the crystal oscillator, which is divided by 12 or 4 (C/$\overline{T2}$ = 0). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

### 12.2.1 Capture Mode

The capture mode is enabled by setting the CP/$\overline{RL2}$ bit in the T2CON register to a 1. In the capture mode, Timer/Counter 2 serves as a 16 bit up counter. When the counter rolls over from FFFFh to 0000h, the TF2 bit is set, which will generate an interrupt request. If the EXEN2 bit is set, then a negative transition of T2EX pin will cause the value in the TL2 and TH2 register to be captured by the RCAP2L and RCAP2H registers. This action also causes the EXF2 bit in T2CON to be set, which will also generate an interrupt. Setting the T2CR bit (T2MOD.3), the W77C032 allows hardware to reset timer 2 automatically after the value of TL2 and TH2 have been captured.

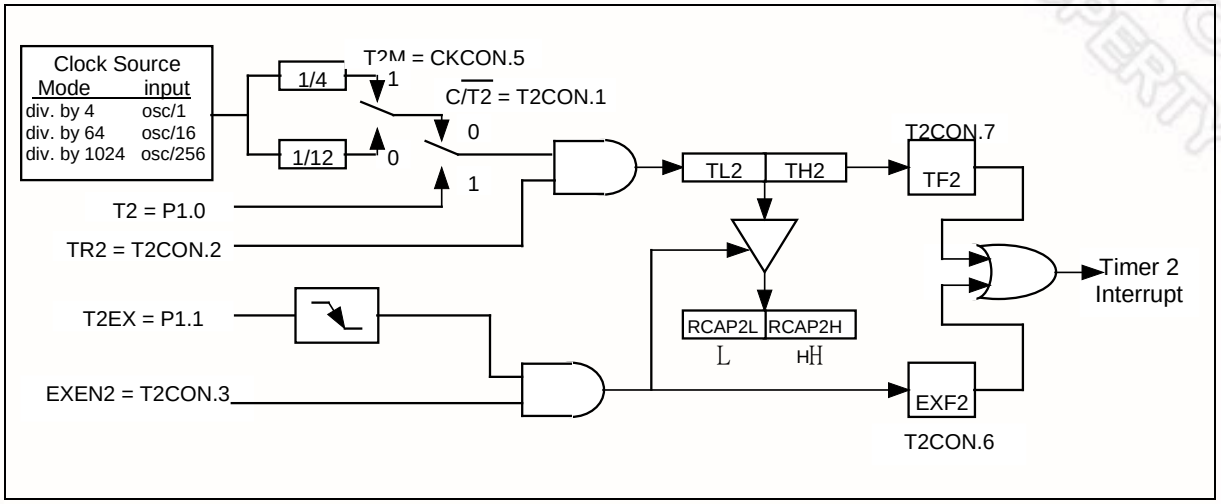



Figure 14. 16-Bit Capture Mode

### 12.2.2 Auto-reload Mode, Counting Up

The auto-reload mode as an up counter is enabled by clearing the CP/$\overline{RL2}$ bit in the T2CON register and clearing the DCEN bit in T2MOD register. In this mode, Timer/Counter 2 is a 16 bit up counter. When the counter rolls over from FFFFh, a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. The reload action also sets the TF2 bit. If the EXEN2 bit is set, then a negative transition of T2EX pin will also cause a reload. This action also sets the EXF2 bit in T2CON.

### 12.2.4 Baud Rate Generator Mode

The baud rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. While in the baud rate generator mode, Timer/Counter 2 is a 16 bit counter with auto reload when the count rolls over from FFFFh. However, rolling over does not set the TF2 bit. If EXEN2 bit is set, then a negative transition of the T2EX pin will set EXF2 bit in the T2CON register and cause an interrupt request.

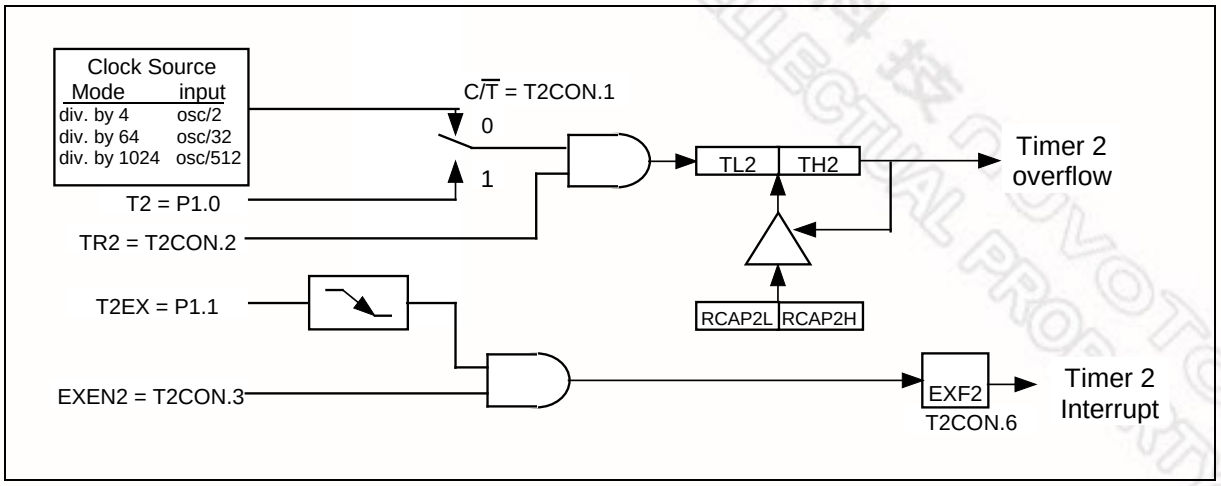



Figure 17. Baud Rate Generator Mode

### 12.2.5 Programmable Clock-out

Timer 2 is equipped with a new clock-out feature which outputs a 50% duty cycle clock on P1.0. It can be invoked as a programmable clock generator. To configure Timer 2 with clock-out mode, software must initiate it by setting bit T2OE = 1, C/T2 = 0 and CP/RL = 0. Setting bit TR2 will start the timer. This mode is similar to the baud rate generator mode, it will not generate an interrupt while Timer 2 overflow. So it is possible to use Timer 2 as a baud rate generator and a clock generator at the same time. The clock-out frequency is determined by the following equation:

The Clock-out Frequency = Oscillator Frequency / [4 X (RCAP2H, RCAP2L) ]

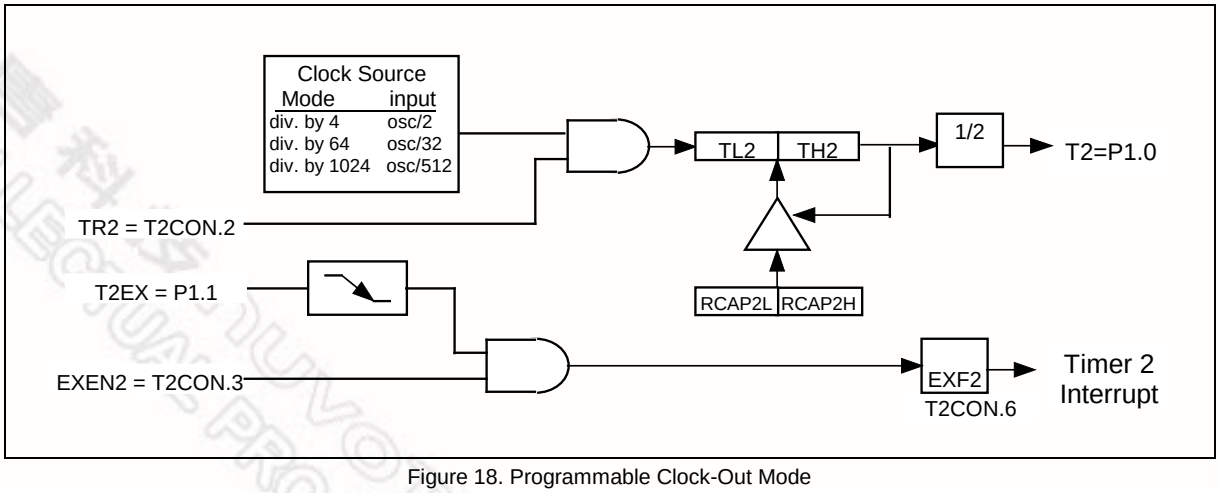



Figure 18. Programmable Clock-Out Mode

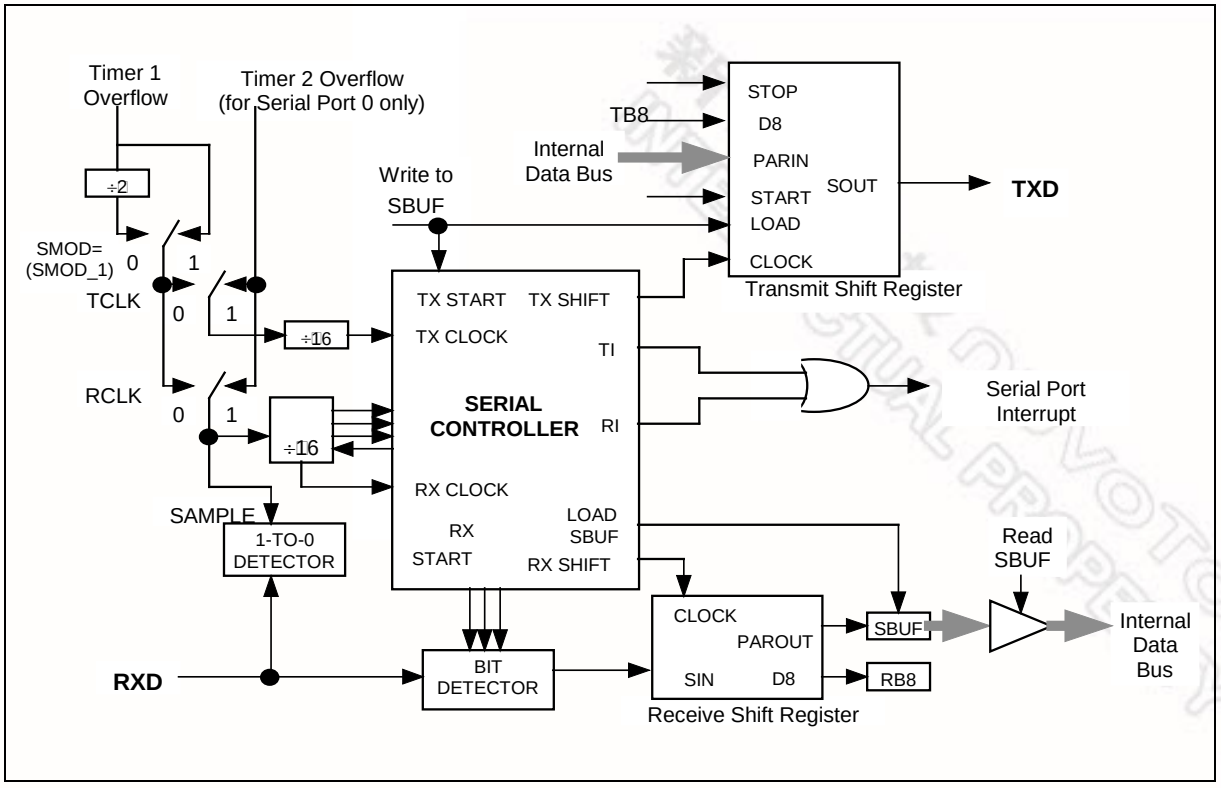



Figure 23: Serial Port Mode 3

### Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. The W77C032 has the facility to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE(FE_1) bit is located in SCON.7(SCON1.7). This bit is normally used as SM0 in the standard 8051 family. However, in the W77C032 it serves a dual function and is called SM0/FE (SM0_1/FE_1). There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7(SCON1.7) is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE or FE_1. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

### Multiprocessor Communications

Multiprocessor communications makes use of the 9$^{th}$ data bit in modes 2 and 3. In the W77C032, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9$^{th}$ bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave

processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of a address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9$^{th}$ bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

| | |
|---|---|
| SADDR | 1010 0100 |
| SADEN | 1111 1010 |
| Given | 1010 0x0x |

Slave 2:

| | |
|---|---|
| SADDR | 1010 0111 |
| SADEN | 1111 1001 |
| Given | 1010 0xx1 |

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical Oring of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXX XXXX(i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.