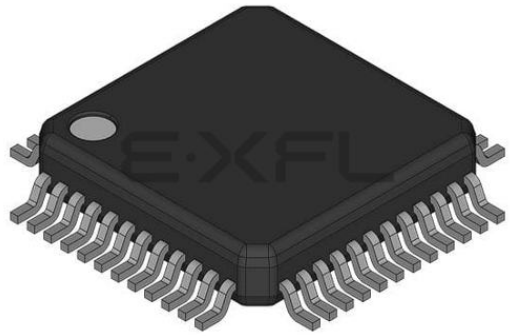

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8246mlf

2 Overview

2.1 MC56F825x/MC56F824x Features

2.1.1 Core

- Efficient 56800E digital signal processor (DSP) engine with modified Harvard architecture
  - Three internal address buses
  - Four internal data buses
- As many as 60 million instructions per second (MIPS) at 60 MHz core frequency
- 155 basic instructions in conjunction with up to 20 address modes
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Instruction set supports DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, processor speed–independent, real-time debugging

2.1.2 Operation Range

- 3.0 V to 3.6 V operation (power supplies and I/O)
- From power-on-reset: approximately 2.7 V to 3.6 V
- Ambient temperature operating range: –40 °C to +105 °C

2.1.3 Memory

- Dual Harvard architecture that permits as many as three simultaneous accesses to program and data memory
- 48 KB (24K x 16) to 64 KB (32K x 16) on-chip flash memory with 2048 bytes (1024 x 16) page size
- 6 KB (3K x 16) to 8 KB (4K x 16) on-chip RAM with byte addressable
- EEPROM emulation capability using flash
- Support for 60 MHz program execution from both internal flash and RAM memories
- Flash security and protection that prevent unauthorized users from gaining access to the internal flash

2.1.4 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: Level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, and SWI3 instruction
  - Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, and EOnCE trace buffer

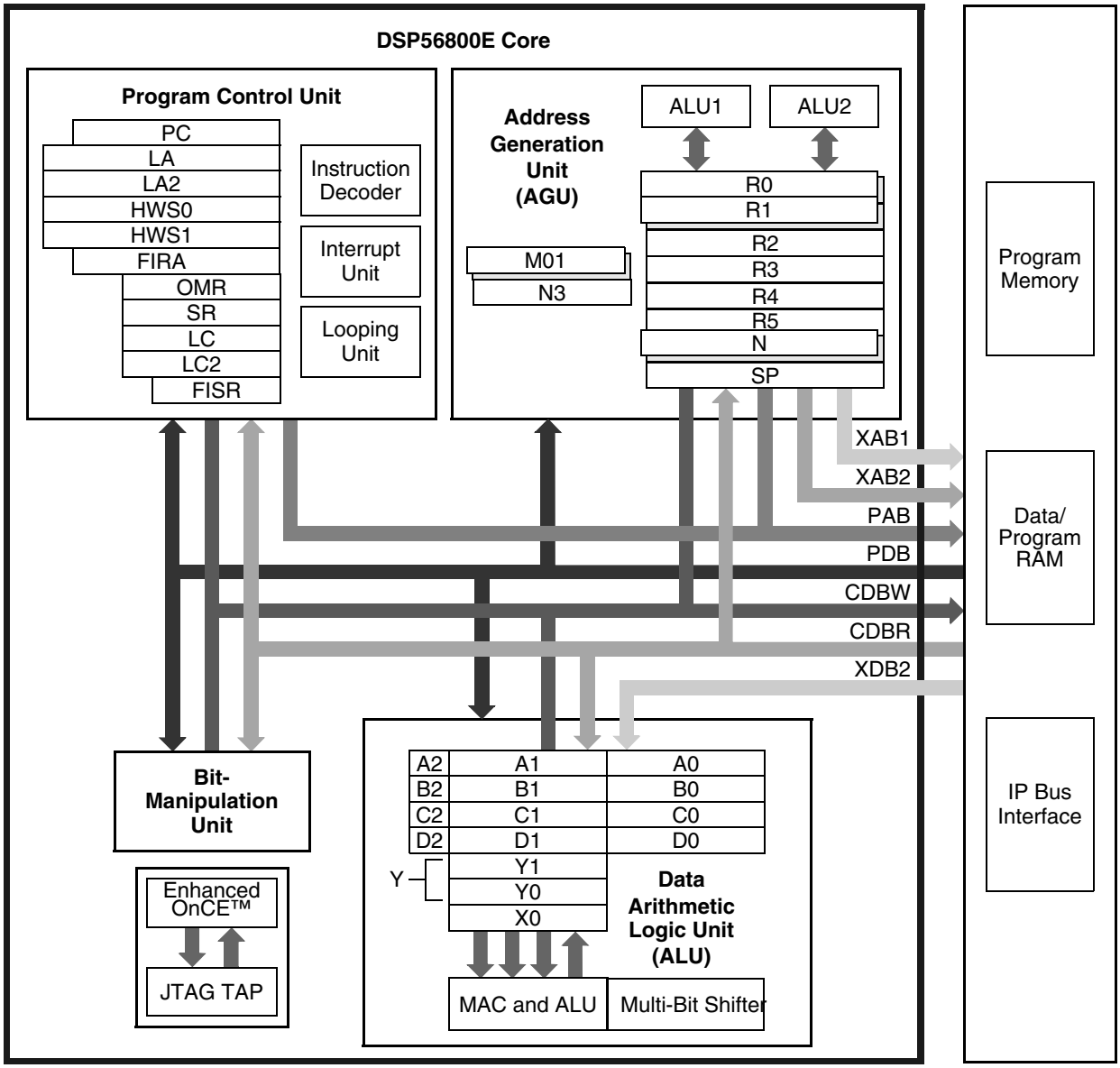


Figure 1. 56800E Core Block Diagram

Figure 2 shows the peripherals and control blocks connected to the IP bus bridge. Refer to the system integration module (SIM) section in the device's reference manual for information about which signals are multiplexed with those of other peripherals.

Table 4. MC56F825x/MC56F824x Pins (continued)

Pin Number			Pin Name	Peripherals													
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MSCAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
19	21	28	GPIOB3/ *ANB3&VREFLB&CMPC_M0*	**GPIOB3**					*ANB3& VREFLB*		*CMPC_M0*					
		29	V_{DD}											**V_{DD}**		
20	22	30	V_{SS}											**V_{SS}**		
21	23	31	GPIOC6/*TA2/XB_IN3/ CMP_REF*	**GPIOC6**						*XB_IN3*	*CMP_REF*	*TA2*				
22	24	32	GPIOC7/$\overline{SS}$/*TXD0*	**GPIOC7**		*TXD0*	$\overline{SS}$									
23	25	33	GPIOC8/*MISO/RXD0*	**GPIOC8**		*RXD0*	*MISO*									
24	26	34	GPIOC9/*SCLK/XB_IN4*	**GPIOC9**			*SCLK*			*XB_IN4*						
25	27	35	GPIOC10/MOSI/XB_IN5/MISO	**GPIOC10**			MOSI/ MISO			XB_IN5						
	28	36	GPIOF0/*XB_IN6*	**GPIOF0**						*XB_IN6*						
26	29	37	GPIOC11/*CANTX/SCL1/TXD1*	**GPIOC11**	*SCL1*	*TXD1*		*CANTX*								
27	30	38	GPIOC12/*CANRX/SDA1/RXD1*	**GPIOC12**	*SDA1*	*RXD1*		*CANRX*								
		39	GPIOF2/*SCL1/XB_OUT2*	**GPIOF2**	*SCL1*					*XB_OUT2*						
		40	GPIOF3/*SDA1/XB_OUT3*	**GPIOF3**	*SDA1*					*XB_OUT3*						
		41	GPIOF4/*TXD1/XB_OUT4*	**GPIOF4**		*TXD1*				*XB_OUT4*						
		42	GPIOF5/*RXD1/XB_OUT5*	**GPIOF5**		*RXD1*				*XB_OUT5*						
28	31	43	V_{SS}											**V_{SS}**		
29	32	44	V_{DD}											**V_{DD}**		
30	33	45	GPIOE0/*PWM0B*	**GPIOE0**									*PWM0B*			
31	34	46	GPIOE1/*PWM0A*	**GPIOE1**									*PWM0A*			
32	35	47	GPIOE2/*PWM1B*	**GPIOE2**									*PWM1B*			
33	36	48	GPIOE3/*PWM1A*	**GPIOE3**									*PWM1A*			
34	37	49	GPIOC13/*TA3/XB_IN6*	**GPIOC13**						*XB_IN6*		TA3				
	38	50	GPIOF1/*CLKO/XB_IN7*	**GPIOF1**						*XB_IN7*						*CLKO*
35	39	51	GPIOE4/*PWM2B/XB_IN2*	**GPIOE4**						*XB_IN2*			*PWM2B*			
36	40	52	GPIOE5/*PWM2A/XB_IN3*	**GPIOE5**						*XB_IN3*			*PWM2A*			
		53	GPIOE6/*PWM3B/XB_IN4*	**GPIOE6**						*XB_IN4*			*PWM3B*			
		54	GPIOE7/*PWM3A/XB_IN5*	**GPIOE7**						*XB_IN5*			*PWM3A*			
37	41	55	GPIOC14/*SDA0/XB_OUT0*	**GPIOC14**	*SDA0*					*XB_OUT0*						
38	42	56	GPIOC15/*SCL0/XB_OUT1*	**GPIOC15**	*SCL0*					*XB_OUT1*						
39	43	57	V_{CAP}											**V_{CAP}**		
		58	GPIOF6/*TB2/PWM3X*	**GPIOF6**								*TB2*	*PWM3X*			
		59	GPIOF7/*TB3*	**GPIOF7**								*TB3*				
40	44	60	V_{DD}											**V_{DD}**		

3.3 MC56F825x/MC56F824x Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses and as *italic*, must be programmed via the GPIO module's peripheral enable registers (GPIO_x_PER) and the SIM module's GPIO peripheral select (GPSx) registers.

Table 5. MC56F825x/MC56F824x Signal and Package Information

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
V_{DD}			29	Supply	Supply	I/O Power — This pin supplies 3.3 V power to the chip I/O interface.
V_{DD}	29	32	44			
V_{DD}	40	44	60			
V_{SS}	20	22	30	Supply	Supply	I/O Ground — These pins provide ground for chip I/O interface.
V_{SS}	28	31	43			
V_{SS}	41	45	61			
V_{DDA}	13	15	22	Supply	Supply	Analog Power — This pin supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	14	16	23	Supply	Supply	Analog Ground — This pin supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	17	19	26	Supply	Supply	V_{CAP} — Connect a bypass capacitor of 2.2 µF or greater between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation. See Section 8.2, "Electrical Design Considerations," on page 73.
V_{CAP}	39	43	57			
TDI *(GPIOD0)*	44	48	64	Input Input/ Output	Input, internal pullup enabled	Test Data Input — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDI.
TDO *(GPIOD1)*	42	46	62	Output Input/ Output	Output	Test Data Output — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
TCK *(GPIOD2)*	1	1	1	Input Input/ Output	Input, internal pullup enabled	Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TCK

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
TMS *(GPIOD3)*	43	47	63	input Input/ Output	Input, internal pullup enabled	Test Mode Select Input — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TMS **Note**: Always tie the TMS pin to VDD through a 2.2K resistor if need to keep on-board debug capability. Otherwise directly tie to VDD
$\overline{\text{RESET}}$ *(GPIOD4)*	2	2	2	Input Input/ Open-drain Output	Input, internal pullup enabled	Reset — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. Port D GPIO — This GPIO pin can be individually programmed as an input or open-drain output pin.If $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can be reset only via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOA0 *(ANA0& CMPA_P2)* *(CMPC_O)*	8	9	13	Input/ Output Input Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA0 and CMPA_P2 — Analog input to channel 0 of ADCA and positive input 2 of analog comparator A. CMPC_O— Analog comparator C output When used as an analog input, the signal goes to the ANA0 and CMPA_P2. After reset, the default state is GPIOA0.
GPIOA1 *(ANA1& CMPA_M0)*	9	10	14	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA1 and CMPA_M0 — Analog input to channel 1of ADCA and negative input 0 of analog comparator A. When used as an analog input, the signal goes to the ANA1 and CMPA_M0. After reset, the default state is GPIOA1.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOF1		38	50	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CLKO)				Output		CLKO — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(XB_IN7)				Input		XB_IN7 — Crossbar module input 7
						After reset, the default state is GPIOF1.
GPIOF2			39	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(SCL1)				Input/ Open-drain Output		SCL1 — The I^2C1 serial clock.
(XB_OUT2)				Output		XB_OUT2 — Crossbar module output 2
						After reset, the default state is GPIOF2.
GPIOF3			40	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(SDA1)				Input/ Open-drain Output		SDA1 — The I^2C1 serial data line.
(XB_OUT3)				Output		XB_OUT3 — Crossbar module output 3
						After reset, the default state is GPIOF3.
GPIOF4			41	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TXD1)				Output		TXD1 — The SCI1 transmit data output or transmit/receive in single wire operation.
(XB_OUT4)				Output		XB_OUT4 — Crossbar module output 4
						After reset, the default state is GPIOF4.
GPIOF5			42	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(RXD1)				Output		RXD1 — The SCI1 receive data input.
(XB_OUT5)				Output		XB_OUT5 — Crossbar module output 5
						After reset, the default state is GPIOF5.

- The 56F824x's startup address is located at 0x00 2000. The reset value of VBA is reset to a value of 0x0020 that corresponds to the address 0x00 2000.

By default, the chip reset address and COP reset address correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Table 48 on page 85 provides the MC56F825x/MC56F824x's interrupt table contents and interrupt priority structure.

4.5 Peripheral Memory-Mapped Registers

The locations of on-chip peripheral registers are part of the data memory map on the 56800E series. These locations may be accessed with the same addressing modes used for ordinary data memory. However, all peripheral registers should be read or written using word accesses only.

Table 12 summarizes the base addresses for the set of peripherals on the MC56F825x/MC56F824x devices. Peripherals are listed in order of the base address.

Table 12. Data Memory Peripheral Base Address Map Summary

Peripheral	Prefix	Base Address
Quad Timer A	TMRA	X:0x00 F000
Quad Timer B	TMRB	X:0x00 F040
Analog-to-Digital Converter	ADC	X:0x00 F080
Interrupt Controller	INTC	X:0x00 F0C0
System Integration Module	SIM	X:0x00 F0E0
Crossbar module	XBAR	X:0x00 F100
Computer Operating Properly module	COP	X:0x00 F110
On-Chip Clock Synthesis module	OCCS	X:0x00 F120
Power Supervisor	PS	X:0x00 F130
GPIO Port A	GPIOA	X:0x00 F140
GPIO Port B	GPIOB	X:0x00 F150
GPIO Port C	GPIOC	X:0x00 F160
GPIO Port D	GPIOD	X:0x00 F170
GPIO Port E	GPIOE	X:0x00 F180
GPIO Port F	GPIOF	X:0x00 F190
12-bit Digital-to-Analog Converter	DAC	X:0x00 F1A0
Analog Comparator A	CMPA	X:0x00 F1B0
Analog Comparator B	CMPB	X:0x00 F1C0
Analog Comparator C	CMPC	X:0x00 F1D0
Queued Serial Communication Interface 0	QSCI0	X:0x00 F1E0
Queued Serial Communication Interface 1	QSCI1	X:0x00 F1F0
Queued Serial Peripheral Interface	QSPI	X:0x00 F200
Inter-Integrated Circuit 0	I^2C0	X:0x00 F210
Inter-Integrated Circuit 1	I^2C1	X:0x00 F220

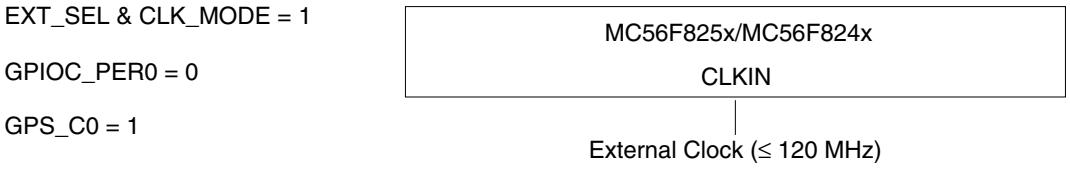


Figure 11. Connecting an External Clock Signal Using GPIO

5.5 Interrupt Controller

The MC56F825x/MC56F824x interrupt controller (INTC) module arbitrates the various interrupt requests (IRQs). When an interrupt of sufficient priority exists, the INTC signals to the 56800E core and provides the address to which to jump to service the interrupt.

The interrupt controller contains registers that allow each of the 66 interrupt sources to be set to one of three priority levels (excluding certain interrupt sources that have fixed priority) or to be disabled. Next, all interrupt requests of a given level are priority encoded to determine the lowest numeric value of the active interrupt requests for that level. Within a given priority level, the lowest vector number is the highest priority, and the highest vector number is the lowest priority.

Any two interrupt sources can be assigned to faster interrupts. Fast interrupts are described in the *DSP56800E Reference Manual*. The interrupt controller recognizes fast interrupts before the core does.

A fast interrupt is defined by:

1. Setting the priority of the interrupt as level 2 with the appropriate field in the Interrupt Priority Register (IPR) registers
2. Setting the Fast Interrupt Match (FIM*n*) register to the appropriate vector number
3. Setting the Fast Interrupt Vector Address Low (FIVAL*n)* and Fast Interrupt Vector Address High (FIVAH*n)* registers with the address of the code for the fast interrupt

When an interrupt occurs, its vector number is compared with the FIM0 and FIM1 register values. If a match occurs, and it is a level 2 interrupt, the INTC handles it as a Fast Interrupt. The INTC takes the vector address from the appropriate FIVAL*n* and FIVAH*n* registers, instead of generating an address that is an offset from the VBA.

The core then fetches the instruction from the indicated vector address instead of jumping to the vector table. If the instruction is not a JSR, the core starts its fast interrupt handling. Refer to section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for details.

Table 48 on page 85 provides the MC56F825x/MC56F824x's interrupt table contents and interrupt priority structure.

5.6 System Integration Module (SIM)

The SIM module consists of the glue logic that ties together the system-on-a-chip. It controls distribution of resets and clocks and provides a number of control features, including pin muxing control, inter-module connection control (such as connecting comparator output to eFlexPWM fault input), individual peripheral enabling/disabling, clock rate control for quad timers and SCIs, enabling peripheral operation in stop mode, and port configuration overwrite protection. For more information, refer to the device's reference manual.

The SIM is responsible for the following functions:

- Chip reset sequencing
- Core and peripheral clock control and distribution
- Stop/wait mode control
- System status control
- Registers containing the JTAG ID of the chip
- Controls for programmable peripheral and GPIO connections

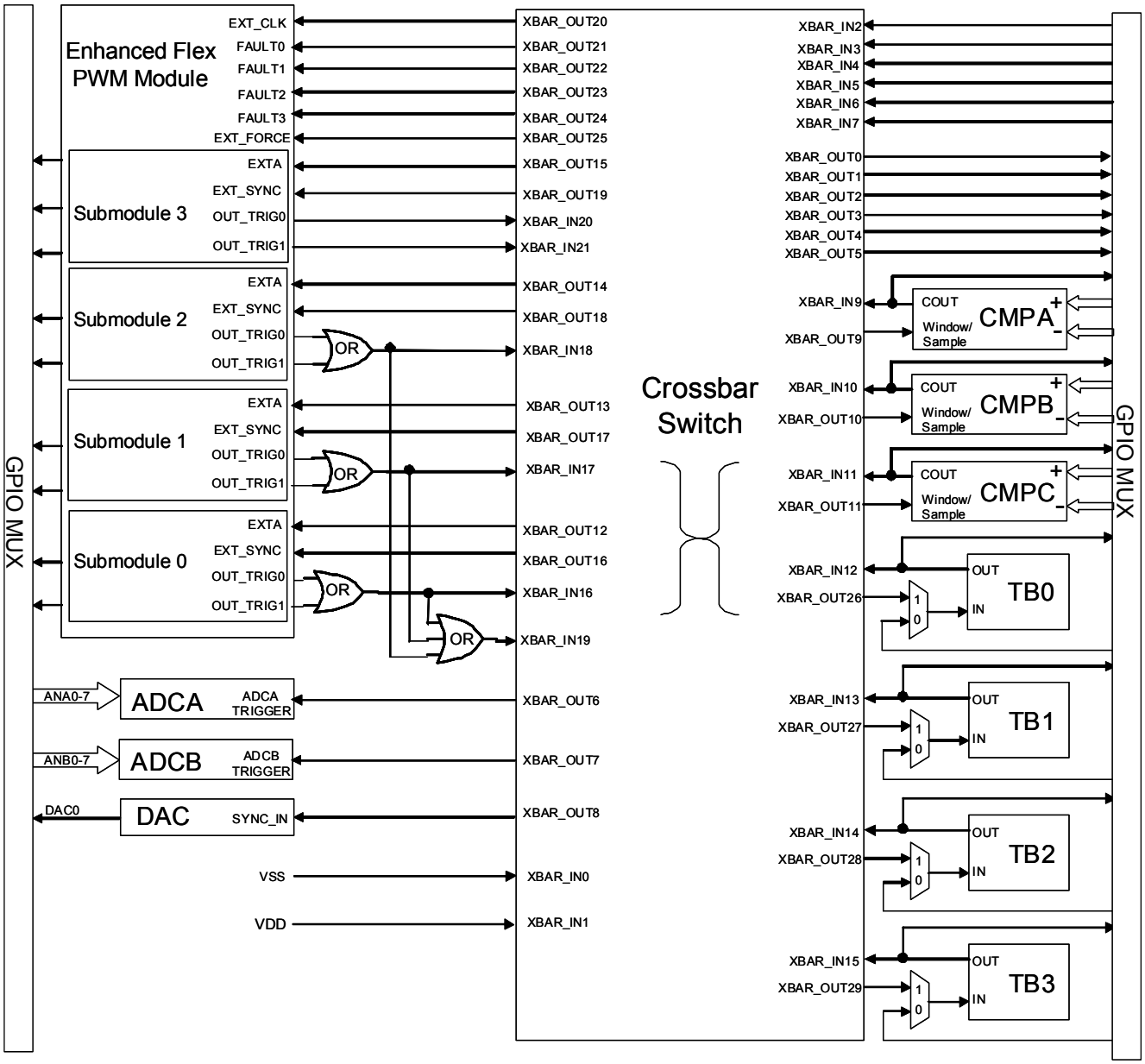


Figure 13. Crossbar Switch Connections

5.7.2.1 Crossbar Switch Inputs

Table 15 lists the signal assignments of Crossbar Switch inputs.

Table 16. Crossbar Output Signal Assignments (continued)

XBAR_OUTn	Output to	Function
XBAR_OUT7	ADCB	ADCB Trigger
XBAR_OUT8	DAC	12-bit DAC SYNC_IN
XBAR_OUT9	CMPA	Comparator A Window/Sample
XBAR_OUT10	CMPB	Comparator B Window/Sample
XBAR_OUT11	CMPC	Comparator C Window/Sample
XBAR_OUT12	PWM0 EXTA	eFlexPWM submodule 0 Alternate Control signal
XBAR_OUT13	PWM1 EXTA	eFlexPWM submodule 1 Alternate Control signal
XBAR_OUT14	PWM2 EXTA	eFlexPWM submodule 2 Alternate Control signal
XBAR_OUT15	PWM3 EXTA	eFlexPWM submodule 3 Alternate Control signal
XBAR_OUT16	PWM0 EXT_SYNC	eFlexPWM submodule 0 External Synchronization signal
XBAR_OUT17	PWM1 EXT_SYNC	eFlexPWM submodule 1 External Synchronization signal
XBAR_OUT18	PWM2 EXT_SYNC	eFlexPWM submodule 2 External Synchronization signal
XBAR_OUT19	PWM3 EXT_SYNC	eFlexPWM submodule 3 External Synchronization signal
XBAR_OUT20	PWM EXT_CLK	eFlexPWM External Clock signal
XBAR_OUT21	PWM FAULT0	eFlexPWM Module FAULT0
XBAR_OUT22	PWM FAULT1	eFlexPWM Module FAULT1
XBAR_OUT23	PWM FAULT2	eFlexPWM Module FAULT2
XBAR_OUT24	PWM FAULT3	eFlexPWM Module FAULT3
XBAR_OUT25	PWM FORCE	eFlexPWM External Output Force signal
XBAR_OUT26	TB0	Quad Timer B0 Input when SIM_GPS3[12] is set
XBAR_OUT27	TB1	Quad Timer B1 Input when SIM_GPS3[13] is set
XBAR_OUT28	TB2	Quad Timer B2 Input when SIM_GPS3[14] is set
XBAR_OUT29	TB3	Quad Timer B3 Input when SIM_GPS3[15] is set

5.7.3 Interconnection of PWM Module and ADC Module

In addition to how PWM0_EXTA, PWM1_EXTA, PWM2_EXTA, and PWM3_EXTA connect to crossbar outputs, the ADC conversion high/low limit compare results of sample0, sample1, and sample2 are used to drive PWM0_EXTB, PWM1_EXTB, and PWM2_EXTB, respectively. PWM3_EXTB is permanently tied to GND.

State of PWM0_EXTB:

- If the ADC conversion result in SAMPLE0 is greater than the value programmed into the high limit register 0, PWM0_EXTB is driven low.
- If the ADC conversion result in SAMPLE0 is less than the value programmed into the low limit register 0, PWM0_EXTB is driven high.

State of PWM1_EXTB:

- If the ADC conversion result in SAMPLE1 is greater than the value programmed into the high limit register 1, PWM1_EXTB is driven low.

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

See Section 8.1, "Thermal Design Considerations," for more detail on thermal design considerations.

7.5 Recommended Operating Conditions

This section contains information about recommended operating conditions.

Table 22. Recommended Operating Conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD}, V_{DDA}		3	3.3	3.6	V
ADC Reference Voltage High	V_{REFHx}		3.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		 0.001 0		 60 60	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2.0		5.5	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	-0.3		0.8	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
DAC Output Load Resistance	R_{LD}	Pin Group 5	3K			Ω
DAC Output Load Capacitance	C_{LD}	Pin Group 5			400	pf
Output Source Current High at V_{OH} min.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -4 -8	mA
Output Source Current Low (at V_{OL} max.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 4 8	mA
Ambient Operating Temperature (Extended Industrial)	T_A		-40		105	°C
Flash Endurance (Program Erase Cycles)	N_F	T_A = -40°C to 125°C	10,000		—	cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15		—	years
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	years

Table 23. DC Electrical Characteristics at Recommended Operating Conditions

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High (a) pull-up enabled or disabled	I_{IH}	Pin Groups 1, 2	—	0	+/- 2.5	µA	V_{IN} = 2.4 V to 5.5 V
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low[1] pull-up enabled pull-up disabled	I_{IL}	Pin Groups 1, 2	-15 —	-30 0	-60 +/- 2.5	µA	V_{IN} = 0 V
Internal Pull-Up Resistance	$R_{Pull-Up}$		60	110	220	kΩ	—
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0 V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0 V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40 mV	—	Typically V_{DDA} – 40 mV	V	—
Output Current [1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 2.5	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	—	0.35	—	V	—
Input Capacitance	C_{IN}		—	10	—	pF	—
Output Capacitance	C_{OUT}		—	10	—	pF	—

[1] See Figure 14.

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK
Pin Group 2: $\overline{\text{RESET}}$, GPIOA7
Pin Group 3: ADC and Comparator Analog Inputs
Pin Group 4: XTAL, EXTAL
Pin Group 5: DAC Analog Output

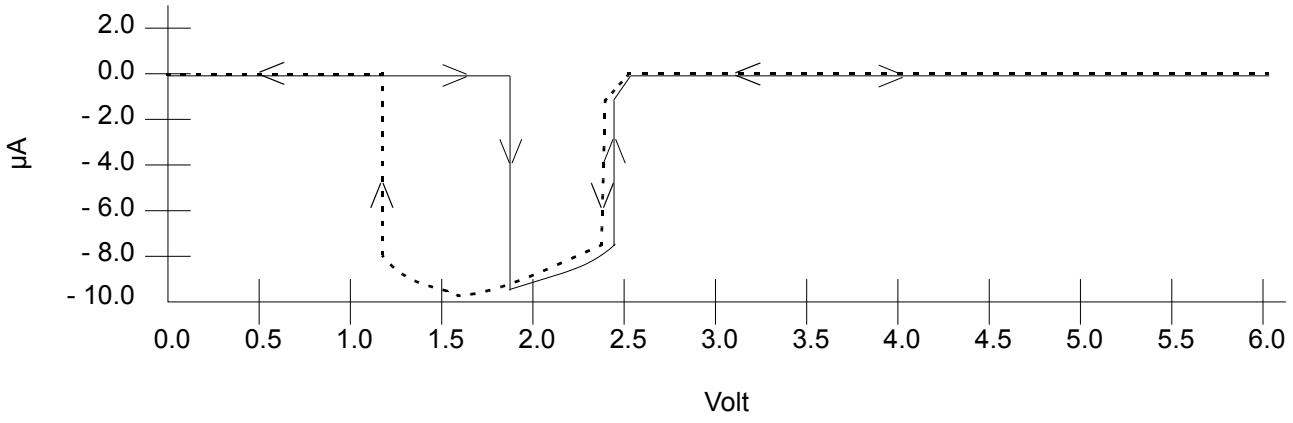


Figure 14. I_{IN}/I_{OZ} versus V_{IN} (Typical; Pull-Up Disabled)

Table 29. External Clock Operation Timing Requirements[1] (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
External clock input rise time[4]	t_{rise}	—	—	3	ns
External clock input fall time[5]	t_{fall}	—	—	3	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.85V_{DD}$	—	—	V
Input high voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

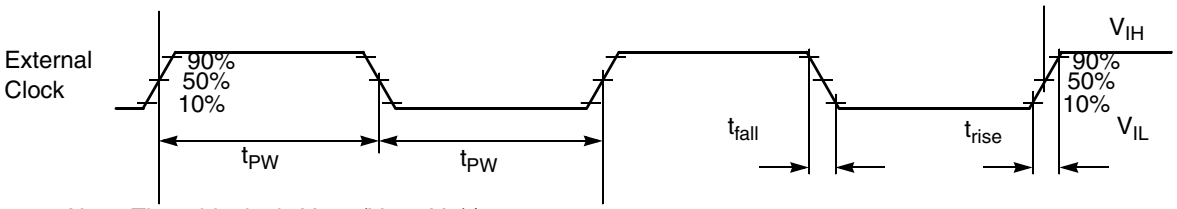
1 Parameters listed are guaranteed by design.

2 See Figure 17 for details on using the recommended connection of an external clock driver.

3 The chip may not function if the high or low pulse width is smaller than 6.25 ns.

4 External clock input rise time is measured from 10% to 90%.

5 External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 17. External Clock Timing

7.14 Phase Locked Loop Timing

Table 30. Phase Locked Loop Timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	4	8	8	MHz
PLL output frequency[2]	f_{op}	120	—	240	MHz
PLL lock time[3] [4]	t_{plls}	—	40	100	µs
Accumulated jitter using an 8 MHz external crystal as the PLL source[5]	J_A	—	—	TBD	%
Cycle-to-cycle jitter	$t_{jitterpll}$	—	350	—	ps

1 An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.

2 The core system clock operates at 1/6 of the PLL output frequency.

3 This is the time required after the PLL is enabled to ensure reliable operation.

4 From powerdown to powerup state at 60 MHz system clock state.

5 This is measured on the CLKO signal (programmed as system clock) over 264 system clocks at 60 MHz system clock frequency and using an 8 MHz oscillator frequency.

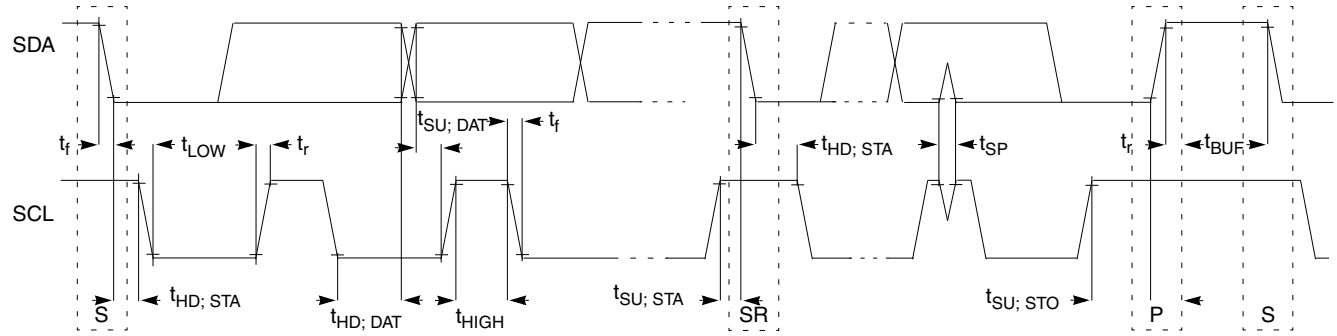


Figure 27. Timing Definition for Standard Mode Devices on the I^2C Bus

7.22 JTAG Timing

Table 38. JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation[1]	f_{OP}	DC	SYS_CLK/8	MHz	Figure 28
TCK clock pulse width	t_{PW}	50	—	ns	Figure 28
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 29
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 29
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 29
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 29

[1] TCK frequency of operation must be less than 1/8 the processor rate.

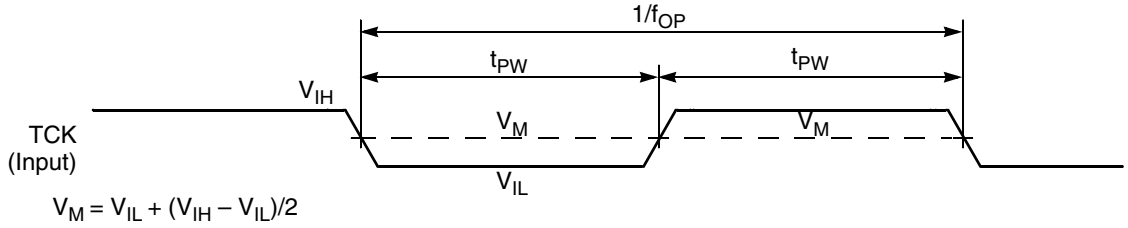


Figure 28. Test Clock Input Timing Diagram

Use the following list of considerations to assure correct operation of the MC56F825x/MC56F824x:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the MC56F825x/MC56F824x and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} is recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with V_{DDA} and V_{SSA} traces.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ to 10 kΩ; the capacitor value should be in the range of 0.22 µF to 4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if a JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input state with internal pullup enabled. The typical value of internal pullup is around 110 kΩ. These internal pullups can be disabled by software.
- To eliminate PCB trace impedance effect, each ADC input should have an RC filter of no less than 33 pF 10 Ω.
- External clamp diodes on analog input pins are recommended.

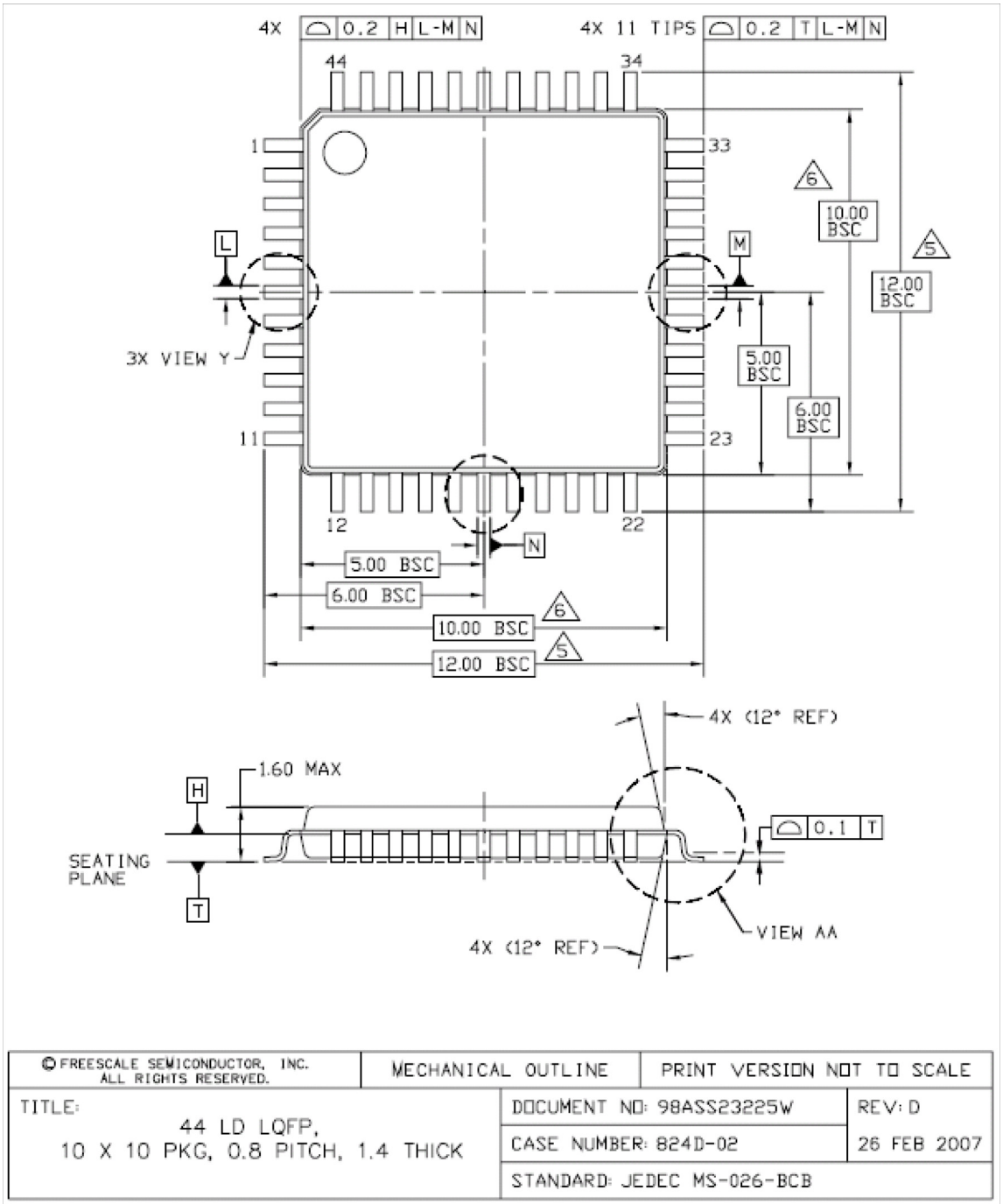
9 Ordering Information

Table 46 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order devices.

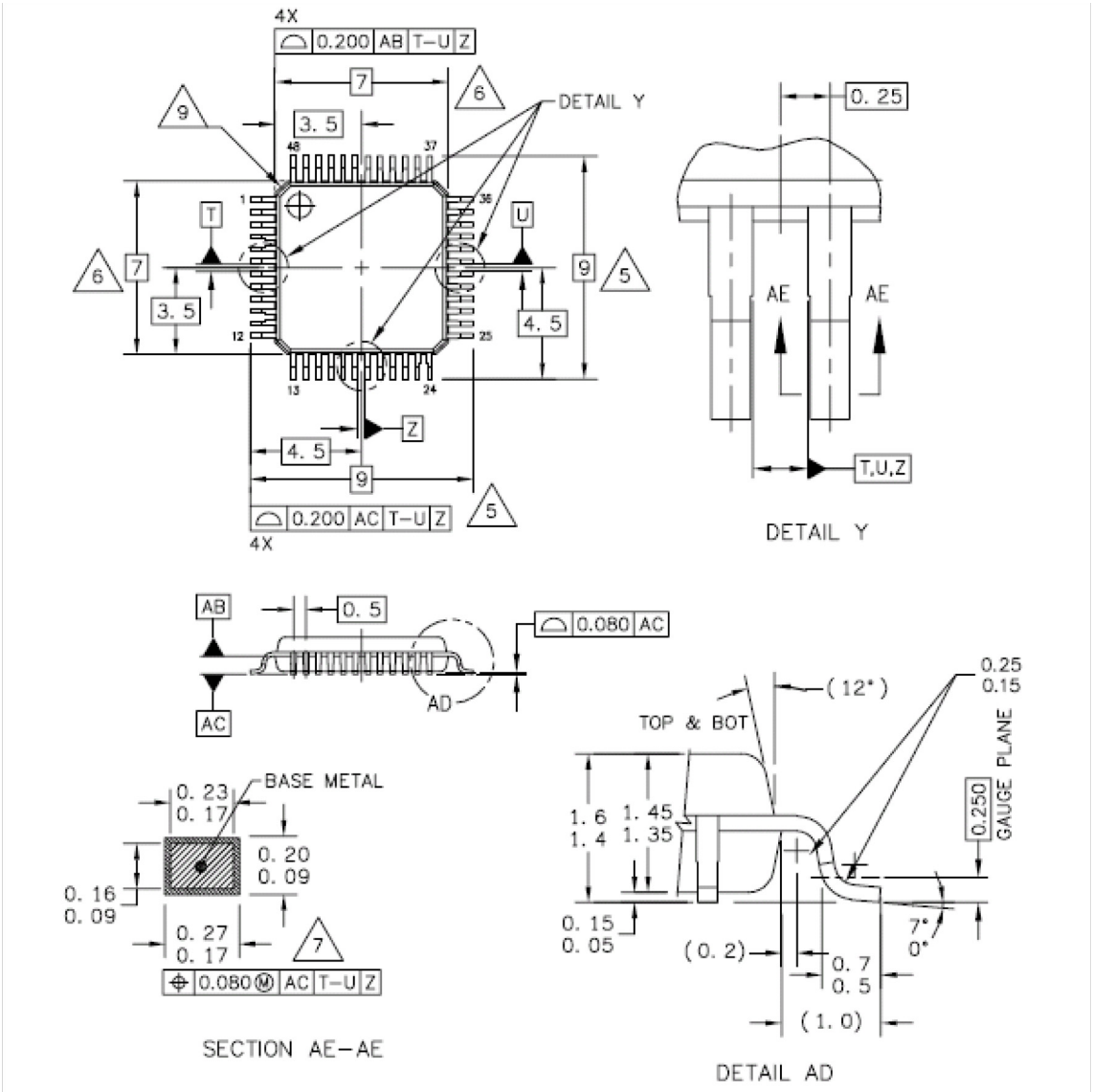
10 Package Mechanical Outline Drawings

To ensure you have the latest version of a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number (shown in the following sections for each package).

10.1 44-pin LQFP



10.2 48-pin LQFP



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TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	DOCUMENT NO: 98ASH00962A	REV: G
	CASE NUMBER: 932-03	14 APR 2005
	STANDARD: JEDEC MS-026-BBC	

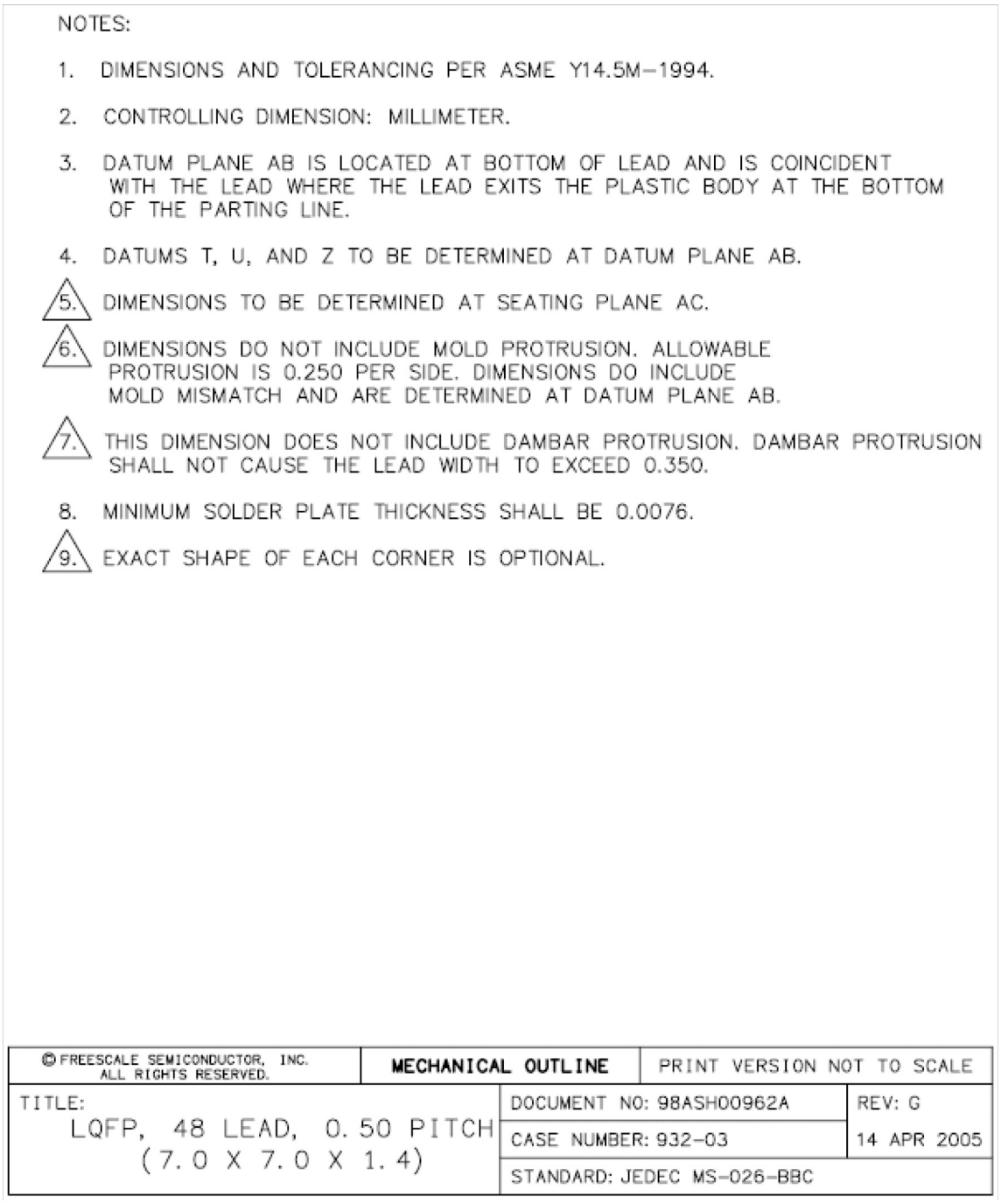

Figure 33. 56F8246 and 56F8256 48-Pin LQFP Mechanical Information

Table 48. Interrupt Vector Table Contents[1] (continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
CAN	25	0 - 2	P:0x32	CAN Error Interrupt
CAN	26	0 - 2	P:0x34	CAN Wake-Up Interrupt
QSCI1	27	0 - 2	P:0x36	QSCI1 Receiver Overrun/Errors
QSCI1	28	0 - 2	P:0x38	QSCI1 Receiver Full
QSCI1	29	0 - 2	P:0x3A	QSCI1 Transmitter Idle
QSCI1	30	0 - 2	P:0x3C	QSCI1 Transmitter Empty
QSCI0	31	0 - 2	P:0x3E	QSCI0 Receiver Overrun/Errors
QSCI0	32	0 - 2	P:0x40	QSCI0 Receiver Full
QSCI0	33	0 - 2	P:0x42	QSCI0 Transmitter Idle
QSCI0	34	0 - 2	P:0x44	QSCI0 Transmitter Empty
QSPI	35	0 - 2	P:0x46	SPI Transmitter Empty
QSPI	36	0 - 2	P:0x48	SPI Receiver Full
I^2C1	37	0 - 2	P:0x4A	I^2C1 Interrupt
I^2C0	38	0 -2	P:0x4C	I^2C0 Interrupt
TMRA3	39	0 -2	P:0x4E	Quad Timer A, Channel 3 Interrupt
TMRA2	40	0 -2	P:0x50	Quad Timer A, Channel 2 Interrupt
TMRA1	41	0 -2	P:0x52	Quad Timer A, Channel 1 Interrupt
TMRA0	42	0 -2	P:0x54	Quad Timer A, Channel 0 Interrupt
eFlexPWM	43	0 -2	P:0x56	PWM Fault
eFlexPWM	44	0 -2	P:0x58	PWM Reload Error
eFlexPWM	45	0 -2	P:0x5A	PWM Sub-Module 3 Reload
eFlexPWM	46	0 -2	P:0x5C	PWM Sub-Module 3 input capture
eFlexPWM	47	0 -2	P:0x5E	PWM Sub-Module 3 Compare
eFlexPWM	48	0 -2	P:0x60	PWM Sub-Module 2 Reload
eFlexPWM	49	0 -2	P:0x62	PWM Sub-Module 2 Compare
eFlexPWM	50	0 -2	P:0x64	PWM Sub-Module 1 Reload
eFlexPWM	51	0 -2	P:0x66	PWM Sub-Module 1 Compare
eFlexPWM	52	0 -2	P:0x68	PWM Sub-Module 0 Reload
eFlexPWM	53	0 -2	P:0x6A	PWM Sub-Module 0Compare
FM	54	0 -2	P:0x6C	Flash Memory Access Error
FM	55	0 -2	P:0x6E	Flash Memory Programming Command Complete
FM	56	0 -2	P:0x70	Flash Memory Buffer Empty Request
CMPC	57	0 - 2	P:0x72	Comparator C Rising/Falling Flag
CMPB	58	0 - 2	P:0x74	Comparator B Rising/Falling Flag

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