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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8247mlh

3.2 Pin Assignment

Figure 3 shows the pin assignments of the 56F8245 and 56F8255's 44-pin low-profile quad flat pack (44LQFP). Figure 4 shows the pin assignments of the 56F8246 and 56F8256's 48-pin low-profile quad flat pack (48LQFP). Figure 5 shows the pin assignments of the 56F8247 and 56F8257's 64-pin low-profile quad flat pack (64LQFP).

NOTE

The CANRX and CANTX signals of the MSCAN module are not available on the MC56F824x devices.

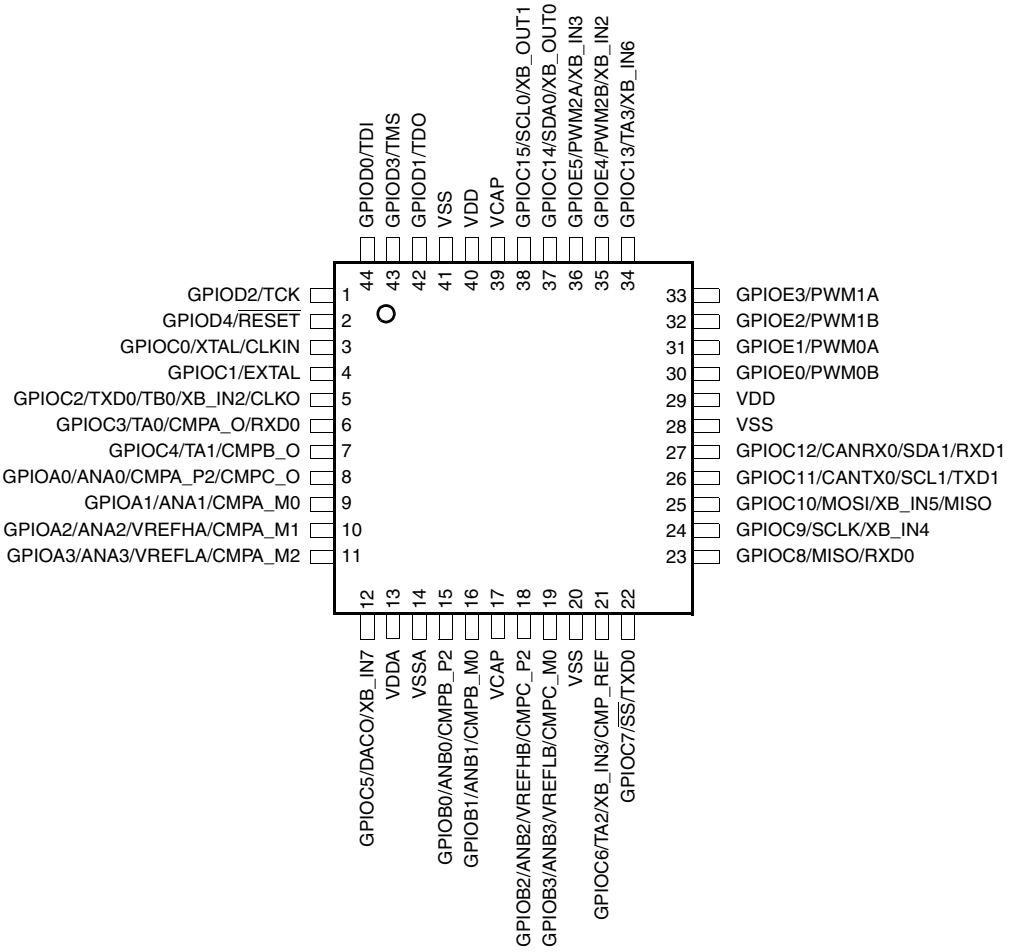


Figure 3. Top View: 56F8245 and 56F8255 44-Pin LQFP Package

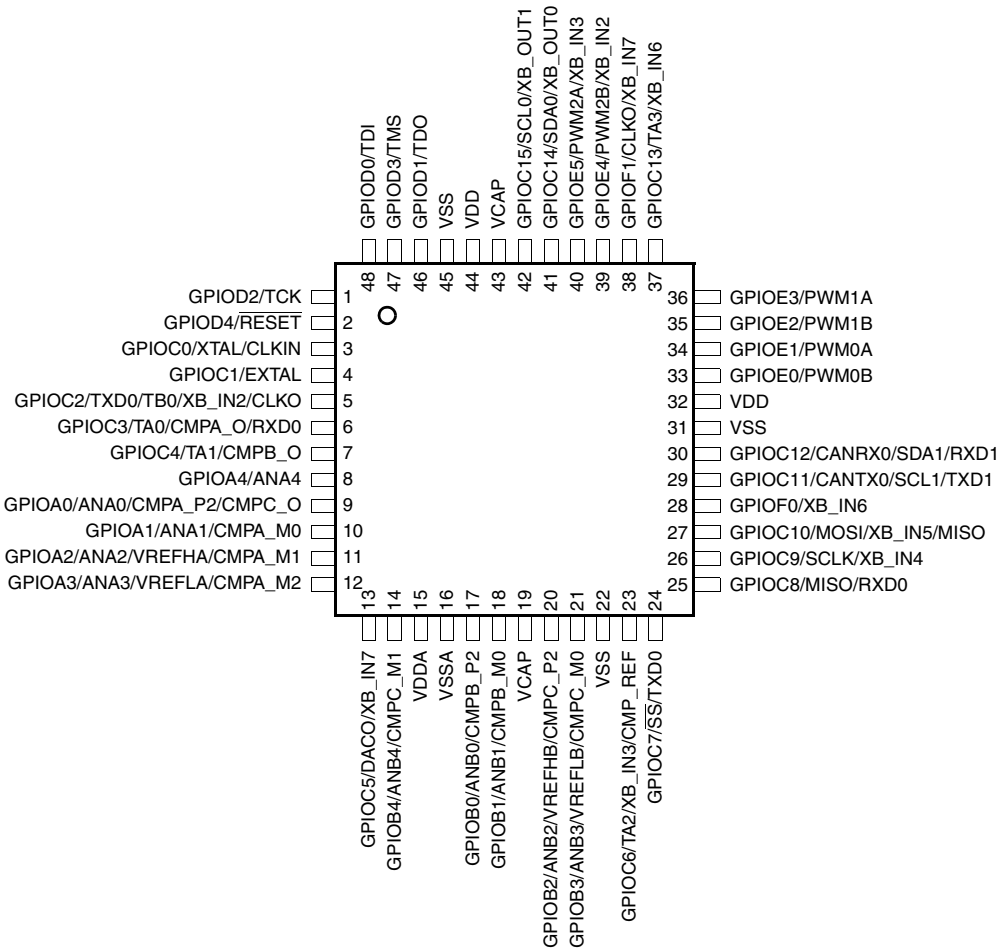


Figure 4. Top View: 56F8246 and 56F8256 48-Pin LQFP Package

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOF6 *(TB2)* *(PWM3X)*			58	Input/ Output Input/ Output Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. TB2 — Quad timer module B channel 2 input/output. PWM3X — Enhanced PWM submodule 3 output X or input capture X After reset, the default state is GPIOF6.
GPIOF7 *(TB3)*			59	Input/ Output Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. TB3 — Quad timer module B channel 3 input/output. After reset, the default state is GPIOF7.
GPIOF8 *(RXD0)* *(TB1)*			6	Input/ Output Input Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. RXD0 — The SCI0 receive data input. TB1 — Quad timer module B channel 1 input/output. After reset, the default state is GPIOF8.

1 If CLKIN is selected as the device's external clock input, both the GPS_C0 bit in GPS1 and the EXT_SEL bit in the OCCS oscillator control register (OSCTL) must be set. In this case, it is also recommended to power down the crystal oscillator.

4 Memory Maps

4.1 Introduction

The MC56F825x/MC56F824x device is based on the 56800E core. It uses a dual Harvard-style architecture with two independent memory spaces for data and program. On-chip RAM is shared by both data and program spaces; flash memory is used only in program space.

This section provides memory maps for:

- Program address space, including the interrupt vector table
- Data address space, including the EOnCE memory and peripheral memory maps

On-chip memory sizes for the device are summarized in Table 6. Flash memories' restrictions are identified in the "Use Restrictions" column of Table 6.

Table 11. 56F8245/56 Data Memory Map[1]

Begin/End Address	Memory Allocation
X:0xFF FFFF X:0xFF FF00	EOnCE 256 locations allocated
X:0xFF FEFF X:0x01 0000	RESERVED
X:0x00 FFFF X:0x00 F000	On-Chip Peripherals 4096 locations allocated
X:0x00 EFFF X:0x00 8C00	RESERVED
X:0x00 8BFF X:0x00 8000	On-Chip Data RAM Alias
X:0x00 7FFF X:0x00 0C00	RESERVED
X:0x00 0BFF X:0x00 0000	On-Chip Data RAM 6 KB[2]

1 All addresses are 16-bit word addresses.

2 This RAM is shared with program space starting at P: 0x00 8000. See Figure 8.

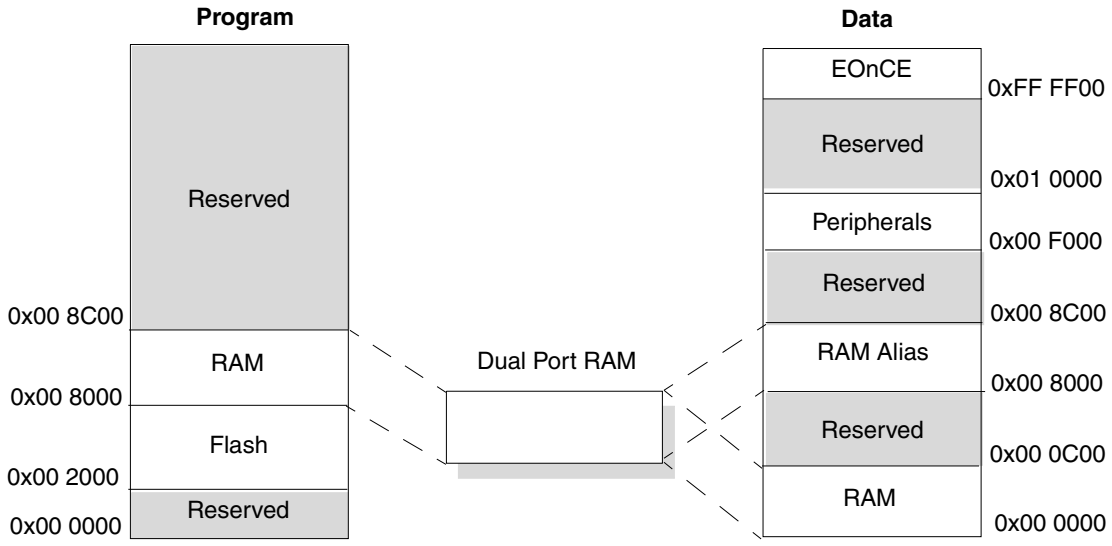


Figure 8. 56F8245/46 Dual Port RAM Map

4.4 Interrupt Vector Table and Reset Vector

The location of the vector table is determined by the vector base address register (VBA). The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower seven bits are determined based on the highest priority interrupt and are then appended to VBA before presenting the full VAB to the core. Refer to the device's reference manual for details.

The reset startup addresses of 56F824x and 56F825x are different.

- The 56F825x's startup address is located at 0x00 0000. The reset value of VBA is reset to a value of 0x0000 that corresponds to the address 0x00 0000.

Table 13. EOnCE Memory Map

Address	Register Abbreviation	Register Name
X:0xFF FF91–X:0xFF FF90	OBMSK (32 bits)	Breakpoint Unit Mask Register 2
X:0xFF FF8F		Reserved
X:0xFF FF8E	OBCNTR	EOnCE Breakpoint Unit Counter
X:0xFF FF8D		Reserved
X:0xFF FF8C		Reserved
X:0xFF FF8B		Reserved
X:0xFF FF8A	OESCR	External Signal Control Register
X:0xFF FF89 –X:0xFF FF00		Reserved

5 General System Control Information

5.1 Overview

This section discusses power pins, reset sources, interrupt sources, clock sources, the system integration module (SIM), ADC synchronization, and JTAG/EOnCE interfaces.

5.2 Power Pins

V_{DD}, V_{SS} and V_{DDA}, V_{SSA} are the primary power supply pins for the device. The voltage source supplies power to all on-chip peripherals, I/O buffer circuitry, and internal voltage regulators. The device has multiple internal voltages to provide regulated lower-voltage sources for the peripherals, core, memory, and on-chip relaxation oscillators.

Typically, at least two separate capacitors are across the power pins to bypass the glitches and provide bulk charge storage. In this case, a bulk electrolytic or tantalum capacitor, such as a 10 µF tantalum capacitor, should provide bulk charge storage for the overall system, and a 0.1 µF ceramic bypass capacitor should be located as near to the device power pins as is practical to suppress high-frequency noise. Each pin must have a bypass capacitor for optimal noise suppression.

V_{DDA} and V_{SSA} are the analog power supply pins for the device. This voltage source supplies power to the ADC, PGA, and CMP modules. A 0.1 µF ceramic bypass capacitor should be located as near to the device V_{DDA} and V_{SSA} pins as is practical to suppress high-frequency noise. V_{DDA} and V_{SSA} are also the voltage reference high and voltage reference low inputs, respectively, for the ADC module.

5.3 Reset

Resetting the device provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values, and the program counter is loaded from the reset vector. On-chip peripheral modules are disabled and I/O pins are initially configured at the reset status shown in Table 5 on page 18.

The MC56F825x/MC56F824x has the following sources for reset:

- Power-on reset (POR)
- Partial power-down reset (PPD)
- Low-voltage detect (LVD)
- External pin reset (EXTR)
- Computer operating properly loss of reference reset (COP_LOR)
- Computer operating properly time-out reset (COP_CPU)

Table 14. Connections by Comparator Inputs (continued)

Comparator Input	Comparator A	Comparator B	Comparator B
M0 (from package pin)	CMPA_M0	CMPB_M0	CMPC_M0
M1 (from package pin)	CMPA_M1	CMPB_M1	CMPC_M1
M2 (from package pin)	CMPA_M2	CMPB_M2	CMPC_M2
M3 (from internal)	12-bit DAC	12-bit DAC	12-bit DAC

5.7.2 Crossbar Switch Connections

The Crossbar Switch module provides a generic mechanism for making connections between on-chip peripherals as well as between peripherals and pins. It provides a purely combinational path from input to output. The module groups 30 identical multiplexes with 22 shared inputs. All Crossbar control registers that are used to select one of the 22 input signals to output are write protected. Control of the write protection setting is in the SIM_PROT register.

In general, the crossbar module connects the Enhanced Flex PWM, ADC, Quad Timers, and comparators together, which allows synchronization between PWM pulse generation and ADC sampling. In addition, several crossbar inputs and outputs are routed to package pins. For example, the user can define an XB_INn pin as a PWM fault protection input that is routed to the PWM module through the crossbar, increasing the flexibility of pin use and reducing the complexity of PCB layout.

Table 16. Crossbar Output Signal Assignments (continued)

XBAR_OUTn	Output to	Function
XBAR_OUT7	ADCB	ADCB Trigger
XBAR_OUT8	DAC	12-bit DAC SYNC_IN
XBAR_OUT9	CMPA	Comparator A Window/Sample
XBAR_OUT10	CMPB	Comparator B Window/Sample
XBAR_OUT11	CMPC	Comparator C Window/Sample
XBAR_OUT12	PWM0 EXTA	eFlexPWM submodule 0 Alternate Control signal
XBAR_OUT13	PWM1 EXTA	eFlexPWM submodule 1 Alternate Control signal
XBAR_OUT14	PWM2 EXTA	eFlexPWM submodule 2 Alternate Control signal
XBAR_OUT15	PWM3 EXTA	eFlexPWM submodule 3 Alternate Control signal
XBAR_OUT16	PWM0 EXT_SYNC	eFlexPWM submodule 0 External Synchronization signal
XBAR_OUT17	PWM1 EXT_SYNC	eFlexPWM submodule 1 External Synchronization signal
XBAR_OUT18	PWM2 EXT_SYNC	eFlexPWM submodule 2 External Synchronization signal
XBAR_OUT19	PWM3 EXT_SYNC	eFlexPWM submodule 3 External Synchronization signal
XBAR_OUT20	PWM EXT_CLK	eFlexPWM External Clock signal
XBAR_OUT21	PWM FAULT0	eFlexPWM Module FAULT0
XBAR_OUT22	PWM FAULT1	eFlexPWM Module FAULT1
XBAR_OUT23	PWM FAULT2	eFlexPWM Module FAULT2
XBAR_OUT24	PWM FAULT3	eFlexPWM Module FAULT3
XBAR_OUT25	PWM FORCE	eFlexPWM External Output Force signal
XBAR_OUT26	TB0	Quad Timer B0 Input when SIM_GPS3[12] is set
XBAR_OUT27	TB1	Quad Timer B1 Input when SIM_GPS3[13] is set
XBAR_OUT28	TB2	Quad Timer B2 Input when SIM_GPS3[14] is set
XBAR_OUT29	TB3	Quad Timer B3 Input when SIM_GPS3[15] is set

5.7.3 Interconnection of PWM Module and ADC Module

In addition to how PWM0_EXTA, PWM1_EXTA, PWM2_EXTA, and PWM3_EXTA connect to crossbar outputs, the ADC conversion high/low limit compare results of sample0, sample1, and sample2 are used to drive PWM0_EXTB, PWM1_EXTB, and PWM2_EXTB, respectively. PWM3_EXTB is permanently tied to GND.

State of PWM0_EXTB:

- If the ADC conversion result in SAMPLE0 is greater than the value programmed into the high limit register 0, PWM0_EXTB is driven low.
- If the ADC conversion result in SAMPLE0 is less than the value programmed into the low limit register 0, PWM0_EXTB is driven high.

State of PWM1_EXTB:

- If the ADC conversion result in SAMPLE1 is greater than the value programmed into the high limit register 1, PWM1_EXTB is driven low.

- If the ADC conversion result in SAMPLE1 is less than the value programmed into the low limit register 1, PWM1_EXTB is driven high.

State of PWM2_EXTB:

- If the ADC conversion result in SAMPLE2 is greater than the value programmed into the high limit register 2, PWM2_EXTB is driven low.
- If the ADC conversion result in SAMPLE2 is less than the value programmed into the low limit register 2, PWM2_EXTB is driven high.

5.8 Joint Test Action Group (JTAG)/Enhanced On-Chip Emulator (EOnCE)

The 56800E family includes extensive integrated support for application software development and real-time debugging. Two modules, the Enhanced On-Chip Emulation (EOnCE) module and the core test access port (TAP, commonly called the JTAG port), work together to provide these capabilities. Both are accessed through a common 4-pin JTAG/EOnCE interface. These modules allow you to insert the MC56F825x/MC56F824x into a target system while retaining debug control. This capability is especially important for devices without an external bus, because it eliminates the need for a costly cable to bring out the footprint of the chip, as is required by a traditional emulator system.

The 56800E's EOnCE module is a Freescale-designed module for developing and debugging application software used with the chip. This module allows non-intrusive interaction with the CPU and is accessible through the pins of the JTAG interface or by software program control of the 56800E core. Among the many features of the EOnCE module is support, in real-time program execution, for data communication between the controller and the host software development and debug systems. Other features allow for hardware breakpoints, the monitoring and tracking of program execution, and the ability to examine and modify the contents of registers, memory, and on-chip peripherals, all in a special debug environment. No user-accessible resources must be sacrificed to perform debugging operations.

The 56800E's JTAG port provides an interface for the EOnCE module to the JTAG pins. The Joint Test Action Group (JTAG) boundary scan is an IEEE 1149.1 standard methodology enabling access to test features using a test access port (TAP). A JTAG boundary scan consists of a TAP controller and boundary scan registers. Contact your Freescale sales representative or authorized distributor for device-specific BSDL information.

NOTE

In normal operation, an external pullup on the TMS pin is highly recommend to place the JTAG state machine in reset state (if this pin is not configured as GPIO).

6 Security Features

The MC56F825x/MC56F824x offers security features intended to prevent unauthorized users from gaining access to and reading the contents of the flash memory (FM) array. The MC56F825x/MC56F824x's flash memory security consists of several hardware interlocks.

After flash memory security is set, the application software can allow an authorized user to access on-chip memory by including a user-defined software subroutine that reads and transfers the contents of internal memory via peripherals. This application software can communicate over a serial port, for example, to validate the authenticity of the requested access and then to grant it until the next device reset. The system designer must use discretion when deciding whether to support this type of "back door" access technique.

6.1 Operation with Security Enabled

After you have programmed flash with the application code, or as part of programming the flash with the application code, you can secure the MC56F825x/MC56F824x by programming the values 1 and 0 into bits 1 and 0, respectively, of program memory location 0x00_7FF7. The CodeWarrior IDE menu flash lock command can also accomplish this task. The nonvolatile security

word ensures that the device remains secure after the next reset (caused, for example, by the device powering down). Refer to the flash memory section of the device's reference manual for details.

When flash security mode is enabled, the MC56F825x/MC56F824x disables the core's EOnCE debug capabilities. Normal program execution is otherwise unaffected.

6.2 Flash Access Lock and Unlock Mechanisms

Several methods effectively lock or unlock the on-chip flash.

6.2.1 Disabling EOnCE Access

You can read on-chip flash by issuing commands across the EOnCE port, which is the debug interface for the 56800E core. The TCK, TMS, TDO, and TDI pins compose a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG port is active and provides the chip's boundary scan capability and access to the ID register. However, proper implementation of flash security blocks any attempt to access the internal flash memory via the EOnCE port when security is enabled. This protection is effective when the device comes out of reset, even prior to the execution of any code at startup.

6.2.2 Flash Lockout Recovery Using JTAG

If the device is secured, one lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field. The erasure disables security by clearing the protection register. This approach does not compromise security. The entire contents of your secured code stored in flash are erased before the next reset or power-up sequence, when security becomes disabled.

To start the lockout recovery sequence via JTAG, first shift the JTAG public instruction (LOCKOUT_RECOVERY) into the chip-level TAP controller's instruction register. Then shift the clock divider value into the corresponding 7-bit data register. Finally, the TAP controller must enter the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence is complete. Refer to the device's reference manual for details, or contact Freescale.

NOTE

After completion of the lockout recovery sequence, you must reset the JTAG TAP controller and the device to return to normal unsecured operation. A power-on reset resets both.

6.2.3 Flash Lockout Recovery Using CodeWarrior

You can use CodeWarrior to unlock a device by selecting the following items in the indicated sequence:

1. Debug menu
2. DSP56800E
3. Unlock Flash

You can accomplish the same task with another CodeWarrior mechanism that uses the device's memory configuration file: the command "Unlock_Flash_on_Connect 1" in the .cfg file.

This lockout recovery mechanism completely erases the internal flash contents, including the configuration field, thereby disabling security (the protection register is cleared).

7.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed.

CAUTION

Stress beyond the limits specified in Table 17 may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this section apply over the ambient temperature range of –40 ºC to +105 ºC over the following supply ranges: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0$ V to 3.6 V, CL ≤ 50 pF, $f_{OP} = 60$ MHz.

For functional operating conditions, refer to the remaining tables in the section.

Table 17. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply Voltage Range	V_{DD}		- 0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		- 0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		- 0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		- 0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Groups 1, 2	- 0.3	6.0	V
Oscillator Voltage Range	V_{OSC}	Pin Group 4	- 0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	- 0.3	4.0	V
Input clamp current, per pin ($V_{IN} < 0$)[1]	V_{IC}		—	-20.0	mA
Output clamp current, per pin ($V_O < 0$)[1]	V_{OC}		—	-20.0	mA
Output Voltage Range (Normal Push-Pull mode)	V_{OUT}	Pin Group 1	- 0.3	4.0	V
Output Voltage Range (Open Drain mode)	V_{OUTOD}	Pin Group 2	- 0.3	6.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	- 0.3	4.0	V
Ambient Temperature Industrial	T_A		- 40	105	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		- 55	150	°C

[1] Continuous clamp current per pin is –2.0 mA

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC and Comparator Analog Inputs

Pin Group 4: XTAL, EXTAL

Pin Group 5: DAC analog output

Table 29. External Clock Operation Timing Requirements[1] (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
External clock input rise time[4]	t_{rise}	—	—	3	ns
External clock input fall time[5]	t_{fall}	—	—	3	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.85V_{DD}$	—	—	V
Input high voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

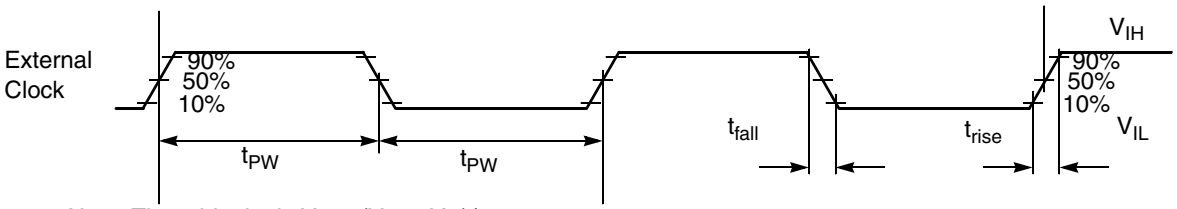
1 Parameters listed are guaranteed by design.

2 See Figure 17 for details on using the recommended connection of an external clock driver.

3 The chip may not function if the high or low pulse width is smaller than 6.25 ns.

4 External clock input rise time is measured from 10% to 90%.

5 External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 17. External Clock Timing

7.14 Phase Locked Loop Timing

Table 30. Phase Locked Loop Timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	4	8	8	MHz
PLL output frequency[2]	f_{op}	120	—	240	MHz
PLL lock time[3] [4]	t_{plls}	—	40	100	µs
Accumulated jitter using an 8 MHz external crystal as the PLL source[5]	J_A	—	—	TBD	%
Cycle-to-cycle jitter	$t_{jitterpll}$	—	350	—	ps

1 An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.

2 The core system clock operates at 1/6 of the PLL output frequency.

3 This is the time required after the PLL is enabled to ensure reliable operation.

4 From powerdown to powerup state at 60 MHz system clock state.

5 This is measured on the CLKO signal (programmed as system clock) over 264 system clocks at 60 MHz system clock frequency and using an 8 MHz oscillator frequency.

7.15 External Crystal or Resonator Requirement

Table 31. Crystal or Resonator Requirement

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation	f_{XOSC}	4	8	16	MHz

7.16 Relaxation Oscillator Timing

Table 32. Relaxation Oscillator Timing

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
Relaxation oscillator output frequency[1] Normal Mode Standby Mode	f_{op}	—	 8.05 400	—	 MHz kHz
Relaxation oscillator stabilization time[2]	t_{roscs}	—	1	3	ms
Cycle-to-cycle jitter. This is measured on the CLKO signal (programmed prescaler_clock) over 264 clocks[3]	$t_{jitterrosc}$	—	400	—	ps
Variation over temperature –40°C to 150°C[4]		—	+1.5 to –1.5	+3.0 to –3.0	%
Variation over temperature 0°C to 105°C[4]		—	0 to +1	+2.0 to –2.0	%

1 Output frequency after factory trim.

2 This is the time required from standby to normal mode transition.

3 J_A is required to meet QSCI requirements.

4 See Figure 18.

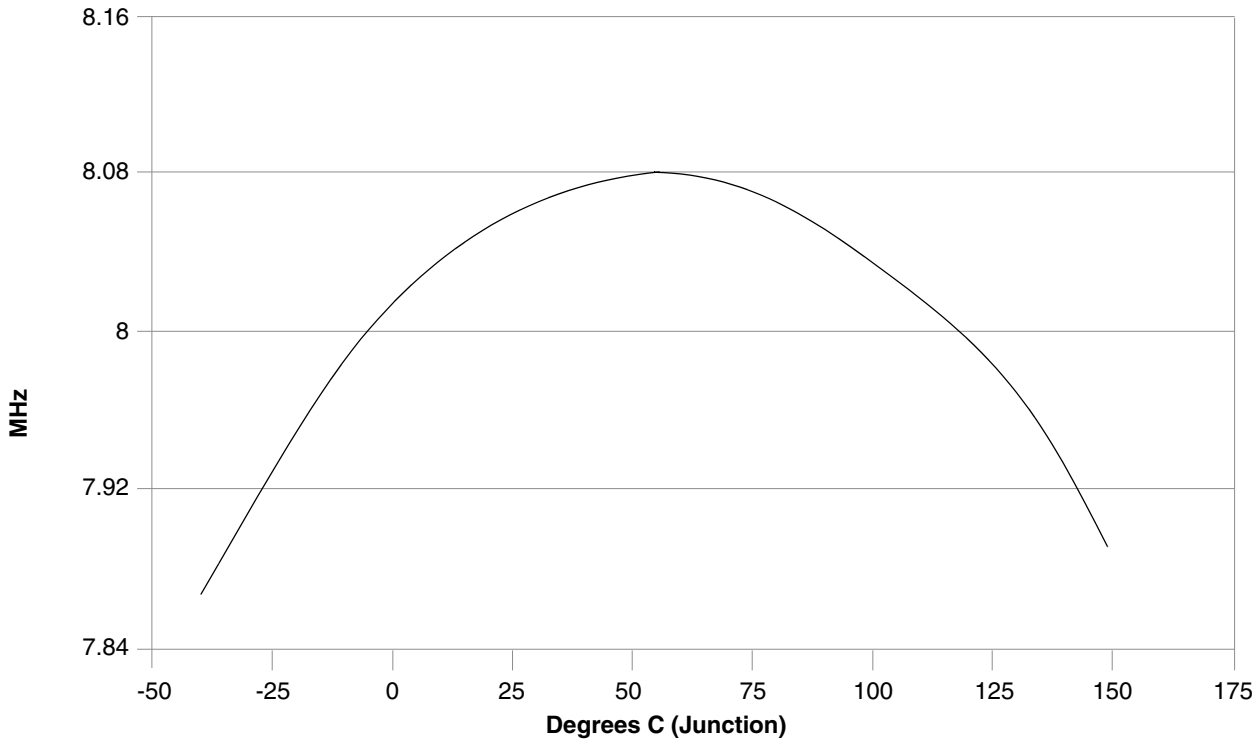


Figure 18. Relaxation Oscillator Temperature Variation (Typical) After Trim

7.20 Freescale's Scalable Controller Area Network (MSCAN)

Table 36. MSCAN Timing

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
Bus Wake-up detection	T_{WAKEUP}	T_{IPBUS}	—	µs

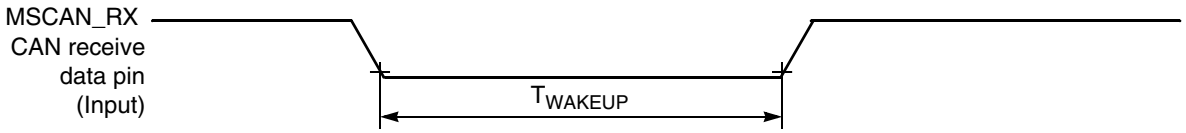


Figure 26. Bus Wake-up Detection

7.21 Inter-Integrated Circuit Interface (I^2C) Timing

Table 37. I^2C Timing

Characteristic	Symbol	Standard Mode		Unit
		Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7	—	µs
Data hold time for I^2C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250[3]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	ns
Fall time of SDA and SCL signals	t_f	—	300	ns
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	ns

1 The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

2 The maximum $t_{HD;\ DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

3 A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\ DAT}$ > = 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.

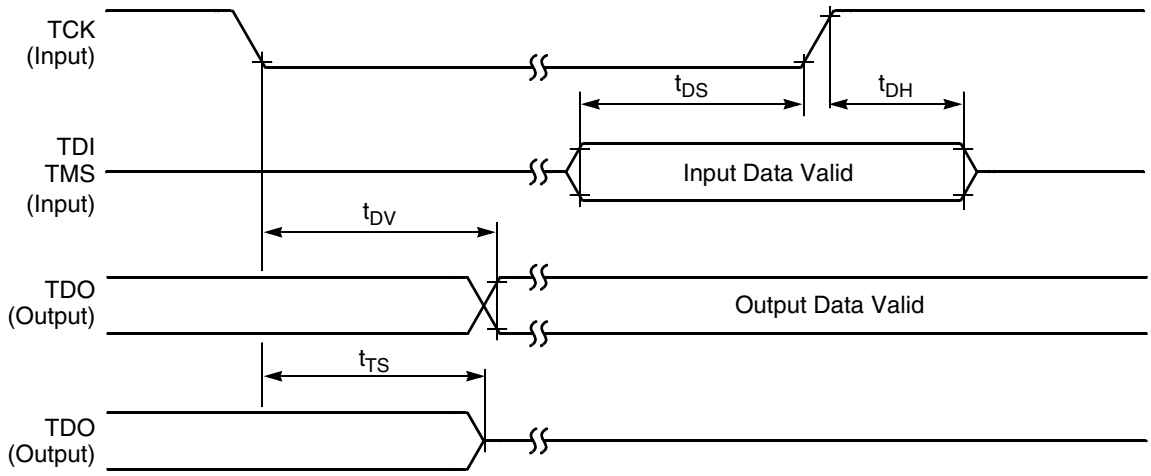


Figure 29. Test Access Port Timing Diagram

7.23 Quad Timer Timing

Table 39. Timer Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	Figure 30
Timer input high/low period	P_{INHL}	1T + 3	—	ns	Figure 30
Timer output period	P_{OUT}	125	—	ns	Figure 30
Timer output high/low period	P_{OUTHL}	50	—	ns	Figure 30

1 In the formulas listed, T = the clock cycle. For 32 MHz operation, T = 31.25 ns.

2. Parameters listed are guaranteed by design.

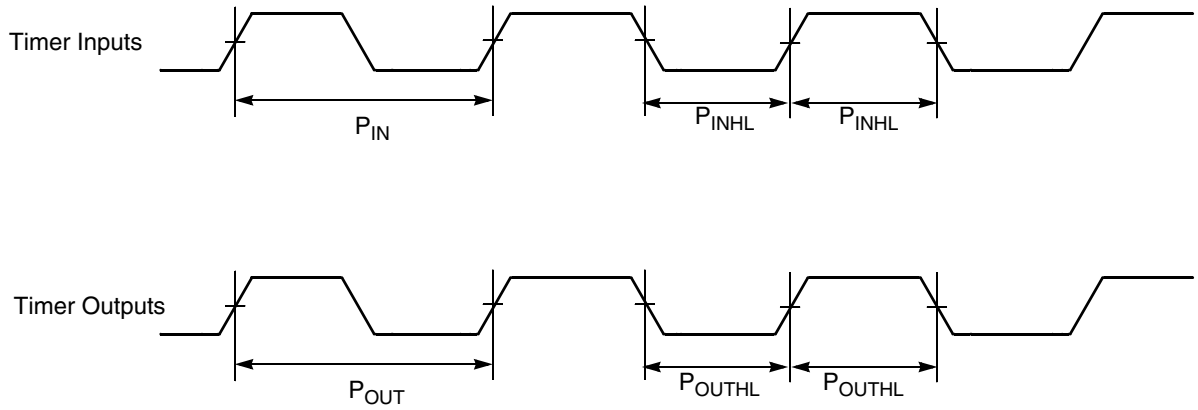


Figure 30. Timer Timing

1 No guaranteed specification within 5% of V_{DDA} or V_{SSA}
2 LSB = 0.806 mV

7.27 5-Bit Digital-to-Analog Converter (DAC) Parameters

Table 43. 5-Bit DAC Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Reference Inputs	Vin	V_{DDA}	—	V_{DDA}	mV
Setup Delay	t_{PRGST}	TBD	TBD	TBD	ns
Step size	V_{STEP}	3Vin/128	Vin/32	5Vin/128	V
Output Range	V_{DACOUT}	Vin/32	—	Vin	ns

7.28 HSCMP Specifications

Table 44. HSCMP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Analog input voltage	V_{AIN}	V_{SSA} – 0.01	—	V_{DDA} + 0.01	V
Analog input offset voltage[1]	V_{AIO}	—	—	40	mV
Analog comparator hysteresis[2]	V_H	—	1 to 16	—	mV
Propagation Delay, high speed mode (EN=1, PMODE=1),	t_{DHSN}[3]	—	70	140	ns
Propagation Delay, Low Speed Mode (EN=1, PMODE=0),	t_{AINIT}[4]	—	400	600	ns

1 Offset when the degree of hysteresis is set to its minimum value.
2 The range of hysteresis is based on simulation only. This range varies from part to part.
3 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.
4 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.

7.29 Optimize Power Consumption

See Section 7.7, "Supply Current Characteristics," for a list of I_{DD} requirements for the MC56F825x/MC56F824x. This section provides additional details for optimizing power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static] component
+B: internal [state-dependent] component
+C: internal [dynamic] component
+D: external [dynamic] component
+E: external [static] component

A, the internal [static] component, consists of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 4}$$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case. Refer to Equation 5.

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 5}$$

where:

T_T = Thermocouple temperature on top of package (^oC)

Ψ_{JT} = Thermal characterization parameter ($^oC/W$)

P_D = Power dissipation in package (W)

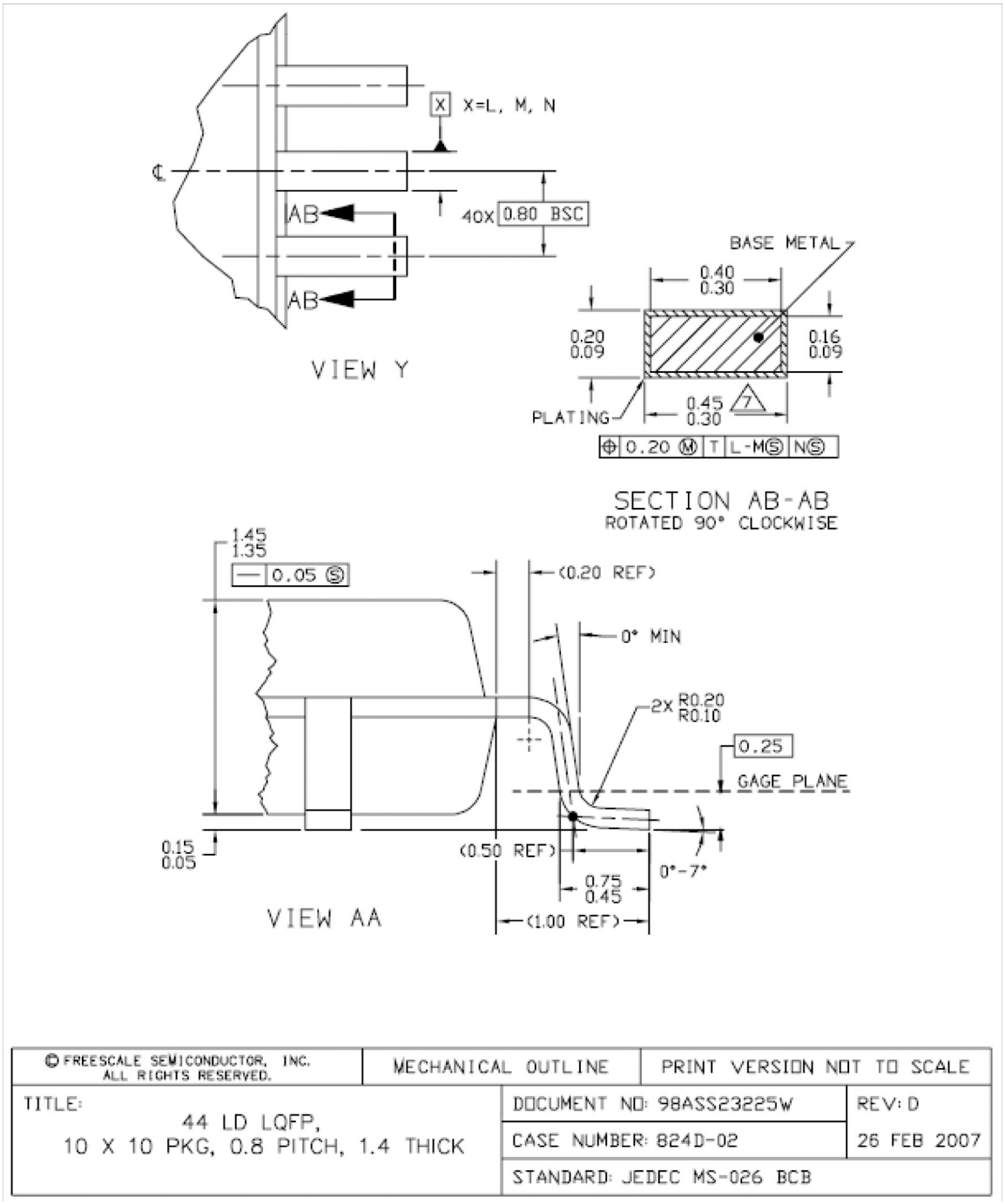
The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

8.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.



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	CASE NUMBER: 824D-02	26 FEB 2007
	STANDARD: JEDEC MS-026 BCB	

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS L, M AND N TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE T.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE DIMENSION TO EXCEED 0.53. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

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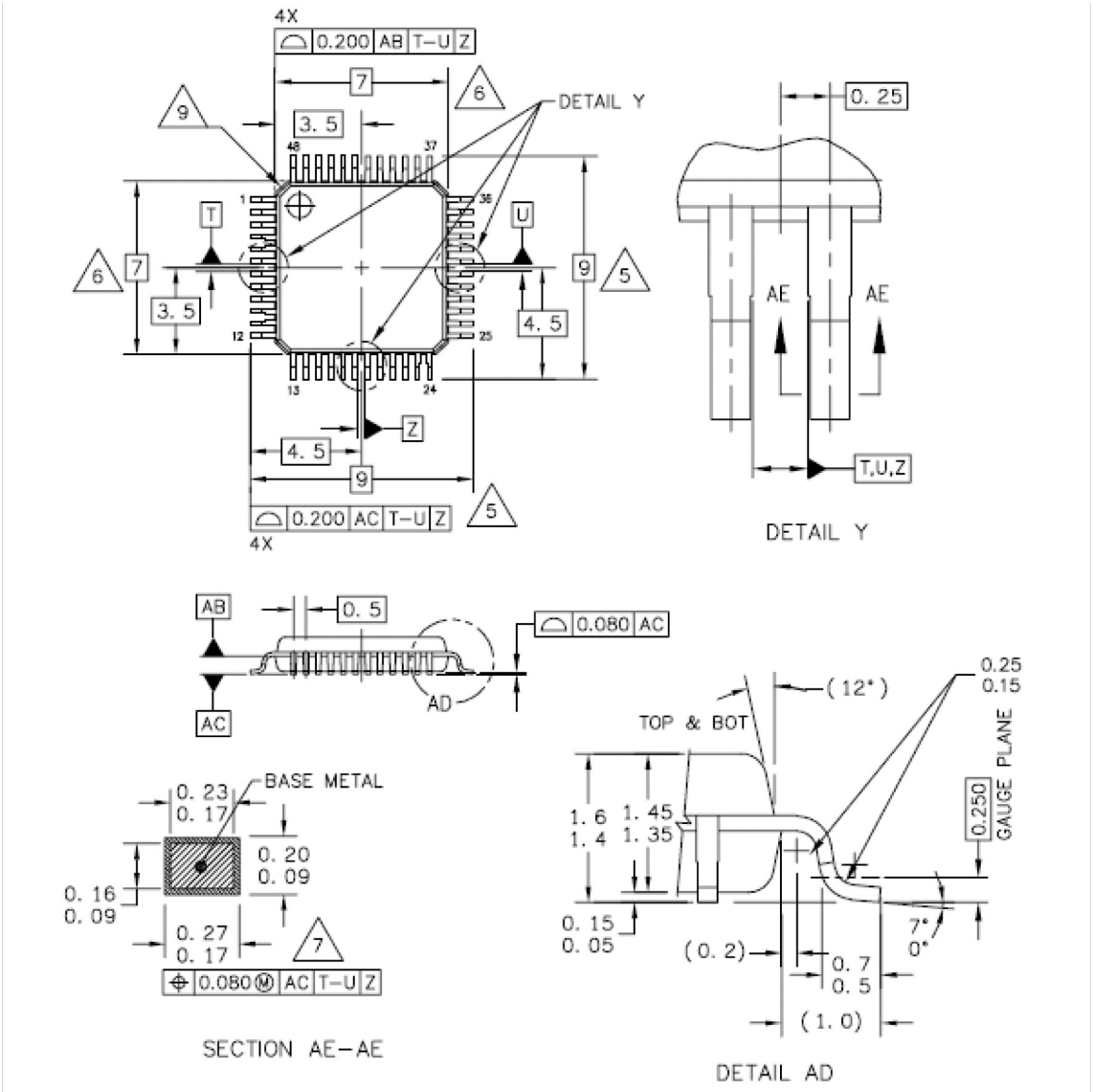
	CASE NUMBER: 824D-02	26 FEB 2007
	STANDARD: JEDEC MS-026 BCB	

Figure 32. 56F8245 and 56F8255 44-Pin LQFP Mechanical Information

10.2 48-pin LQFP



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	CASE NUMBER: 932-03	14 APR 2005
	STANDARD: JEDEC MS-026-BBC	

11 Revision History

Table 47 summarizes changes to the document since the release of the previous version.

Table 47. Revision History

Revision	Date	Description
Rev. 3	2011-04-22	Table 46 on page 75: Added “M” orderable part numbers Table 24 on page 55: Updated data for run, wait, and stop modes, and added data for standby and powerdown modes Table 23 on page 54: Added minimum and maximum values for Internal Pull-Up Resistance Renumbered sections: Section 9 (was 8.3), Section 10 (was 9), Section 11 (was 10)