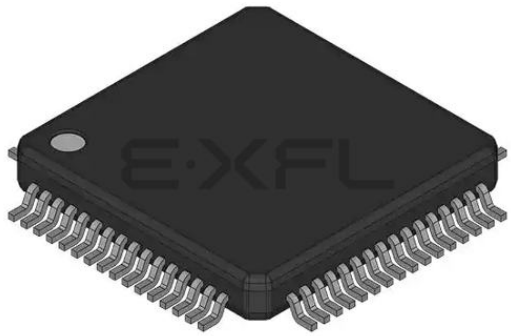

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8247vlh

2.4 Product Documentation

The documents listed in Table 2 are required for a complete description and proper design with the MC56F825x/MC56F824x. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at http://www.freescale.com.

Table 2. MC56F825x/MC56F824x Device Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F825x Reference Manual	Detailed description of peripherals of the MC56F825x/MC56F824x devices	MC56F825XRM
MC56F824x/5x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F800x family of devices	TBD
MC56F825x Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F825X
MC56F825x Errata	Detailed description of any chip issues that might be present	MC56F825XE

3 Signal/Connection Descriptions

3.1 Introduction

The input and output signals of the MC56F825x/MC56F824x are organized into functional groups, as detailed in Table 3.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins in 44 LQFP	Number of Pins in 48 LQFP	Number of Pins in 64 LQFP
Power inputs (V_{DD}, V_{DDA}, V_{CAP})	5	5	6
Ground (V_{SS}, V_{SSA})	4	4	4
Reset[1]	1	1	1
Enhanced Flex Pulse Width Modulator (eFlexPWM) ports[1]	6	6	9
Queued Serial Peripheral Interface (SPI) ports[1]	4	4	4
Queued Serial Communications Interface 0&1 (QSCI0 & QSCI1) ports[1]	6	6	9
Inter-Integrated Circuit Interface 0&1 (I^2C0 & I^2C0) ports[1]	4	4	6
Analog-to-Digital Converter (ADC) inputs[1]	8	10	16
High Speed Analog Comparator inputs/outputs[1]	11	12	15
12-bit Digital-to-Analog Converter (DAC_12B) output	1	1	1
Quad Timer Module (TMRA & TMRB) ports[1]	5	5	8
Freescale's Scalable Controller-Area-Network (MSCAN)[1, 2]	2	2	2
Inter-Module Cross Bar package inputs/outputs[1]	10	12	17
Clock[1]	3	4	4
JTAG/Enhanced On-Chip Emulation (EOnCE)[1]	4	4	4

Table 4. MC56F825x/MC56F824x Pins (continued)

Pin Number			Pin Name	Peripherals													
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MSCAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
19	21	28	GPIOB3/ *ANB3&VREFLB&CMPC_M0*	**GPIOB3**					*ANB3& VREFLB*		*CMPC_M0*					
		29	V_{DD}											**V_{DD}**		
20	22	30	V_{SS}											**V_{SS}**		
21	23	31	GPIOC6/*TA2/XB_IN3/ CMP_REF*	**GPIOC6**						*XB_IN3*	*CMP_REF*	*TA2*				
22	24	32	GPIOC7/$\overline{SS}$/*TXD0*	**GPIOC7**		*TXD0*	$\overline{SS}$									
23	25	33	GPIOC8/*MISO/RXD0*	**GPIOC8**		*RXD0*	*MISO*									
24	26	34	GPIOC9/*SCLK/XB_IN4*	**GPIOC9**			*SCLK*			*XB_IN4*						
25	27	35	GPIOC10/MOSI/XB_IN5/MISO	**GPIOC10**			MOSI/ MISO			XB_IN5						
	28	36	GPIOF0/*XB_IN6*	**GPIOF0**						*XB_IN6*						
26	29	37	GPIOC11/*CANTX/SCL1/TXD1*	**GPIOC11**	*SCL1*	*TXD1*		*CANTX*								
27	30	38	GPIOC12/*CANRX/SDA1/RXD1*	**GPIOC12**	*SDA1*	*RXD1*		*CANRX*								
		39	GPIOF2/*SCL1/XB_OUT2*	**GPIOF2**	*SCL1*					*XB_OUT2*						
		40	GPIOF3/*SDA1/XB_OUT3*	**GPIOF3**	*SDA1*					*XB_OUT3*						
		41	GPIOF4/*TXD1/XB_OUT4*	**GPIOF4**		*TXD1*				*XB_OUT4*						
		42	GPIOF5/*RXD1/XB_OUT5*	**GPIOF5**		*RXD1*				*XB_OUT5*						
28	31	43	V_{SS}											**V_{SS}**		
29	32	44	V_{DD}											**V_{DD}**		
30	33	45	GPIOE0/*PWM0B*	**GPIOE0**									*PWM0B*			
31	34	46	GPIOE1/*PWM0A*	**GPIOE1**									*PWM0A*			
32	35	47	GPIOE2/*PWM1B*	**GPIOE2**									*PWM1B*			
33	36	48	GPIOE3/*PWM1A*	**GPIOE3**									*PWM1A*			
34	37	49	GPIOC13/*TA3/XB_IN6*	**GPIOC13**						*XB_IN6*		TA3				
	38	50	GPIOF1/*CLKO/XB_IN7*	**GPIOF1**						*XB_IN7*						*CLKO*
35	39	51	GPIOE4/*PWM2B/XB_IN2*	**GPIOE4**						*XB_IN2*			*PWM2B*			
36	40	52	GPIOE5/*PWM2A/XB_IN3*	**GPIOE5**						*XB_IN3*			*PWM2A*			
		53	GPIOE6/*PWM3B/XB_IN4*	**GPIOE6**						*XB_IN4*			*PWM3B*			
		54	GPIOE7/*PWM3A/XB_IN5*	**GPIOE7**						*XB_IN5*			*PWM3A*			
37	41	55	GPIOC14/*SDA0/XB_OUT0*	**GPIOC14**	*SDA0*					*XB_OUT0*						
38	42	56	GPIOC15/*SCL0/XB_OUT1*	**GPIOC15**	*SCL0*					*XB_OUT1*						
39	43	57	V_{CAP}											**V_{CAP}**		
		58	GPIOF6/*TB2/PWM3X*	**GPIOF6**								*TB2*	*PWM3X*			
		59	GPIOF7/*TB3*	**GPIOF7**								*TB3*				
40	44	60	V_{DD}											**V_{DD}**		

3.3 MC56F825x/MC56F824x Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses and as *italic*, must be programmed via the GPIO module's peripheral enable registers (GPIO_x_PER) and the SIM module's GPIO peripheral select (GPSx) registers.

Table 5. MC56F825x/MC56F824x Signal and Package Information

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
V_{DD}			29	Supply	Supply	I/O Power — This pin supplies 3.3 V power to the chip I/O interface.
V_{DD}	29	32	44			
V_{DD}	40	44	60			
V_{SS}	20	22	30	Supply	Supply	I/O Ground — These pins provide ground for chip I/O interface.
V_{SS}	28	31	43			
V_{SS}	41	45	61			
V_{DDA}	13	15	22	Supply	Supply	Analog Power — This pin supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	14	16	23	Supply	Supply	Analog Ground — This pin supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	17	19	26	Supply	Supply	V_{CAP} — Connect a bypass capacitor of 2.2 µF or greater between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation. See Section 8.2, "Electrical Design Considerations," on page 73.
V_{CAP}	39	43	57			
TDI *(GPIOD0)*	44	48	64	Input Input/ Output	Input, internal pullup enabled	Test Data Input — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDI.
TDO *(GPIOD1)*	42	46	62	Output Input/ Output	Output	Test Data Output — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
TCK *(GPIOD2)*	1	1	1	Input Input/ Output	Input, internal pullup enabled	Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TCK

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC2	5	5	5	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TXD0)				Output		TXD0 — The SCI0 transmit data output or transmit/receive in single wire operation.
(TB0)				Input/ Output		TB0 — Quad timer module B channel 0 input/output.
(XB_IN2)				Input		XB_IN2 — Crossbar module input 2
(CLKO)				Output		CLKO — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM. After reset, the default state is GPIOC2.
GPIOC3	6	6	7	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA0)				Input/ Output		TA0 — Quad timer module A channel 0 input/output.
(CMPA_O)				Output		CMPA_O— Analog comparator A output
(RXD0)				Input		RXD0 — The SCI0 receive data input. After reset, the default state is GPIOC3.
GPIOC4	7	7	8	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA1)				Input/ Output		TA1 — Quad timer module A channel 1input/output
(CMPB_O)				Output		CMPB_O — Analog comparator B output After reset, the default state is GPIOC4.
GPIOC5	12	13	18	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(DACO)				Analog Output		DACO — 12-bit Digital-to-Analog Controller output
(XB_IN7)				Input		XB_IN7 — Crossbar module input 7 After reset, the default state is GPIOC5.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC14 *(SDA0)* *(XB_OUT0)*	37	41	55	Input/ Output Input/ Open-drain Output Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. SDA0 — I^2C0 serial data line XB_OUT0 — Crossbar module output 0 After reset, the default state is GPIOC14.
GPIOC15 *(SCL0)* *(XB_OUT1)*	38	42	56	Input/ Output Input/ Open-drain Output Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. SCL0 — I^2C0 serial clock XB_OUT1 — Crossbar module output 1 After reset, the default state is GPIOC15.
GPIOE0 *PWM0B*	30	33	45	Input/ Output Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM0B — NanoEdge PWM submodule 0 output B After reset, the default state is GPIOE0.
GPIOE1 *(PWM0A)*	31	34	46	Input/ Output Output	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM0A — NanoEdge PWM submodule 0 output B After reset, the default state is GPIOE1.
GPIOE2 *(PWM1B)*	32	35	47	Input/ Output Output	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM1B — NanoEdge PWM submodule 1 output A After reset, the default state is GPIOE2.
GPIOE3 *(PWM1A)*	33	36	48	Input/ Output Output	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM1A — NanoEdge PWM submodule 1 output A After reset, the default state is GPIOE3.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOF6 *(TB2)* *(PWM3X)*			58	Input/ Output Input/ Output Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. TB2 — Quad timer module B channel 2 input/output. PWM3X — Enhanced PWM submodule 3 output X or input capture X After reset, the default state is GPIOF6.
GPIOF7 *(TB3)*			59	Input/ Output Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. TB3 — Quad timer module B channel 3 input/output. After reset, the default state is GPIOF7.
GPIOF8 *(RXD0)* *(TB1)*			6	Input/ Output Input Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. RXD0 — The SCI0 receive data input. TB1 — Quad timer module B channel 1 input/output. After reset, the default state is GPIOF8.

1 If CLKIN is selected as the device's external clock input, both the GPS_C0 bit in GPS1 and the EXT_SEL bit in the OCCS oscillator control register (OSCTL) must be set. In this case, it is also recommended to power down the crystal oscillator.

4 Memory Maps

4.1 Introduction

The MC56F825x/MC56F824x device is based on the 56800E core. It uses a dual Harvard-style architecture with two independent memory spaces for data and program. On-chip RAM is shared by both data and program spaces; flash memory is used only in program space.

This section provides memory maps for:

- Program address space, including the interrupt vector table
- Data address space, including the EOnCE memory and peripheral memory maps

On-chip memory sizes for the device are summarized in Table 6. Flash memories' restrictions are identified in the "Use Restrictions" column of Table 6.

Table 6. Chip Memory Configurations

On-Chip Memory	56F8245 56F8246	56F8247	56F8255 56F8256 56F8357	Use Restrictions
Program Flash (PFLASH)	24K x 16 or 48 KB	24K x 16 or 48 KB	32K x 16 or 64 KB	Erase/program via flash interface unit and word writes to CDBW
Unified RAM (RAM)	3K x 16 or 6 KB	4K x 16 or 8 KB	4K x 16 or 8 KB	Usable by the program and data memory spaces

4.2 Program Map

The MC56F825x/MC56F824x series provide up to 64 KB on-chip flash memory. It primarily accesses through the program memory buses (PAB; PDB). PAB is used to select program memory addresses; instruction fetches are performed over PDB. Data can be read from and written to the program memory space through the primary data memory buses: CDBW for data write and CDBR for data read. Access time for accessing the program memory space over the data memory buses is longer than for accessing data memory space. The special MOVE instructions are provided to support these accesses. The benefit is that non-time-critical constants or tables can be stored and accessed in program memory.

The program memory map appears in Table 7, Table 8, and Table 9, depending on the device.

Table 7. Program Memory Map[1] for 56F8255/56/57 at Reset

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 8FFF P: 0x00 8000	On-chip RAM[2]: 8 KB
P: 0x00 7FFF P: 0x00 0000	• Internal program flash: 64 KB • Interrupt vector table locates from 0x00 0000 to 0x00 0085 • COP reset address = 0x00 0002 • Boot location = 0x00 0000

1 All addresses are 16-bit word addresses.

2 This RAM is shared with data space starting at address X: 0x00 0000. See Figure 6.

Table 8. Program Memory Map[1] for 56F82447 at Reset

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 8FFF P: 0x00 8000	On-chip RAM[2]: 8 KB
P: 0x00 7FFF P: 0x00 2000	• Internal program flash: 48 KB • Interrupt vector table locates from 0x00 2000 to 0x00 2085 • COP reset address = 0x00 2002 • Boot location = 0x00 2000
P: 0x00 2000 P: 0x00 0000	RESERVED

- Software reset (SWR)

Each of these sources has an associated bit in the reset status register (RSTAT) in the system integration module (SIM).

The external pin reset function is shared with a GPIO port A7 on the $\overline{\text{RESET}}$/GPIOA7 pin. The reset function is enabled following any reset of the device. Bit 7 of the GPIOA_PER register must be cleared to use this pin as a GPIO port pin. When the pin is enabled as the $\overline{\text{RESET}}$ pin, an internal pullup device is automatically enabled.

5.4 On-chip Clock Synthesis

The on-chip clock synthesis (OCCS) module allows designers using an internal relaxation oscillator, an external crystal, or an external clock to run 56F8000 family devices at user-selectable frequencies up to 60 MHz.

The features of OCCS module include:

- Ability to power down the internal relaxation oscillator or crystal oscillator
- Ability to put the internal relaxation oscillator into standby mode
- Ability to power down the PLL
- Provides a 2x system clock that operates at two times the system clock to the timer and SCI modules
- Safety shutdown feature if the PLL reference clock is lost
- Ability to be driven from an external clock source

The clock generation module provides the programming interface for the PLL, internal relaxation oscillator, and crystal oscillator. It also provides a postscaler to divide clock frequency down by 1, 2, 4, 8, 16, 32, 64, 128, or 256 before feeding it to the SIM. The SIM is responsible for further dividing these frequencies by 2, which ensures a 50% duty cycle in the system clock output. For details, refer to the OCCS section of the device's reference manual.

5.4.1 Internal Clock Source

When an external frequency source or crystal is not used, an internal relaxation oscillator can supply the reference frequency. It is optimized for accuracy and programmability while providing several power-saving configurations that accommodate different operating conditions. The internal relaxation oscillator has little temperature and voltage variability. To optimize power, the internal relaxation oscillator supports a run state (8 MHz), standby state (400 kHz), and a power-down state.

During a boot or reset sequence, the relaxation oscillator is enabled by default (the PRECS bit in the PLLCR word is set to 0). Application code can then also switch to the external clock source and power down the internal oscillator, if desired. If a changeover between internal and external clock sources is required at power-on, ensure that the clock source is not switched until the desired external clock source is enabled and stable.

To compensate for variances in the device manufacturing process, the accuracy of the relaxation oscillator can be incrementally adjusted to within + 0.078% of 8 MHz by trimming an internal capacitor. Bits 0–9 of the oscillator control (OSCTL) register allow you to set an additional offset (trim) to this preset value to increase or decrease capacitance. Each unit added or subtracted changes the output frequency by about 0.078% of 8 MHz, allowing incremental adjustment until the desired frequency accuracy is achieved.

The center frequency of the internal oscillator is calibrated at the factory to 8 MHz, and the TRIM value is stored in the flash information block and loaded to the HFM IFR option register 0 at reset. When using the relaxation oscillator, the boot code should read the HFM IFR option register 0 and set this value as OSCTL TRIM. For further information, refer to the device's reference manual.

5.4.2 Crystal Oscillator/Ceramic Resonator

The internal crystal oscillator circuit is designed to interface with a parallel-resonant crystal resonator in the frequency range, specified for the external crystal, of 4 MHz to 16 MHz. A ceramic resonator can be substituted for the 4 MHz to 16 MHz range. When used to supply a source to the internal PLL, the recommended crystal/resonator is in the 8 MHz to 16 MHz range to optimize PLL performance. Oscillator circuits appear in Figure 9 and Figure 10. Follow the crystal supplier's recommendations

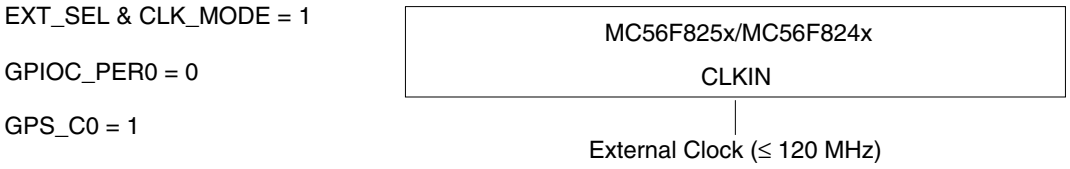


Figure 11. Connecting an External Clock Signal Using GPIO

5.5 Interrupt Controller

The MC56F825x/MC56F824x interrupt controller (INTC) module arbitrates the various interrupt requests (IRQs). When an interrupt of sufficient priority exists, the INTC signals to the 56800E core and provides the address to which to jump to service the interrupt.

The interrupt controller contains registers that allow each of the 66 interrupt sources to be set to one of three priority levels (excluding certain interrupt sources that have fixed priority) or to be disabled. Next, all interrupt requests of a given level are priority encoded to determine the lowest numeric value of the active interrupt requests for that level. Within a given priority level, the lowest vector number is the highest priority, and the highest vector number is the lowest priority.

Any two interrupt sources can be assigned to faster interrupts. Fast interrupts are described in the *DSP56800E Reference Manual*. The interrupt controller recognizes fast interrupts before the core does.

A fast interrupt is defined by:

1. Setting the priority of the interrupt as level 2 with the appropriate field in the Interrupt Priority Register (IPR) registers
2. Setting the Fast Interrupt Match (FIM*n*) register to the appropriate vector number
3. Setting the Fast Interrupt Vector Address Low (FIVAL*n)* and Fast Interrupt Vector Address High (FIVAH*n)* registers with the address of the code for the fast interrupt

When an interrupt occurs, its vector number is compared with the FIM0 and FIM1 register values. If a match occurs, and it is a level 2 interrupt, the INTC handles it as a Fast Interrupt. The INTC takes the vector address from the appropriate FIVAL*n* and FIVAH*n* registers, instead of generating an address that is an offset from the VBA.

The core then fetches the instruction from the indicated vector address instead of jumping to the vector table. If the instruction is not a JSR, the core starts its fast interrupt handling. Refer to section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for details.

Table 48 on page 85 provides the MC56F825x/MC56F824x's interrupt table contents and interrupt priority structure.

5.6 System Integration Module (SIM)

The SIM module consists of the glue logic that ties together the system-on-a-chip. It controls distribution of resets and clocks and provides a number of control features, including pin muxing control, inter-module connection control (such as connecting comparator output to eFlexPWM fault input), individual peripheral enabling/disabling, clock rate control for quad timers and SCIs, enabling peripheral operation in stop mode, and port configuration overwrite protection. For more information, refer to the device's reference manual.

The SIM is responsible for the following functions:

- Chip reset sequencing
- Core and peripheral clock control and distribution
- Stop/wait mode control
- System status control
- Registers containing the JTAG ID of the chip
- Controls for programmable peripheral and GPIO connections

7.3 ESD Protection and Latch-up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing conforms with AEC-Q100 Stress Test Qualification. During device qualification, ESD stresses are performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing conforms with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification. Comprehensive DC parametric and functional testing is performed according to the applicable device specification at room temperature and then at hot temperature, unless specified otherwise in the device specification.

Table 18. MC56F825x/MC56F824x ESD/Latch-up Protection

Characteristic [1]	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	750	—	—	V
Latch-up current at T_A = 85 °C (I_{LAT})	± 100			mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions, unless otherwise noted

7.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the device design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

Table 19. 44LQFP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	70	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	48	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	57	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	42	°C/W
Junction to board		$R_{\theta JB}$	30	°C/W
Junction to case		$R_{\theta JC}$	13	°C/W
Junction to package top	Natural convection	Ψ_{JT}	2	°C/W

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

See Section 8.1, "Thermal Design Considerations," for more detail on thermal design considerations.

7.5 Recommended Operating Conditions

This section contains information about recommended operating conditions.

Table 22. Recommended Operating Conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD}, V_{DDA}		3	3.3	3.6	V
ADC Reference Voltage High	V_{REFHx}		3.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		 0.001 0		 60 60	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2.0		5.5	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	-0.3		0.8	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
DAC Output Load Resistance	R_{LD}	Pin Group 5	3K			Ω
DAC Output Load Capacitance	C_{LD}	Pin Group 5			400	pf
Output Source Current High at V_{OH} min.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -4 -8	mA
Output Source Current Low (at V_{OL} max.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 4 8	mA
Ambient Operating Temperature (Extended Industrial)	T_A		-40		105	°C
Flash Endurance (Program Erase Cycles)	N_F	T_A = -40°C to 125°C	10,000		—	cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15		—	years
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	years

7.8 Power-On Reset, Low Voltage Detection Specification

Table 25. Power-On Reset and Low-Voltage Detection Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Voltage Interrupt for 3.3 V supply[1]	V_{LVI27}	2.6	2.7	2.8	V
Low-Voltage Interrupt for 2.5 V supply[2]	V_{LVI21}	—	2.18	—	V
Low-Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power-On Reset Threshold[3]	POR	2.6	2.7	2.8	V
Brown-Out Reset Threshold[4]	BOR	—	1.8	1.9	V

1 When V_{DD} drops below LVI27, an interrupt is generated.
2 When V_{DD} drops below LVI21, an interrupt is generated.
3 While power is ramping up, this signal remains active for as long as the internal 2.5 V is below 2.18 V or the 3.3 V V_{DD} voltage is below 2.7 V, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp-up until 2.5 V is reached, at which time it self-regulates.
4 Brown-Out Reset occurs whenever the internally regulated 2.5 V digital supply drops below 1.8 V.

7.9 Voltage Regulator Specifications

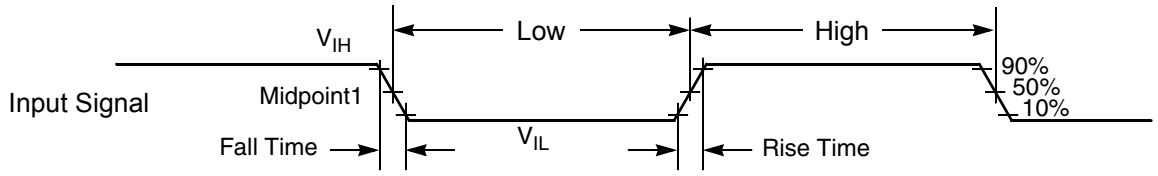
The MC56F825x/MC56F824x has two on-chip regulators. One supplies the PLL, crystal oscillator, NanoEdge placement PWM, and relaxation oscillator. It has no external pins and therefore has no external characteristics that must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.5 V to the MC56F825x/MC56F824x's core logic. For proper operation, this regulator requires an external capacitor of 2.2 µF or greater. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator appear in Table 26.

Table 26. Regulator Parameters

Characteristic	Symbol	Min	Typical	Max	Unit
Short Circuit Current	I_{SS}	—	900	1300	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	minutes

7.10 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 23. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 15.



The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 15. Input Signal Measurement References

Table 29. External Clock Operation Timing Requirements[1] (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
External clock input rise time[4]	t_{rise}	—	—	3	ns
External clock input fall time[5]	t_{fall}	—	—	3	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.85V_{DD}$	—	—	V
Input high voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

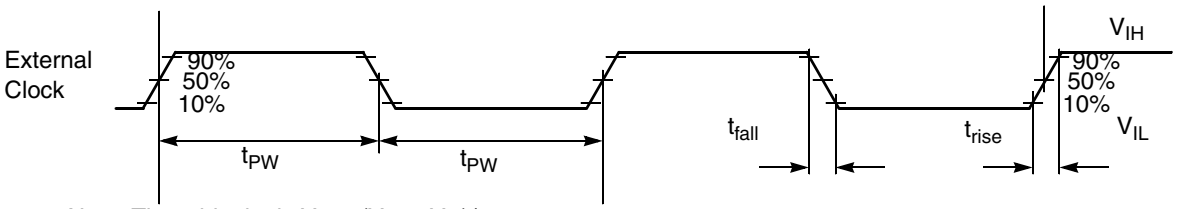
1 Parameters listed are guaranteed by design.

2 See Figure 17 for details on using the recommended connection of an external clock driver.

3 The chip may not function if the high or low pulse width is smaller than 6.25 ns.

4 External clock input rise time is measured from 10% to 90%.

5 External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 17. External Clock Timing

7.14 Phase Locked Loop Timing

Table 30. Phase Locked Loop Timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	4	8	8	MHz
PLL output frequency[2]	f_{op}	120	—	240	MHz
PLL lock time[3] [4]	t_{plls}	—	40	100	µs
Accumulated jitter using an 8 MHz external crystal as the PLL source[5]	J_A	—	—	TBD	%
Cycle-to-cycle jitter	$t_{jitterpll}$	—	350	—	ps

1 An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.

2 The core system clock operates at 1/6 of the PLL output frequency.

3 This is the time required after the PLL is enabled to ensure reliable operation.

4 From powerdown to powerup state at 60 MHz system clock state.

5 This is measured on the CLKO signal (programmed as system clock) over 264 system clocks at 60 MHz system clock frequency and using an 8 MHz oscillator frequency.

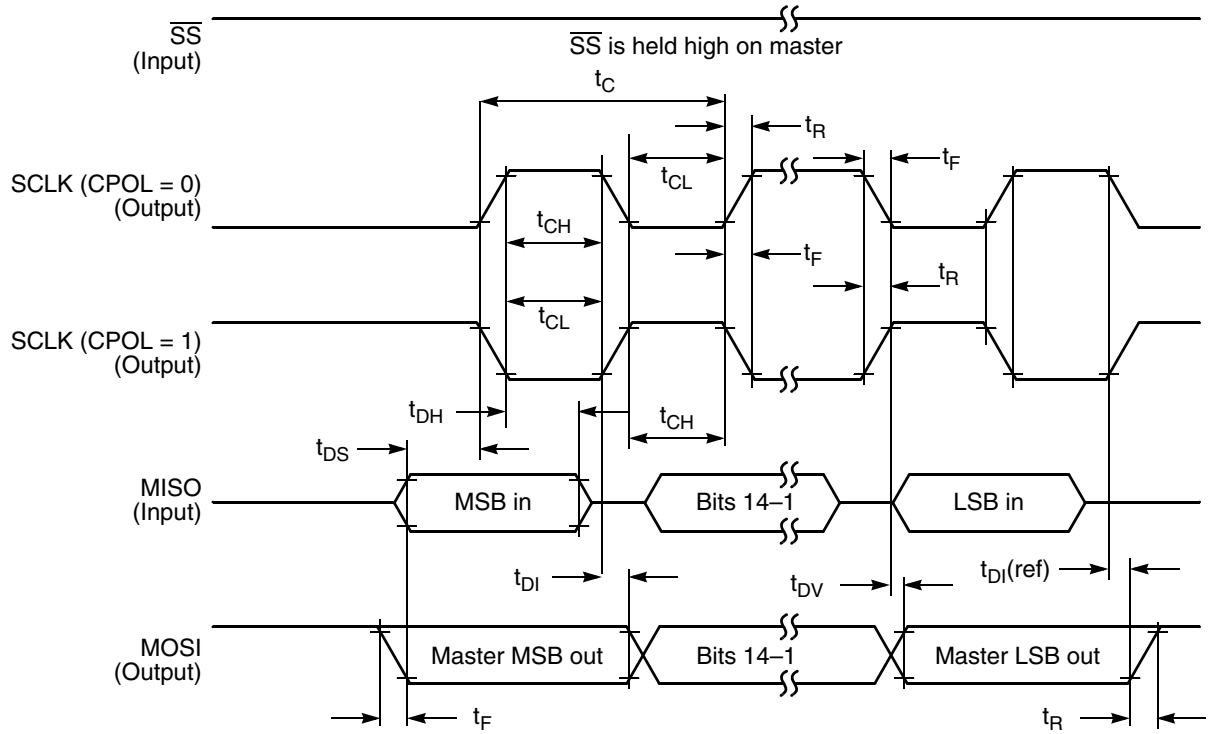


Figure 20. SPI Master Timing (CPHA = 0)

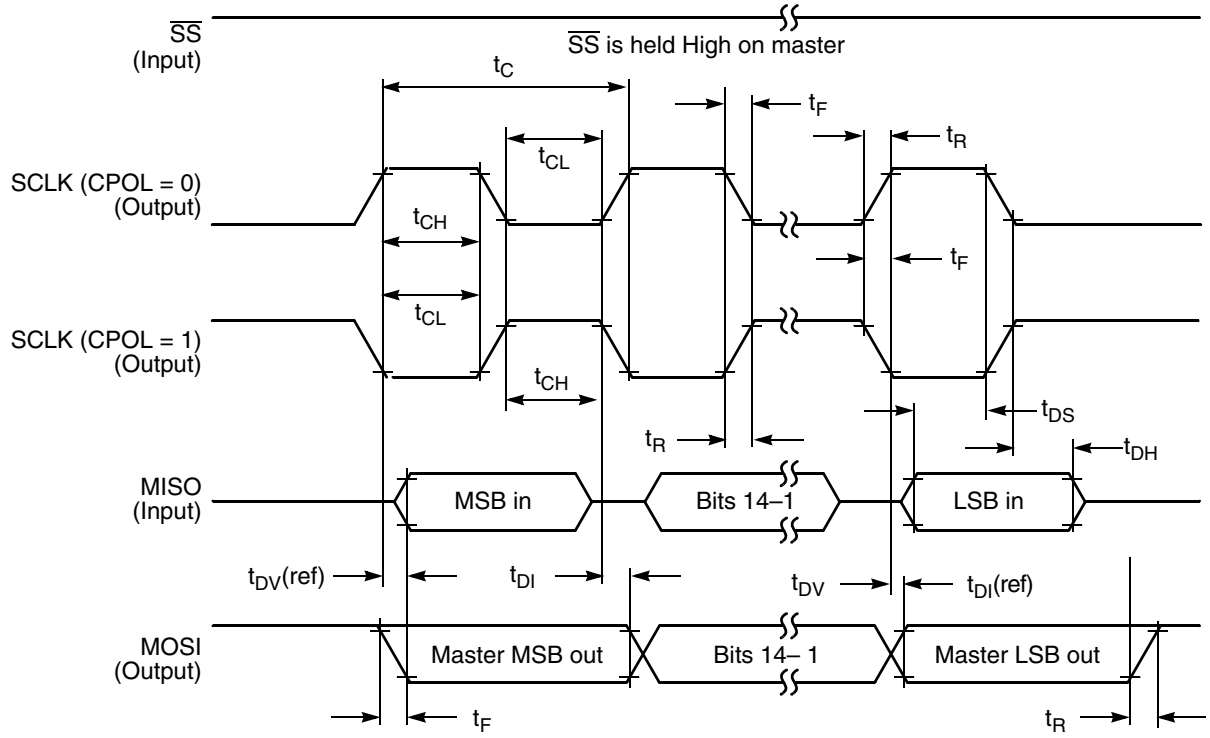


Figure 21. SPI Master Timing (CPHA = 1)

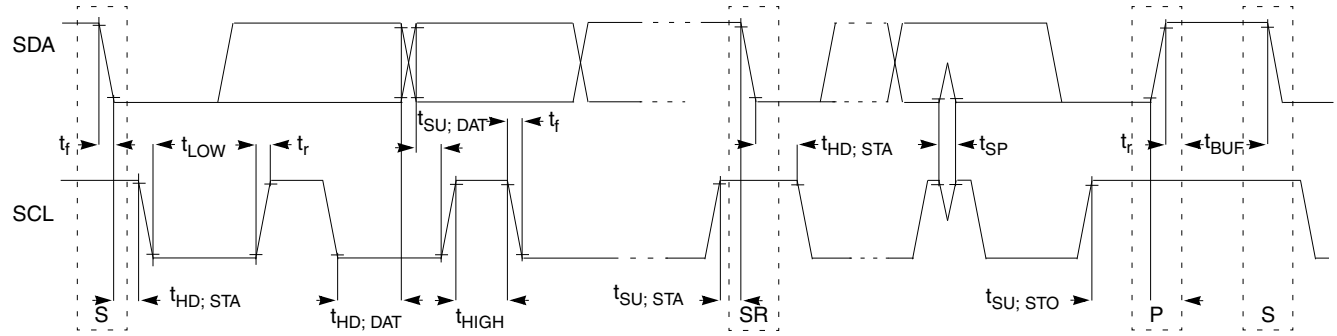


Figure 27. Timing Definition for Standard Mode Devices on the I^2C Bus

7.22 JTAG Timing

Table 38. JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation[1]	f_{OP}	DC	SYS_CLK/8	MHz	Figure 28
TCK clock pulse width	t_{PW}	50	—	ns	Figure 28
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 29
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 29
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 29
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 29

[1] TCK frequency of operation must be less than 1/8 the processor rate.

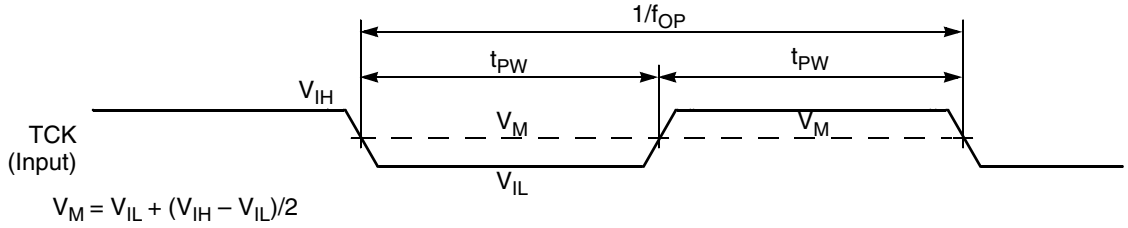


Figure 28. Test Clock Input Timing Diagram

7.24 COP Specifications

Table 40. COP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Oscillator output frequency	LPFosc	500	1000	1500	Hz
Oscillator current consumption in partial power down mode	IDD		TBD		nA

7.25 Analog-to-Digital Converter (ADC) Parameters

Table 41. ADC Parameters[1]

Parameter	Symbol	Min	Typ	Max	Unit
DC Specifications					
Resolution	R_{ES}	12	—	12	Bits
ADC internal clock	f_{ADIC}	0.1	—	15	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC and VREF power-up time[2](from power down mode)	t_{ADPU}	—	13	—	t_{AIC} cycles[3]
VREF power-up time (from low power mode)	t_{REFPU}	—	6	—	t_{AIC} cycles[3]
ADC RUN current (Speed Control setting) at 100 kHz ADC clock (Standby Mode) at ADC clock ≤ 5 MHz (00) at 5 MHz < ADC clock ≤ 12 MHz (01) at 12 MHz < ADC clock ≤ 15 MHz (10)	I_{ADRUN}	 — — — —	 0.6 10 17 27	 — — — —	mA
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Accuracy (DC or absolute) (gain of 1x, 2x, 4x and f_{ADC} ≤ 10 MHz) (all data in single-ended mode)[4]					
Integral non-linearity[5] (Full input signal range)	INL	—	+/- 3	+/- 6	LSB[6]
Differential non-linearity[5]	DNL	—	+/- 0.6	+/- 1	LSB[5]
Monotonicity	GUARANTEED				
Offset Voltage Internal Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Offset Voltage External Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Gain Error (transfer gain)	E_{GAIN}	—	0.995 to 1.005	1.01 to 0.99	—
ADC Inputs[7] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0.001	—	µA
Input injection current[8], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See Figure 31	—	pF

Use the following list of considerations to assure correct operation of the MC56F825x/MC56F824x:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the MC56F825x/MC56F824x and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} is recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with V_{DDA} and V_{SSA} traces.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ to 10 kΩ; the capacitor value should be in the range of 0.22 µF to 4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if a JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input state with internal pullup enabled. The typical value of internal pullup is around 110 kΩ. These internal pullups can be disabled by software.
- To eliminate PCB trace impedance effect, each ADC input should have an RC filter of no less than 33 pF 10 Ω.
- External clamp diodes on analog input pins are recommended.

9 Ordering Information

Table 46 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order devices.

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS L, M AND N TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE T.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE DIMENSION TO EXCEED 0.53. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

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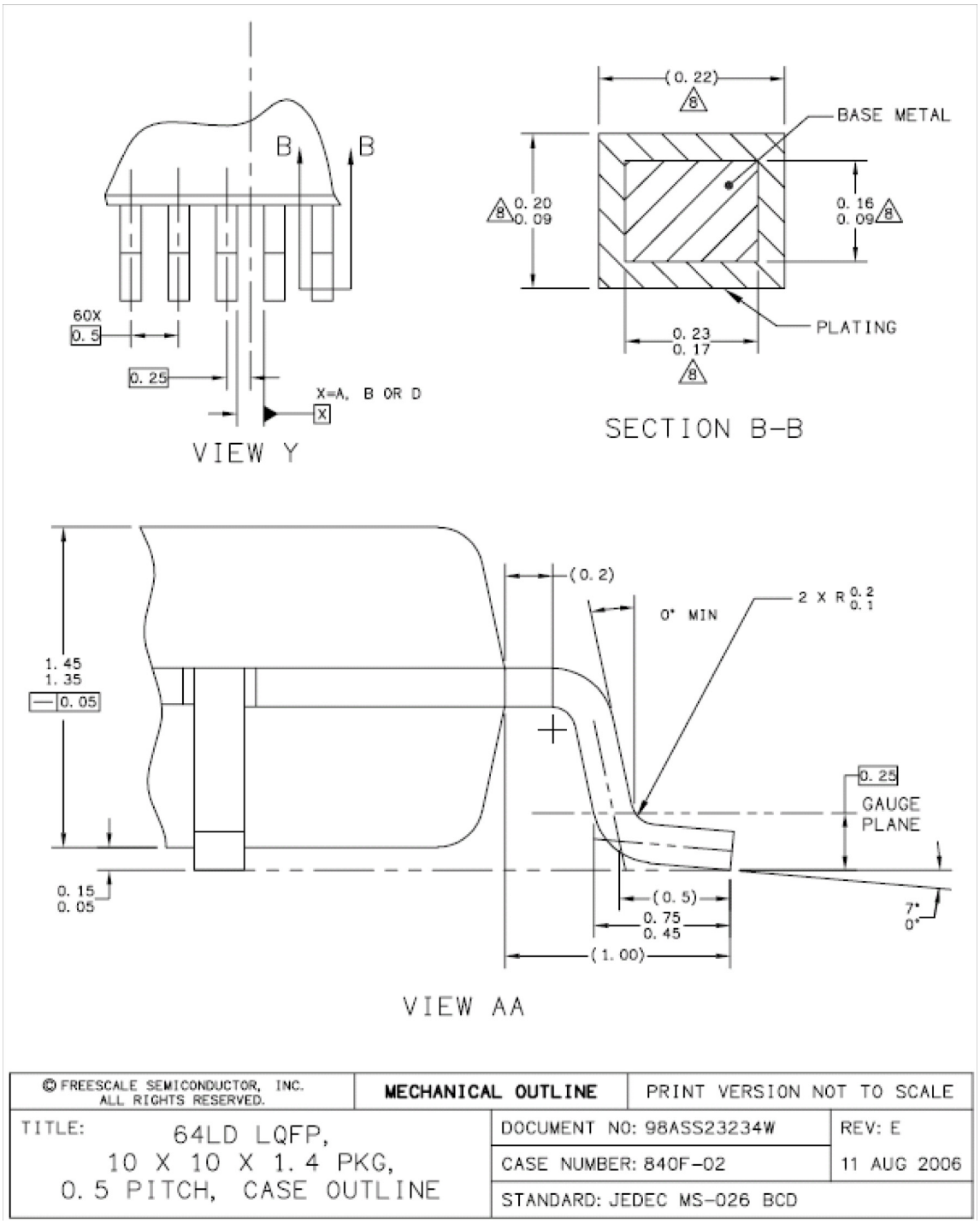
TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23225W	REV: D
	CASE NUMBER: 824D-02	26 FEB 2007
	STANDARD: JEDEC MS-026 BCB	

Figure 32. 56F8245 and 56F8255 44-Pin LQFP Mechanical Information



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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: E
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	

11 Revision History

Table 47 summarizes changes to the document since the release of the previous version.

Table 47. Revision History

Revision	Date	Description
Rev. 3	2011-04-22	Table 46 on page 75: Added “M” orderable part numbers Table 24 on page 55: Updated data for run, wait, and stop modes, and added data for standby and powerdown modes Table 23 on page 54: Added minimum and maximum values for Internal Pull-Up Resistance Renumbered sections: Section 9 (was 8.3), Section 10 (was 9), Section 11 (was 10)