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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8255mld

3.2 Pin Assignment

Figure 3 shows the pin assignments of the 56F8245 and 56F8255's 44-pin low-profile quad flat pack (44LQFP). Figure 4 shows the pin assignments of the 56F8246 and 56F8256's 48-pin low-profile quad flat pack (48LQFP). Figure 5 shows the pin assignments of the 56F8247 and 56F8257's 64-pin low-profile quad flat pack (64LQFP).

NOTE

The CANRX and CANTX signals of the MSCAN module are not available on the MC56F824x devices.

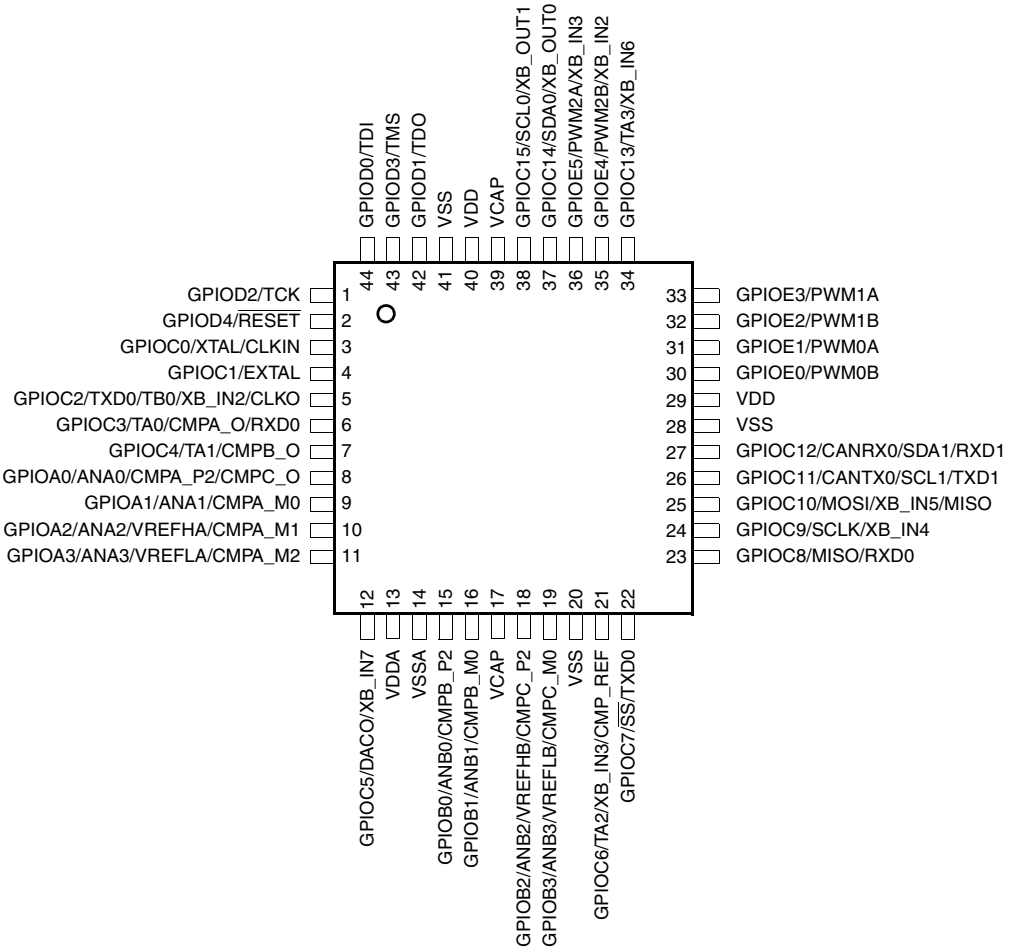


Figure 3. Top View: 56F8245 and 56F8255 44-Pin LQFP Package

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
TMS *(GPIOD3)*	43	47	63	input Input/ Output	Input, internal pullup enabled	Test Mode Select Input — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TMS **Note**: Always tie the TMS pin to VDD through a 2.2K resistor if need to keep on-board debug capability. Otherwise directly tie to VDD
$\overline{\text{RESET}}$ *(GPIOD4)*	2	2	2	Input Input/ Open-drain Output	Input, internal pullup enabled	Reset — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. Port D GPIO — This GPIO pin can be individually programmed as an input or open-drain output pin.If $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can be reset only via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOA0 *(ANA0& CMPA_P2)* *(CMPC_O)*	8	9	13	Input/ Output Input Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA0 and CMPA_P2 — Analog input to channel 0 of ADCA and positive input 2 of analog comparator A. CMPC_O— Analog comparator C output When used as an analog input, the signal goes to the ANA0 and CMPA_P2. After reset, the default state is GPIOA0.
GPIOA1 *(ANA1& CMPA_M0)*	9	10	14	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA1 and CMPA_M0 — Analog input to channel 1of ADCA and negative input 0 of analog comparator A. When used as an analog input, the signal goes to the ANA1 and CMPA_M0. After reset, the default state is GPIOA1.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOB0 *(ANB0& CMPB_P2)*	15	17	24	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB0 and CMPB_P2 — Analog input to channel 0 of ADCB and positive input 2 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_P2. After reset, the default state is GPIOB0.
GPIOB1 *(ANB1& CMPB_M0)*	16	18	25	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB1 and CMPB_M0— Analog input to channel 1 of ADCB and negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_M0. After reset, the default state is GPIOB1.
GPIOB2 *(ANB2& VREFHB& CMPC_P2)*	18	20	27	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB2 and VREFHB and CMPC_P2 — Analog input to channel 2 of ADCB and analog references high of ADCB and positive input 2 of analog comparator C. When used as an analog input, the signal goes to ANB2 and VREFHB and CMPC_P2. ADC control register configures this input as ANB2 or VREFHB. After reset, the default state is GPIOB2.
GPIOB3 *(ANB3& VREFLB& CMPC_M0)*	19	21	28	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB3 and VREFLB and CMPC_M0 — Analog input to channel 3 of ADCB and analog references low of ADCB and negative input 0 of analog comparator C. When used as an analog input, the signal goes to ANB3 and VREFLB and MPC_M0. ADC control register configures this input as ANB3 or VREFLB. After reset, the default state is GPIOB3.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC6	21	23	31	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA2)				Input/ Output		TA2 — Quad timer module A channel 2 input/output
(XB_IN3)				Input		XB_IN3 — Crossbar module input 3
(CMP_REF)				Analog Input		CMP_REF— Positive input 3 of analog comparator A and B and C
						After reset, the default state is GPIOC6
GPIOC7	22	24	32	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
($\overline{SS}$)				Input/ Output		$\overline{SS}$ — $\overline{SS}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received.
(TXD0)				Output		TXD0 — SCI0 transmit data output or transmit/receive in single wire operation
						After reset, the default state is GPIOC7.
GPIOC8	23	25	33	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(MISO)				Input/ Output		MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(RXD0)				Input		RXD0 — SCI0 receive data input
						After reset, the default state is GPIOC8.
GPIOC9	24	26	34	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(SCLK)				Input/ Output		SCLK — The SPI serial clock. In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
(XB_IN4)				Input		XB_IN4 — Crossbar module input 4
						After reset, the default state is GPIOC9.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC10	25	27	35	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(MOSI)				Input/ Output		MOSI — Master out/slave in. In master mode, this pin serves as the data output. In slave mode, this pin serves as the data input.
(XB_IN5)				Input		XB_IN5 — Crossbar module input 5
(MISO)				Input/ Output		MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. After reset, the default state is GPIOC10.
GPIOC11	26	29	37	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CANTX)				Open-drain Output		CANTX — CAN transmit data output (not available on 56F8245/46/47)
(SCL1)				Input/ Open-drain Output		SCL1 — I^2C1 serial clock
(TXD1)				Output		TXD1 — SCI1 transmit data output or transmit/receive in single wire operation After reset, the default state is GPIOC11.
GPIOC12	27	30	38	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CANRX)				Input		CANRX — CAN receive data input (not available on 56F8245/46/47)
(SDA1)				Input/ Open-drain Output		SDA1 — I^2C1 serial data line
(RXD1)				Input		RXD1 — SCI1 receive data input After reset, the default state is GPIOC12.
GPIOC13	34	37	49	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA3)				Input/ Output		TA3 — Quad timer module A channel 3input/output.
(XB_IN6)				Input		XB_IN6 — Crossbar module input 6 After reset, the default state is GPIOC13.

Table 11. 56F8245/56 Data Memory Map[1]

Begin/End Address	Memory Allocation
X:0xFF FFFF X:0xFF FF00	EOnCE 256 locations allocated
X:0xFF FEFF X:0x01 0000	RESERVED
X:0x00 FFFF X:0x00 F000	On-Chip Peripherals 4096 locations allocated
X:0x00 EFFF X:0x00 8C00	RESERVED
X:0x00 8BFF X:0x00 8000	On-Chip Data RAM Alias
X:0x00 7FFF X:0x00 0C00	RESERVED
X:0x00 0BFF X:0x00 0000	On-Chip Data RAM 6 KB[2]

1 All addresses are 16-bit word addresses.

2 This RAM is shared with program space starting at P: 0x00 8000. See Figure 8.

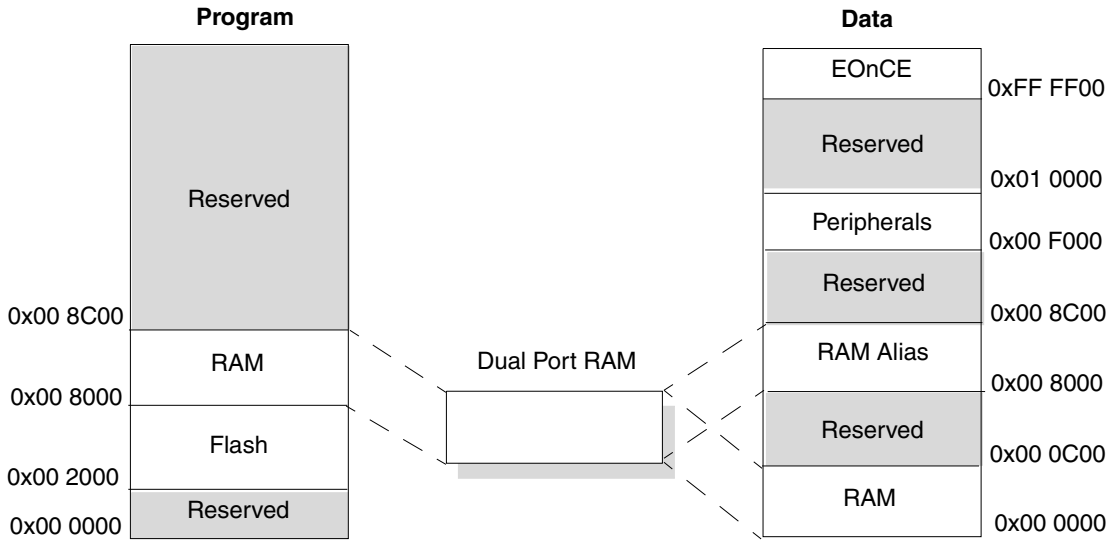


Figure 8. 56F8245/46 Dual Port RAM Map

4.4 Interrupt Vector Table and Reset Vector

The location of the vector table is determined by the vector base address register (VBA). The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower seven bits are determined based on the highest priority interrupt and are then appended to VBA before presenting the full VAB to the core. Refer to the device's reference manual for details.

The reset startup addresses of 56F824x and 56F825x are different.

- The 56F825x's startup address is located at 0x00 0000. The reset value of VBA is reset to a value of 0x0000 that corresponds to the address 0x00 0000.

when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable startup. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances. The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and startup stabilization time. When using low-frequency, low-power mode, the only external component is the crystal itself. In the other oscillator modes, load capacitors (C_x, C_y) and feedback resistor (R_F) are required. In addition, a series resistor (R_S) may be used in high-gain modes. Recommended component values appear in Table 27.

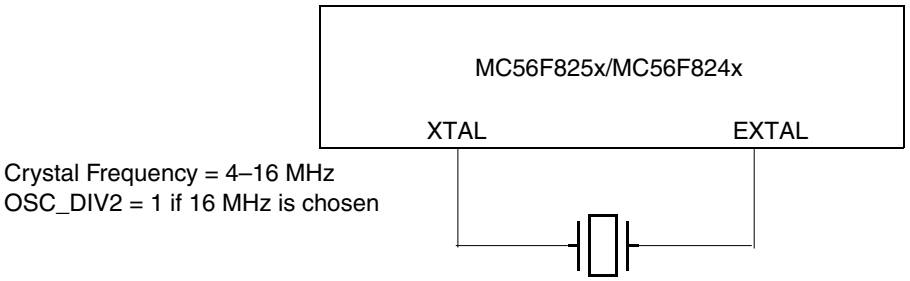


Figure 9. Typical Crystal Oscillator Circuit without Frequency Compensation Capacitor

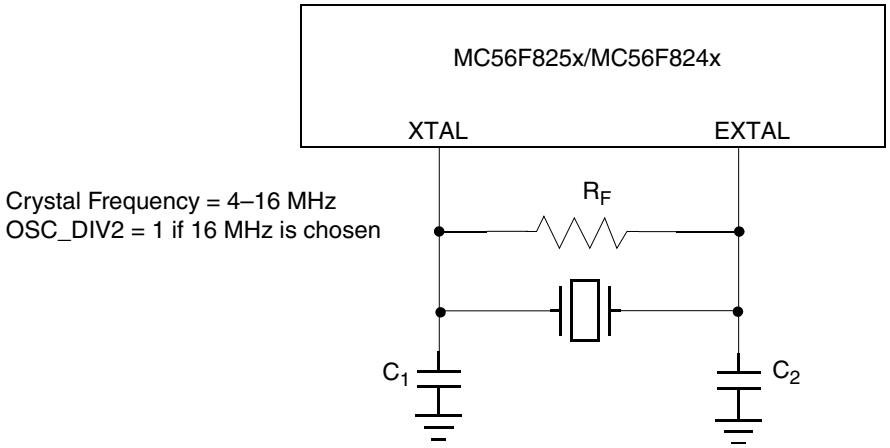


Figure 10. Typical Crystal or Ceramic Resonator Circuit

5.4.3 Alternate External Clock Input

The recommended method of connecting an external clock appears in Figure 11. The external clock source is connected to the CLKIN pin while:

- both the EXT_SEL bit and the CLK_MODE bit in the OSCTL register are set, and
- corresponding bits in the GPIOB_PER register in the GPIO module and the GPS_C0 bit in the GPS0 register in the system integration module (SIM) are set to the correct values.

The external clock input must be generated using a relatively low-impedance driver with a maximum frequency not greater than 120 MHz.

7.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed.

CAUTION

Stress beyond the limits specified in Table 17 may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this section apply over the ambient temperature range of –40 ºC to +105 ºC over the following supply ranges: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0$ V to 3.6 V, CL ≤ 50 pF, $f_{OP} = 60$ MHz.

For functional operating conditions, refer to the remaining tables in the section.

Table 17. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply Voltage Range	V_{DD}		- 0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		- 0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		- 0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		- 0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Groups 1, 2	- 0.3	6.0	V
Oscillator Voltage Range	V_{OSC}	Pin Group 4	- 0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	- 0.3	4.0	V
Input clamp current, per pin ($V_{IN} < 0$)[1]	V_{IC}		—	-20.0	mA
Output clamp current, per pin ($V_O < 0$)[1]	V_{OC}		—	-20.0	mA
Output Voltage Range (Normal Push-Pull mode)	V_{OUT}	Pin Group 1	- 0.3	4.0	V
Output Voltage Range (Open Drain mode)	V_{OUTOD}	Pin Group 2	- 0.3	6.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	- 0.3	4.0	V
Ambient Temperature Industrial	T_A		- 40	105	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		- 55	150	°C

[1] Continuous clamp current per pin is –2.0 mA

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC and Comparator Analog Inputs

Pin Group 4: XTAL, EXTAL

Pin Group 5: DAC analog output

7.3 ESD Protection and Latch-up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing conforms with AEC-Q100 Stress Test Qualification. During device qualification, ESD stresses are performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing conforms with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification. Comprehensive DC parametric and functional testing is performed according to the applicable device specification at room temperature and then at hot temperature, unless specified otherwise in the device specification.

Table 18. MC56F825x/MC56F824x ESD/Latch-up Protection

Characteristic [1]	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	750	—	—	V
Latch-up current at T_A = 85 °C (I_{LAT})	± 100			mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions, unless otherwise noted

7.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the device design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

Table 19. 44LQFP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	70	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	48	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	57	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	42	°C/W
Junction to board		$R_{\theta JB}$	30	°C/W
Junction to case		$R_{\theta JC}$	13	°C/W
Junction to package top	Natural convection	Ψ_{JT}	2	°C/W

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

See Section 8.1, "Thermal Design Considerations," for more detail on thermal design considerations.

7.5 Recommended Operating Conditions

This section contains information about recommended operating conditions.

Table 22. Recommended Operating Conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD}, V_{DDA}		3	3.3	3.6	V
ADC Reference Voltage High	V_{REFHx}		3.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		 0.001 0		 60 60	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2.0		5.5	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	-0.3		0.8	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
DAC Output Load Resistance	R_{LD}	Pin Group 5	3K			Ω
DAC Output Load Capacitance	C_{LD}	Pin Group 5			400	pf
Output Source Current High at V_{OH} min.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -4 -8	mA
Output Source Current Low (at V_{OL} max.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 4 8	mA
Ambient Operating Temperature (Extended Industrial)	T_A		-40		105	°C
Flash Endurance (Program Erase Cycles)	N_F	T_A = -40°C to 125°C	10,000		—	cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15		—	years
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	years

7.8 Power-On Reset, Low Voltage Detection Specification

Table 25. Power-On Reset and Low-Voltage Detection Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Voltage Interrupt for 3.3 V supply[1]	V_{LVI27}	2.6	2.7	2.8	V
Low-Voltage Interrupt for 2.5 V supply[2]	V_{LVI21}	—	2.18	—	V
Low-Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power-On Reset Threshold[3]	POR	2.6	2.7	2.8	V
Brown-Out Reset Threshold[4]	BOR	—	1.8	1.9	V

1 When V_{DD} drops below LVI27, an interrupt is generated.
2 When V_{DD} drops below LVI21, an interrupt is generated.
3 While power is ramping up, this signal remains active for as long as the internal 2.5 V is below 2.18 V or the 3.3 V V_{DD} voltage is below 2.7 V, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp-up until 2.5 V is reached, at which time it self-regulates.
4 Brown-Out Reset occurs whenever the internally regulated 2.5 V digital supply drops below 1.8 V.

7.9 Voltage Regulator Specifications

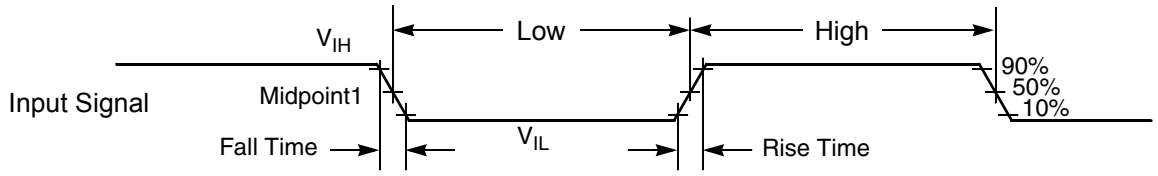
The MC56F825x/MC56F824x has two on-chip regulators. One supplies the PLL, crystal oscillator, NanoEdge placement PWM, and relaxation oscillator. It has no external pins and therefore has no external characteristics that must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.5 V to the MC56F825x/MC56F824x's core logic. For proper operation, this regulator requires an external capacitor of 2.2 µF or greater. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator appear in Table 26.

Table 26. Regulator Parameters

Characteristic	Symbol	Min	Typical	Max	Unit
Short Circuit Current	I_{SS}	—	900	1300	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	minutes

7.10 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 23. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 15.



The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 15. Input Signal Measurement References

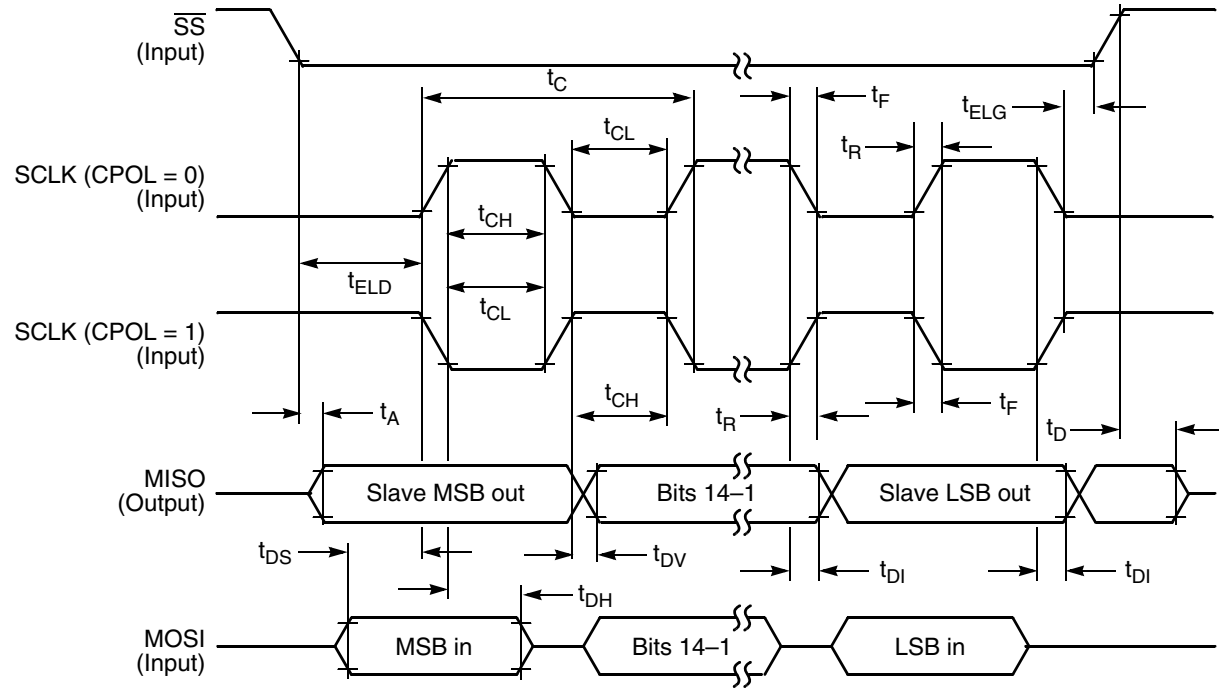


Figure 22. SPI Slave Timing (CPHA = 0)

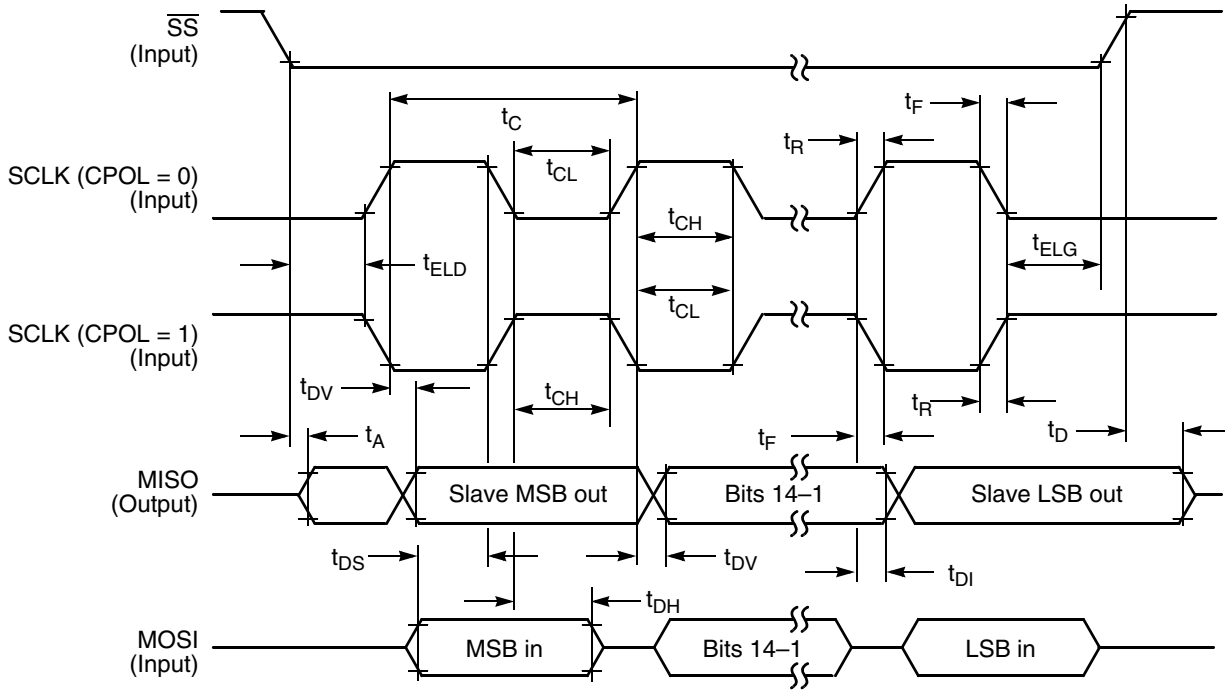


Figure 23. SPI Slave Timing (CPHA = 1)

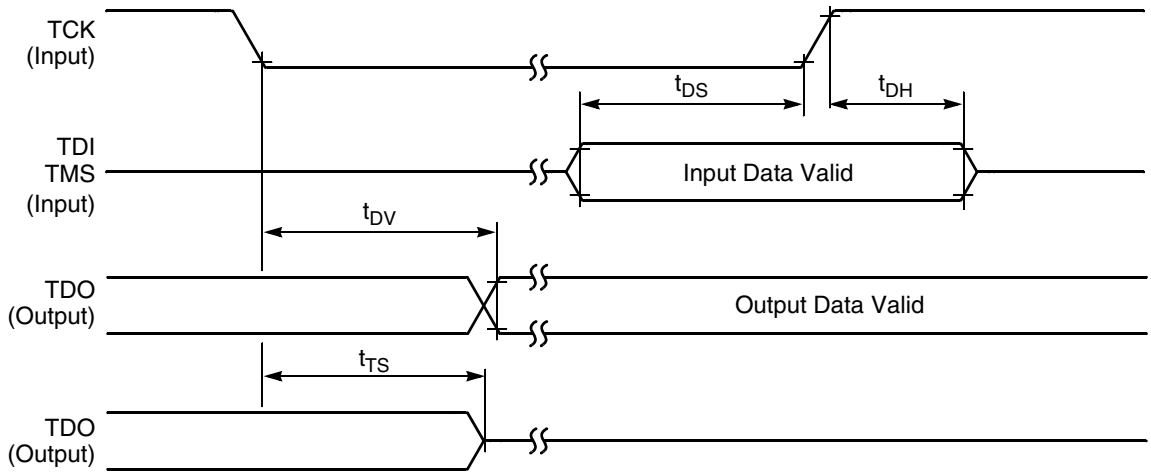


Figure 29. Test Access Port Timing Diagram

7.23 Quad Timer Timing

Table 39. Timer Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	Figure 30
Timer input high/low period	P_{INHL}	1T + 3	—	ns	Figure 30
Timer output period	P_{OUT}	125	—	ns	Figure 30
Timer output high/low period	P_{OUTHL}	50	—	ns	Figure 30

1 In the formulas listed, T = the clock cycle. For 32 MHz operation, T = 31.25 ns.

2. Parameters listed are guaranteed by design.

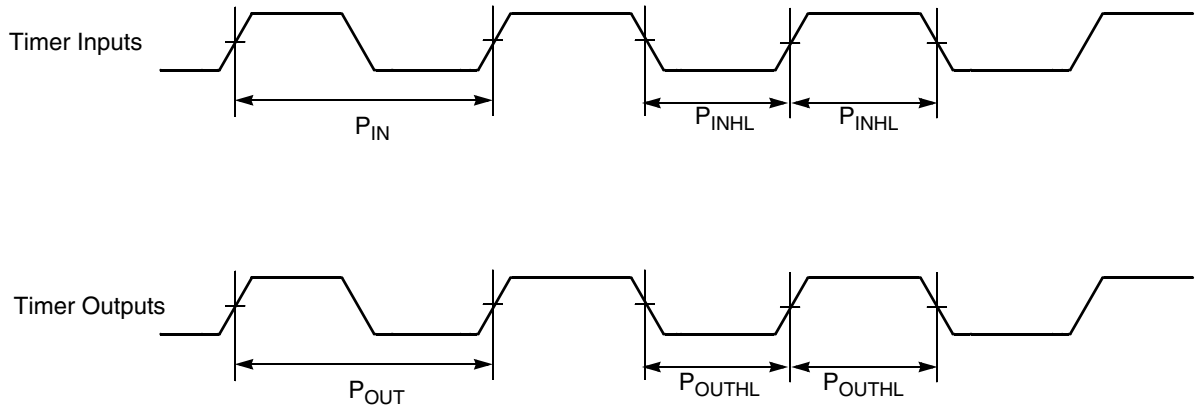


Figure 30. Timer Timing

7.24 COP Specifications

Table 40. COP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Oscillator output frequency	LPFosc	500	1000	1500	Hz
Oscillator current consumption in partial power down mode	IDD		TBD		nA

7.25 Analog-to-Digital Converter (ADC) Parameters

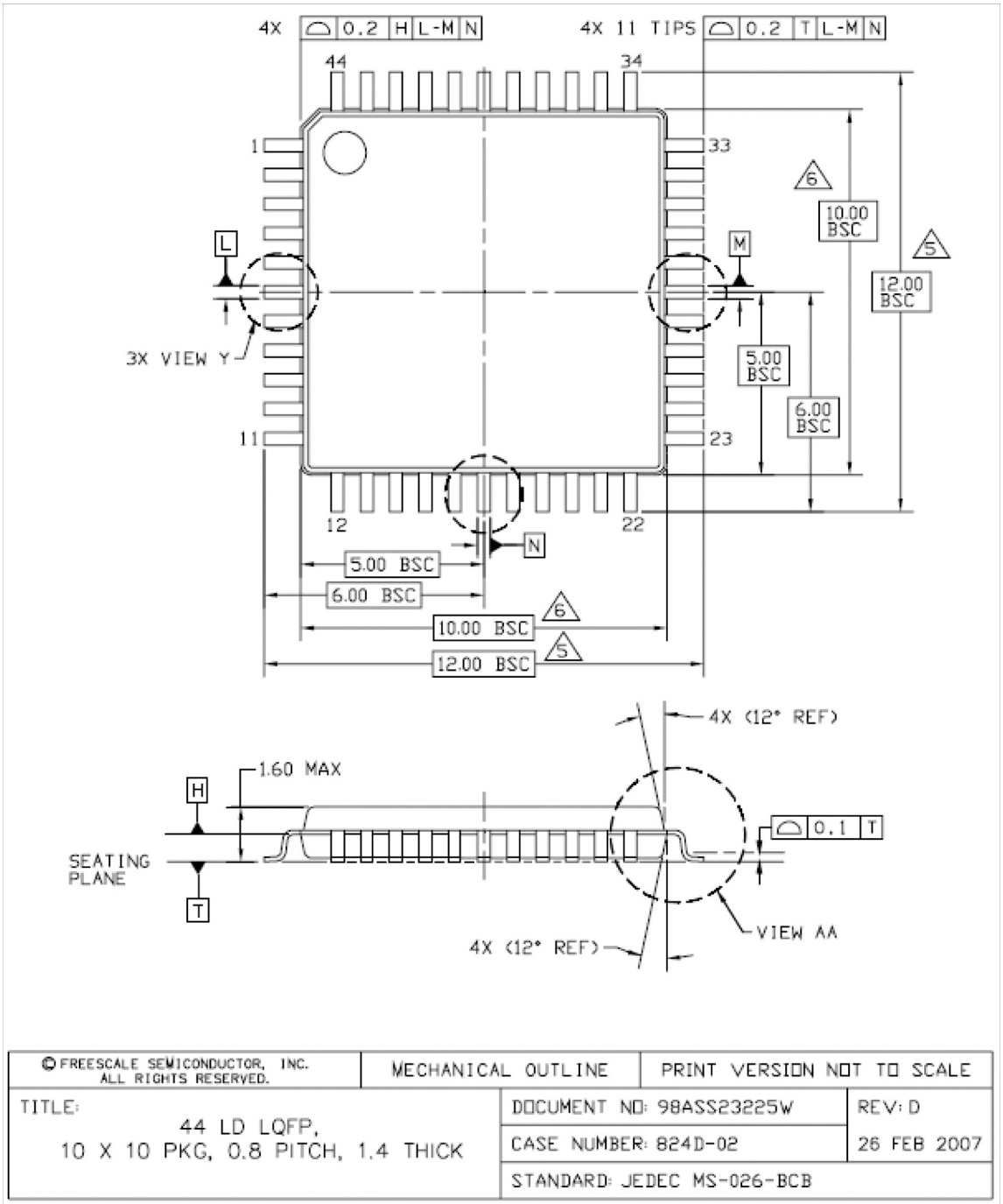
Table 41. ADC Parameters[1]

Parameter	Symbol	Min	Typ	Max	Unit
DC Specifications					
Resolution	R_{ES}	12	—	12	Bits
ADC internal clock	f_{ADIC}	0.1	—	15	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC and VREF power-up time[2](from power down mode)	t_{ADPU}	—	13	—	t_{AIC} cycles[3]
VREF power-up time (from low power mode)	t_{REFPU}	—	6	—	t_{AIC} cycles[3]
ADC RUN current (Speed Control setting) at 100 kHz ADC clock (Standby Mode) at ADC clock ≤ 5 MHz (00) at 5 MHz < ADC clock ≤ 12 MHz (01) at 12 MHz < ADC clock ≤ 15 MHz (10)	I_{ADRUN}	 — — — —	 0.6 10 17 27	 — — — —	mA
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Accuracy (DC or absolute) (gain of 1x, 2x, 4x and f_{ADC} ≤ 10 MHz) (all data in single-ended mode)[4]					
Integral non-linearity[5] (Full input signal range)	INL	—	+/- 3	+/- 6	LSB[6]
Differential non-linearity[5]	DNL	—	+/- 0.6	+/- 1	LSB[5]
Monotonicity	GUARANTEED				
Offset Voltage Internal Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Offset Voltage External Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Gain Error (transfer gain)	E_{GAIN}	—	0.995 to 1.005	1.01 to 0.99	—
ADC Inputs[7] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0.001	—	µA
Input injection current[8], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See Figure 31	—	pF

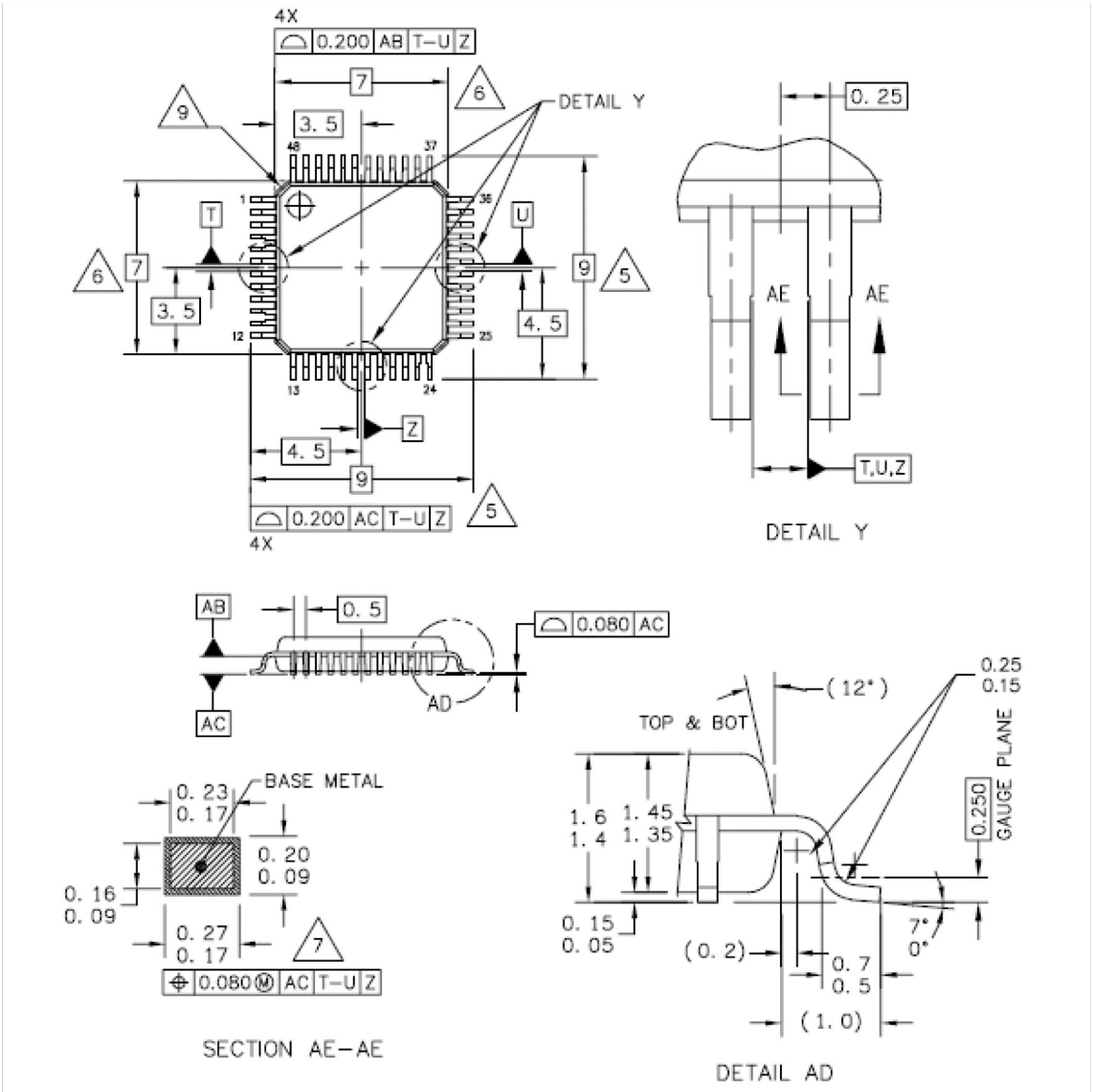
10 Package Mechanical Outline Drawings

To ensure you have the latest version of a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number (shown in the following sections for each package).

10.1 44-pin LQFP



10.2 48-pin LQFP



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TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	DOCUMENT NO: 98ASH00962A	REV: G
	CASE NUMBER: 932-03	14 APR 2005
	STANDARD: JEDEC MS-026-BBC	

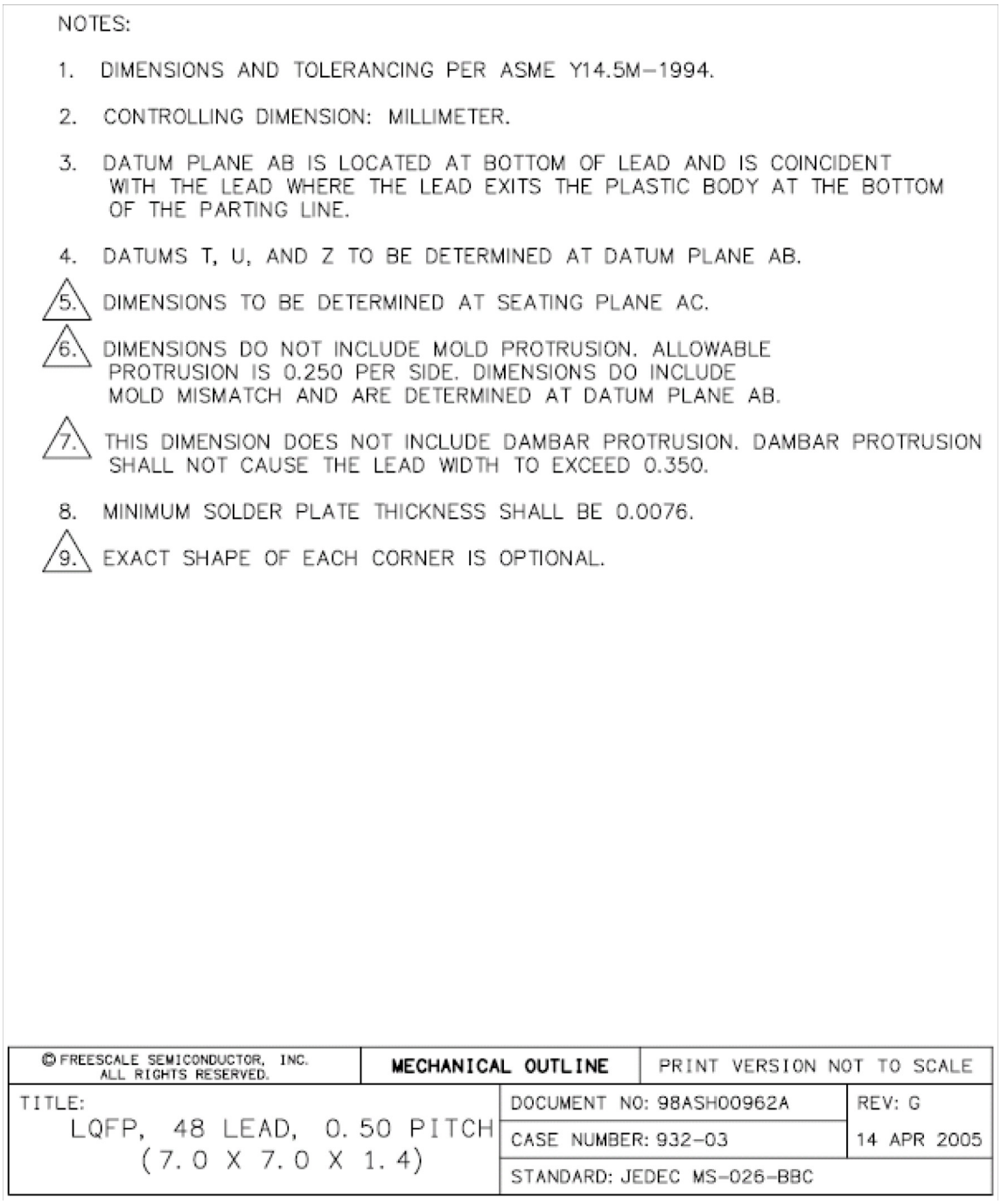
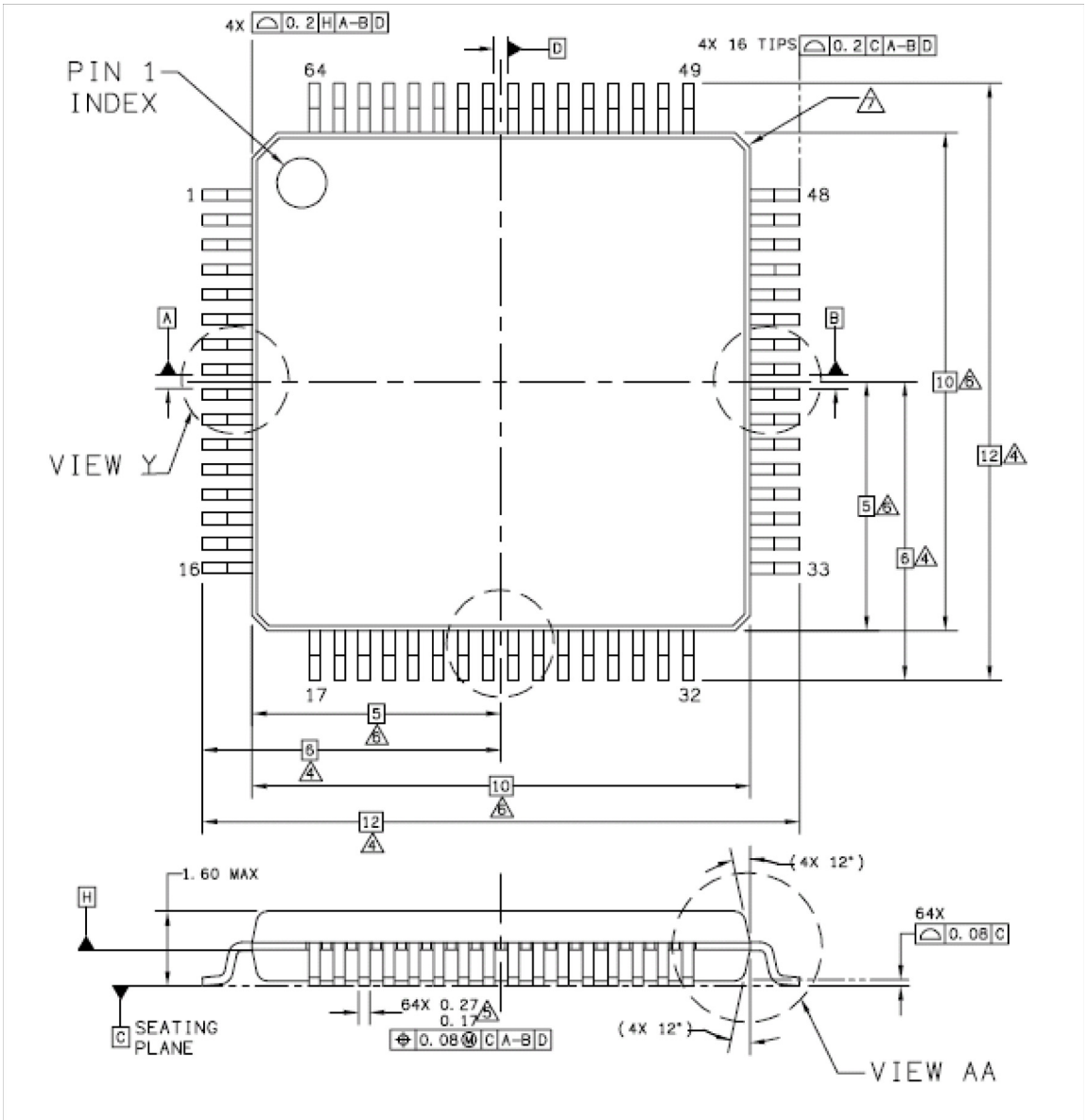


Figure 33. 56F8246 and 56F8256 48-Pin LQFP Mechanical Information

10.3 64-pin LQFP



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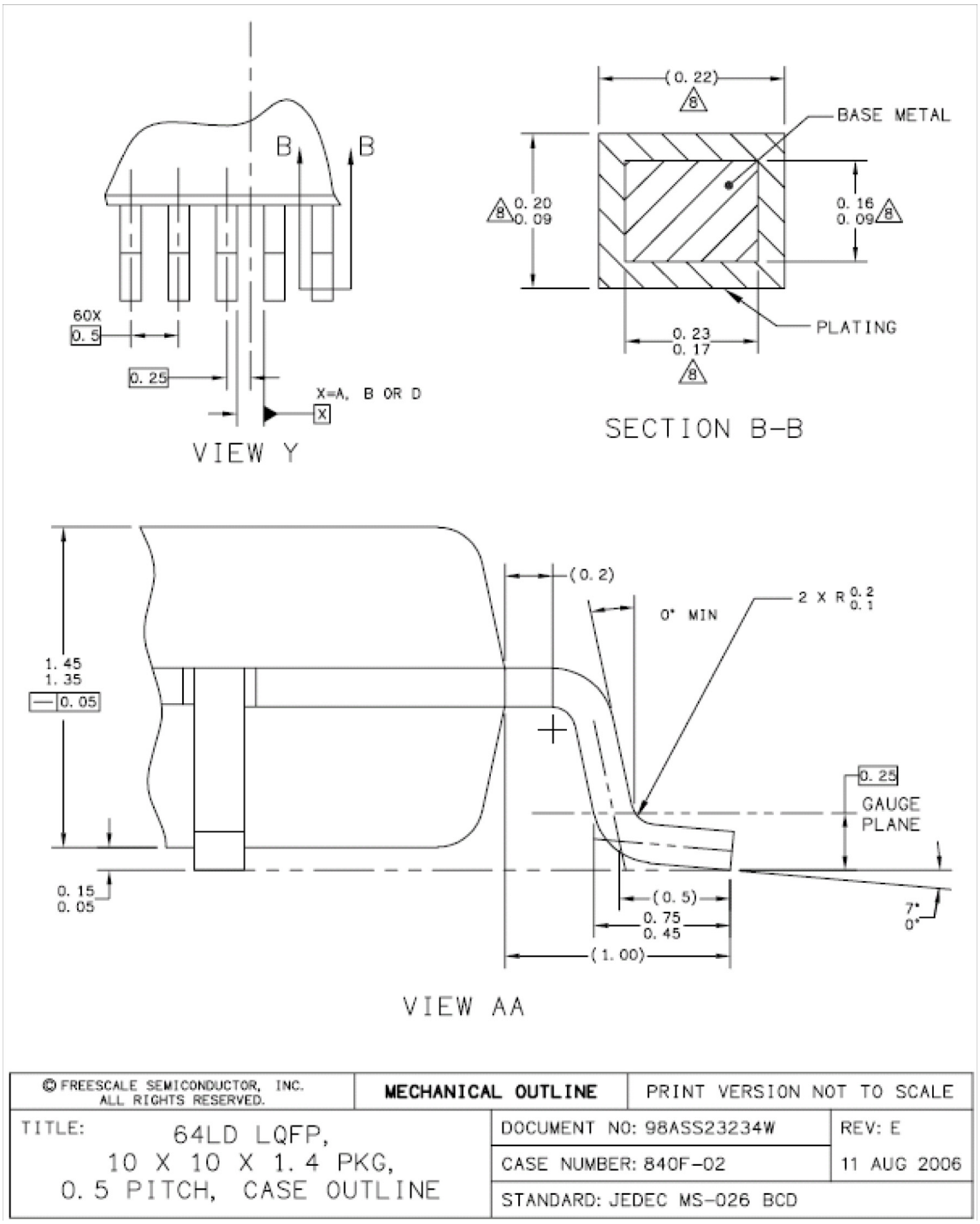
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	



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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: E
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	

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