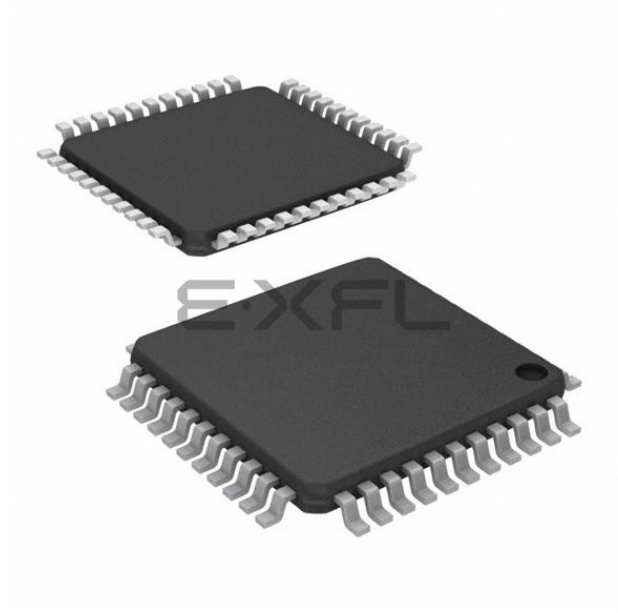

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8255vld

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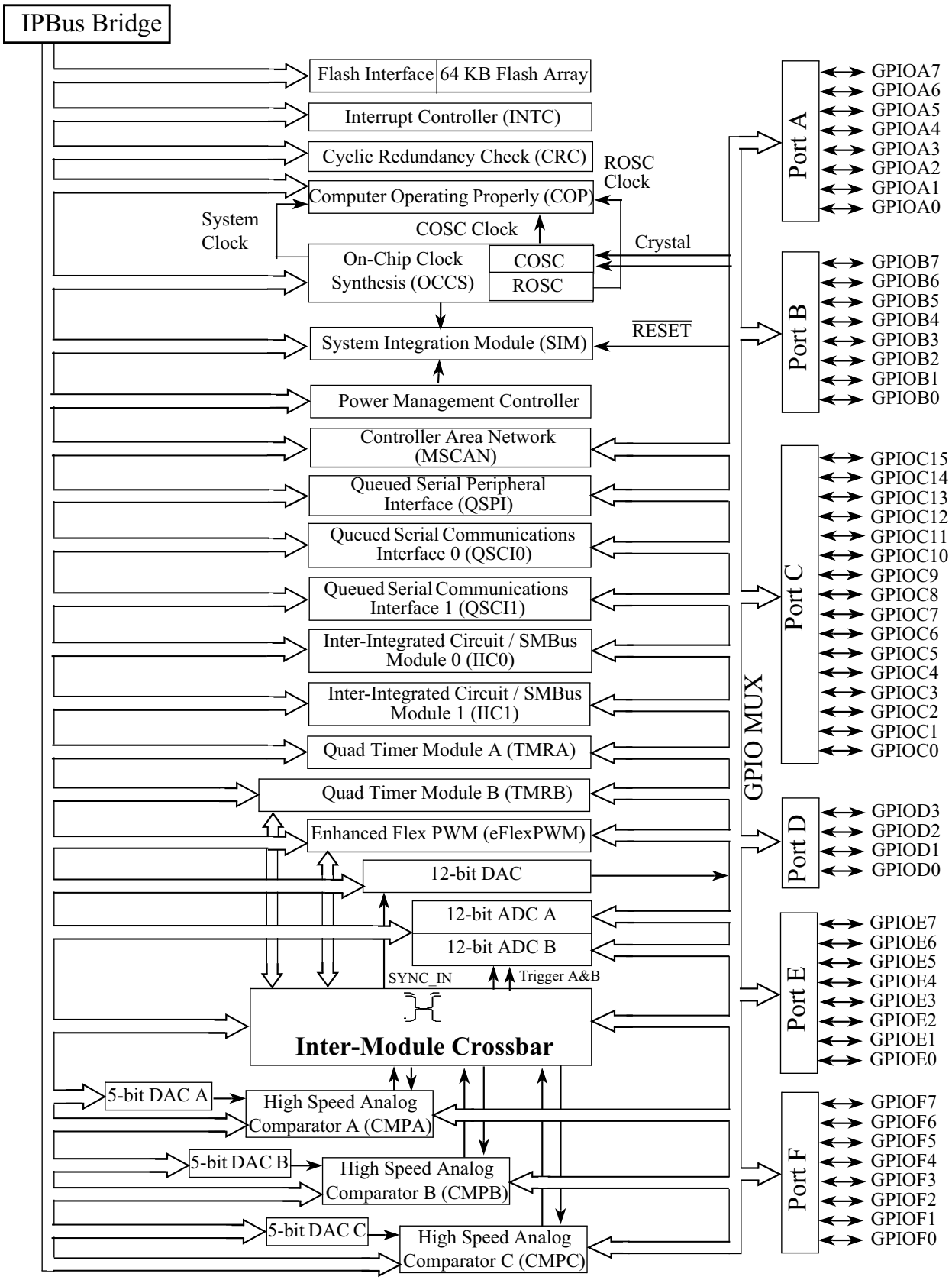


Figure 2. Peripheral Subsystem

1 Pins may be shared with other peripherals. See Table 4.

2 Exclude MC56F824x.

Table 4 summarizes all device pins. Each table row describes the signal or signals present on a pin, sorted by pin number. Peripheral pins in bold identify reset state.

Table 4. MC56F825x/MC56F824x Pins

Pin Number			Pin Name	Peripherals													
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MS CAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
1	1	1	TCK/*GPIOD2*	*GPIOD2*											**TCK**	
2	2	2	$\overline{\text{RESET}}$ / *GPIOD4*	*GPIOD4*												**$\overline{\text{RESET}}$**
3	3	3	GPIOC0/*XTAL/CLKIN*	**GPIOC0**												*XTAL/ CLKIN*
4	4	4	GPIOC1/*EXTAL*	**GPIOC1**												*EXTAL*
5	5	5	GPIOC2/*TXD0/TB0/XB_IN2/ CLKO*	**GPIOC2**		*TXD0*				*XB_IN2*		*TB0*				*CLKO*
		6	GPIOF8/*RXD0/TB1*	**GPIOF8**		*RXD0*						*TB1*				
6	6	7	GPIOC3/*TA0/CMPA_O/RXD0*	**GPIOC3**		*RXD0*					*CMPA_O*	*TA0*				
7	7	8	GPIOC4/*TA1/CMPB_O*	**GPIOC4**							*CMPB_O*	*TA1*				
		9	GPIOA7/*ANA7*	**GPIOA7**					*ANA7*							
		10	GPIOA6/*ANA6*	**GPIOA6**					*ANA6*							
		11	GPIOA5/*ANA5*	**GPIOA5**					*ANA5*							
	8	12	GPIOA4/*ANA4*	**GPIOA4**					*ANA4*							
8	9	13	GPIOA0/*ANA0& CMPA_P2/CMPC_O*	**GPIOA0**					*ANA0*		*CMPA_P2/ CMPC_O*					
9	10	14	GPIOA1/ *ANA1&CMPA_M0*	**GPIOA1**					*ANA1*		*CMPA_M0*					
10	11	15	GPIOA2/*ANA2&VREFHA& CMPA_M1*	**GPIOA2**					*ANA2& VREFHA*		*CMPA_M1*					
11	12	16	GPIOA3/*ANA3&VREFLA& CMPA_M2*	**GPIOA3**					*ANA3& VREFLA*		*CMPA_M2*					
		17	GPIOB7/*ANB7&CMPB_M2*	**GPIOB7**					*ANB7*		*CMPB_M2*					
12	13	18	GPIOC5/*DACO/XB_IN7*	**GPIOC5**						*XB_IN7*						*DACO*
		19	GPIOB6/*ANB6&CMPB_M1*	**GPIOB6**					*ANB6*		*CMPB_M1*					
		20	GPIOB5/*ANB5&CMPC_M2*	**GPIOB5**					*ANB5*		*CMPC_M2*					
	14	21	GPIOB4/*ANB4&CMPC_M1*	**GPIOB4**					*ANB4*		*CMPC_M1*					
13	15	22	V_{DDA}											**V_{DDA}**		
14	16	23	V_{SSA}											**V_{SSA}**		
15	17	24	GPIOB0/ *ANB0&CMPB_P2*	**GPIOB0**					*ANB0*		*CMPB_P2*					
16	18	25	GPIOB1/ *ANB1&CMPB_M0*	**GPIOB1**					*ANB1*		*CMPB_M0*					
17	19	26	V_{CAP}											**V_{CAP}**		
18	20	27	GPIOB2/ *ANB2&VREFHB&CMPC_P2*	**GPIOB2**					*ANB2& VREFHB*		*CMPC_P2*					

Table 4. MC56F825x/MC56F824x Pins (continued)

Pin Number			Pin Name	Peripherals													
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MSCAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
19	21	28	GPIOB3/ *ANB3&VREFLB&CMPC_M0*	**GPIOB3**					*ANB3& VREFLB*		*CMPC_M0*					
		29	V_{DD}											**V_{DD}**		
20	22	30	V_{SS}											**V_{SS}**		
21	23	31	GPIOC6/*TA2/XB_IN3/ CMP_REF*	**GPIOC6**						*XB_IN3*	*CMP_REF*	*TA2*				
22	24	32	GPIOC7/$\overline{SS}$/*TXD0*	**GPIOC7**		*TXD0*	$\overline{SS}$									
23	25	33	GPIOC8/*MISO/RXD0*	**GPIOC8**		*RXD0*	*MISO*									
24	26	34	GPIOC9/*SCLK/XB_IN4*	**GPIOC9**			*SCLK*			*XB_IN4*						
25	27	35	GPIOC10/MOSI/XB_IN5/MISO	**GPIOC10**			MOSI/ MISO			XB_IN5						
	28	36	GPIOF0/*XB_IN6*	**GPIOF0**						*XB_IN6*						
26	29	37	GPIOC11/*CANTX/SCL1/TXD1*	**GPIOC11**	*SCL1*	*TXD1*		*CANTX*								
27	30	38	GPIOC12/*CANRX/SDA1/RXD1*	**GPIOC12**	*SDA1*	*RXD1*		*CANRX*								
		39	GPIOF2/*SCL1/XB_OUT2*	**GPIOF2**	*SCL1*					*XB_OUT2*						
		40	GPIOF3/*SDA1/XB_OUT3*	**GPIOF3**	*SDA1*					*XB_OUT3*						
		41	GPIOF4/*TXD1/XB_OUT4*	**GPIOF4**		*TXD1*				*XB_OUT4*						
		42	GPIOF5/*RXD1/XB_OUT5*	**GPIOF5**		*RXD1*				*XB_OUT5*						
28	31	43	V_{SS}											**V_{SS}**		
29	32	44	V_{DD}											**V_{DD}**		
30	33	45	GPIOE0/*PWM0B*	**GPIOE0**									*PWM0B*			
31	34	46	GPIOE1/*PWM0A*	**GPIOE1**									*PWM0A*			
32	35	47	GPIOE2/*PWM1B*	**GPIOE2**									*PWM1B*			
33	36	48	GPIOE3/*PWM1A*	**GPIOE3**									*PWM1A*			
34	37	49	GPIOC13/*TA3/XB_IN6*	**GPIOC13**						*XB_IN6*		TA3				
	38	50	GPIOF1/*CLKO/XB_IN7*	**GPIOF1**						*XB_IN7*						*CLKO*
35	39	51	GPIOE4/*PWM2B/XB_IN2*	**GPIOE4**						*XB_IN2*			*PWM2B*			
36	40	52	GPIOE5/*PWM2A/XB_IN3*	**GPIOE5**						*XB_IN3*			*PWM2A*			
		53	GPIOE6/*PWM3B/XB_IN4*	**GPIOE6**						*XB_IN4*			*PWM3B*			
		54	GPIOE7/*PWM3A/XB_IN5*	**GPIOE7**						*XB_IN5*			*PWM3A*			
37	41	55	GPIOC14/*SDA0/XB_OUT0*	**GPIOC14**	*SDA0*					*XB_OUT0*						
38	42	56	GPIOC15/*SCL0/XB_OUT1*	**GPIOC15**	*SCL0*					*XB_OUT1*						
39	43	57	V_{CAP}											**V_{CAP}**		
		58	GPIOF6/*TB2/PWM3X*	**GPIOF6**								*TB2*	*PWM3X*			
		59	GPIOF7/*TB3*	**GPIOF7**								*TB3*				
40	44	60	V_{DD}											**V_{DD}**		

3.3 MC56F825x/MC56F824x Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses and as *italic*, must be programmed via the GPIO module's peripheral enable registers (GPIO_x_PER) and the SIM module's GPIO peripheral select (GPSx) registers.

Table 5. MC56F825x/MC56F824x Signal and Package Information

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
V_{DD}			29	Supply	Supply	I/O Power — This pin supplies 3.3 V power to the chip I/O interface.
V_{DD}	29	32	44			
V_{DD}	40	44	60			
V_{SS}	20	22	30	Supply	Supply	I/O Ground — These pins provide ground for chip I/O interface.
V_{SS}	28	31	43			
V_{SS}	41	45	61			
V_{DDA}	13	15	22	Supply	Supply	Analog Power — This pin supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	14	16	23	Supply	Supply	Analog Ground — This pin supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	17	19	26	Supply	Supply	V_{CAP} — Connect a bypass capacitor of 2.2 µF or greater between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation. See Section 8.2, "Electrical Design Considerations," on page 73.
V_{CAP}	39	43	57			
TDI *(GPIOD0)*	44	48	64	Input Input/ Output	Input, internal pullup enabled	Test Data Input — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDI.
TDO *(GPIOD1)*	42	46	62	Output Input/ Output	Output	Test Data Output — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
TCK *(GPIOD2)*	1	1	1	Input Input/ Output	Input, internal pullup enabled	Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TCK

Table 11. 56F8245/56 Data Memory Map[1]

Begin/End Address	Memory Allocation
X:0xFF FFFF X:0xFF FF00	EOnCE 256 locations allocated
X:0xFF FEFF X:0x01 0000	RESERVED
X:0x00 FFFF X:0x00 F000	On-Chip Peripherals 4096 locations allocated
X:0x00 EFFF X:0x00 8C00	RESERVED
X:0x00 8BFF X:0x00 8000	On-Chip Data RAM Alias
X:0x00 7FFF X:0x00 0C00	RESERVED
X:0x00 0BFF X:0x00 0000	On-Chip Data RAM 6 KB[2]

1 All addresses are 16-bit word addresses.

2 This RAM is shared with program space starting at P: 0x00 8000. See Figure 8.

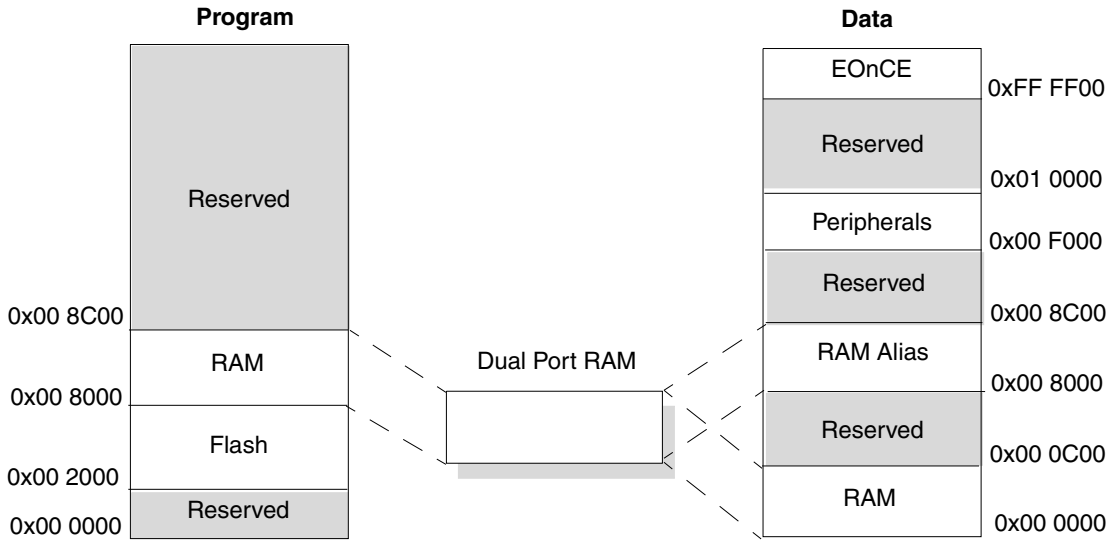


Figure 8. 56F8245/46 Dual Port RAM Map

4.4 Interrupt Vector Table and Reset Vector

The location of the vector table is determined by the vector base address register (VBA). The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower seven bits are determined based on the highest priority interrupt and are then appended to VBA before presenting the full VAB to the core. Refer to the device's reference manual for details.

The reset startup addresses of 56F824x and 56F825x are different.

- The 56F825x's startup address is located at 0x00 0000. The reset value of VBA is reset to a value of 0x0000 that corresponds to the address 0x00 0000.

Table 13. EOnCE Memory Map

Address	Register Abbreviation	Register Name
X:0xFF FF91–X:0xFF FF90	OBMSK (32 bits)	Breakpoint Unit Mask Register 2
X:0xFF FF8F		Reserved
X:0xFF FF8E	OBCNTR	EOnCE Breakpoint Unit Counter
X:0xFF FF8D		Reserved
X:0xFF FF8C		Reserved
X:0xFF FF8B		Reserved
X:0xFF FF8A	OESCR	External Signal Control Register
X:0xFF FF89 –X:0xFF FF00		Reserved

5 General System Control Information

5.1 Overview

This section discusses power pins, reset sources, interrupt sources, clock sources, the system integration module (SIM), ADC synchronization, and JTAG/EOnCE interfaces.

5.2 Power Pins

V_{DD}, V_{SS} and V_{DDA}, V_{SSA} are the primary power supply pins for the device. The voltage source supplies power to all on-chip peripherals, I/O buffer circuitry, and internal voltage regulators. The device has multiple internal voltages to provide regulated lower-voltage sources for the peripherals, core, memory, and on-chip relaxation oscillators.

Typically, at least two separate capacitors are across the power pins to bypass the glitches and provide bulk charge storage. In this case, a bulk electrolytic or tantalum capacitor, such as a 10 µF tantalum capacitor, should provide bulk charge storage for the overall system, and a 0.1 µF ceramic bypass capacitor should be located as near to the device power pins as is practical to suppress high-frequency noise. Each pin must have a bypass capacitor for optimal noise suppression.

V_{DDA} and V_{SSA} are the analog power supply pins for the device. This voltage source supplies power to the ADC, PGA, and CMP modules. A 0.1 µF ceramic bypass capacitor should be located as near to the device V_{DDA} and V_{SSA} pins as is practical to suppress high-frequency noise. V_{DDA} and V_{SSA} are also the voltage reference high and voltage reference low inputs, respectively, for the ADC module.

5.3 Reset

Resetting the device provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values, and the program counter is loaded from the reset vector. On-chip peripheral modules are disabled and I/O pins are initially configured at the reset status shown in Table 5 on page 18.

The MC56F825x/MC56F824x has the following sources for reset:

- Power-on reset (POR)
- Partial power-down reset (PPD)
- Low-voltage detect (LVD)
- External pin reset (EXTR)
- Computer operating properly loss of reference reset (COP_LOR)
- Computer operating properly time-out reset (COP_CPU)

when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable startup. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances. The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and startup stabilization time. When using low-frequency, low-power mode, the only external component is the crystal itself. In the other oscillator modes, load capacitors (C_x, C_y) and feedback resistor (R_F) are required. In addition, a series resistor (R_S) may be used in high-gain modes. Recommended component values appear in Table 27.

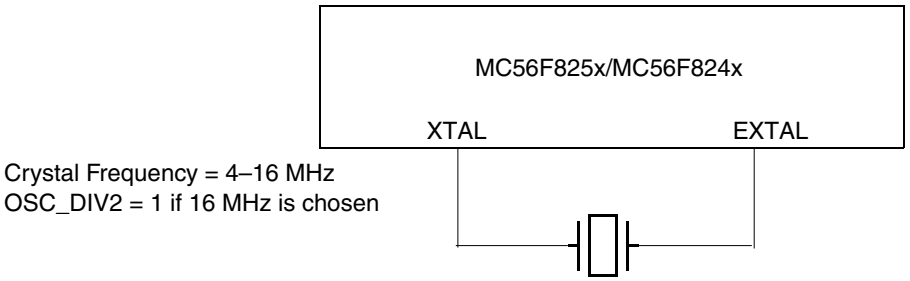


Figure 9. Typical Crystal Oscillator Circuit without Frequency Compensation Capacitor

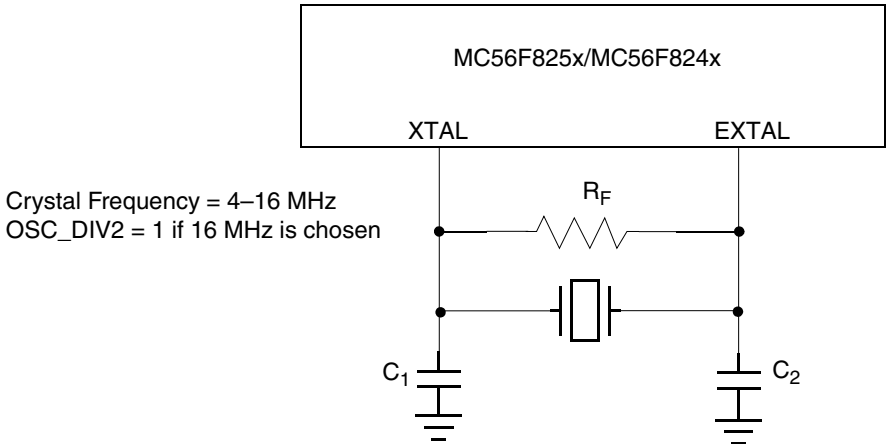


Figure 10. Typical Crystal or Ceramic Resonator Circuit

5.4.3 Alternate External Clock Input

The recommended method of connecting an external clock appears in Figure 11. The external clock source is connected to the CLKIN pin while:

- both the EXT_SEL bit and the CLK_MODE bit in the OSCTL register are set, and
- corresponding bits in the GPIOB_PER register in the GPIO module and the GPS_C0 bit in the GPS0 register in the system integration module (SIM) are set to the correct values.

The external clock input must be generated using a relatively low-impedance driver with a maximum frequency not greater than 120 MHz.

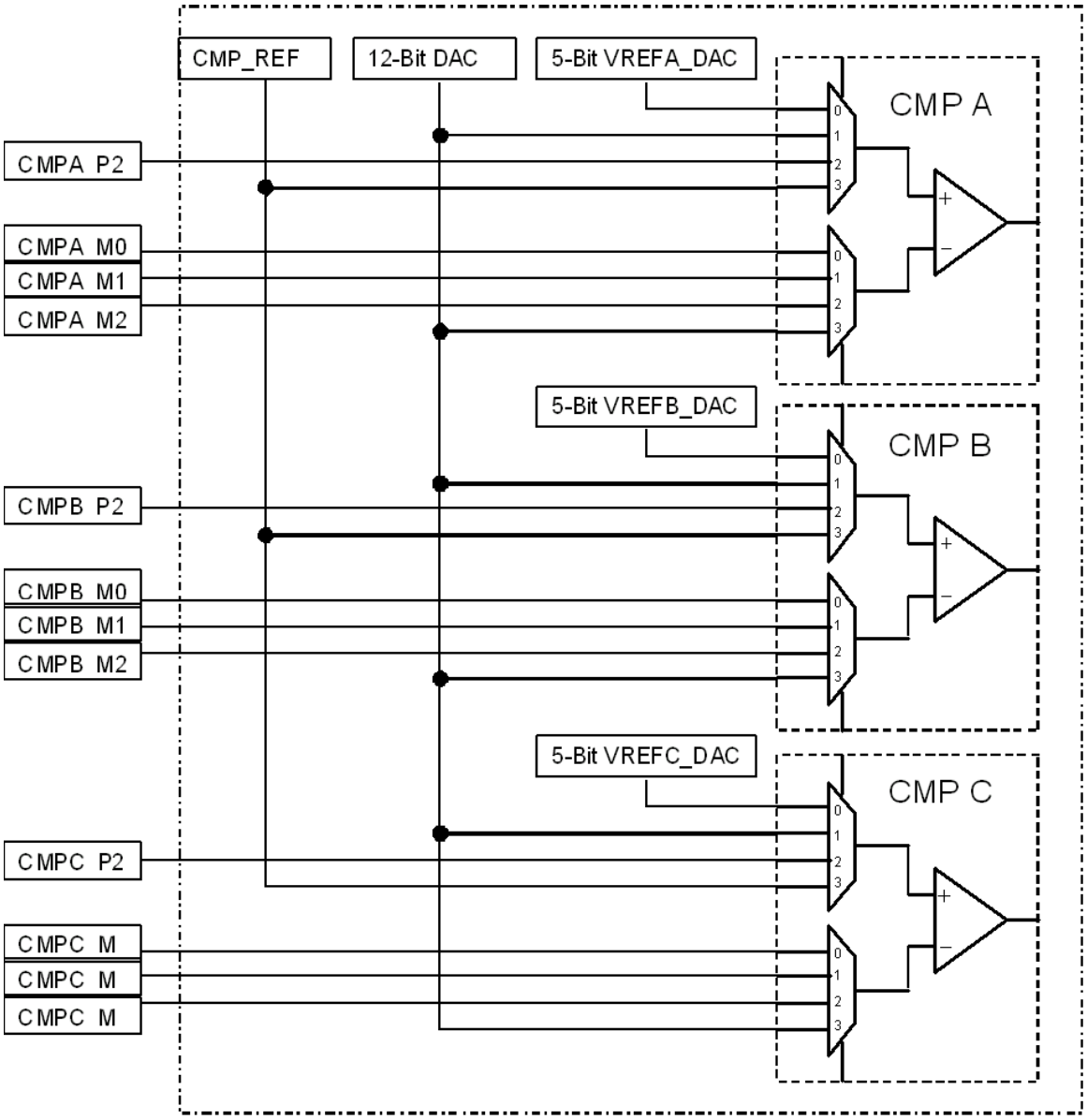


Figure 12. On-Chip Comparator Connections

Table 14. Connections by Comparator Inputs

Comparator Input	Comparator A	Comparator B	Comparator B
P0 (from internal)	5-bit VREFA_DAC	5-bit VREFB_DAC	5-bit VREFC_DAC
P1 (from internal)	12-bit DAC	12-bit DAC	12-bit DAC
P2 (from package pin)	CMPA_P2	CMPB_P2	CMPC_P2
P3 (from package pin)	CMP_REF	CMP_REF	CMP_REF

Table 16. Crossbar Output Signal Assignments (continued)

XBAR_OUTn	Output to	Function
XBAR_OUT7	ADCB	ADCB Trigger
XBAR_OUT8	DAC	12-bit DAC SYNC_IN
XBAR_OUT9	CMPA	Comparator A Window/Sample
XBAR_OUT10	CMPB	Comparator B Window/Sample
XBAR_OUT11	CMPC	Comparator C Window/Sample
XBAR_OUT12	PWM0 EXTA	eFlexPWM submodule 0 Alternate Control signal
XBAR_OUT13	PWM1 EXTA	eFlexPWM submodule 1 Alternate Control signal
XBAR_OUT14	PWM2 EXTA	eFlexPWM submodule 2 Alternate Control signal
XBAR_OUT15	PWM3 EXTA	eFlexPWM submodule 3 Alternate Control signal
XBAR_OUT16	PWM0 EXT_SYNC	eFlexPWM submodule 0 External Synchronization signal
XBAR_OUT17	PWM1 EXT_SYNC	eFlexPWM submodule 1 External Synchronization signal
XBAR_OUT18	PWM2 EXT_SYNC	eFlexPWM submodule 2 External Synchronization signal
XBAR_OUT19	PWM3 EXT_SYNC	eFlexPWM submodule 3 External Synchronization signal
XBAR_OUT20	PWM EXT_CLK	eFlexPWM External Clock signal
XBAR_OUT21	PWM FAULT0	eFlexPWM Module FAULT0
XBAR_OUT22	PWM FAULT1	eFlexPWM Module FAULT1
XBAR_OUT23	PWM FAULT2	eFlexPWM Module FAULT2
XBAR_OUT24	PWM FAULT3	eFlexPWM Module FAULT3
XBAR_OUT25	PWM FORCE	eFlexPWM External Output Force signal
XBAR_OUT26	TB0	Quad Timer B0 Input when SIM_GPS3[12] is set
XBAR_OUT27	TB1	Quad Timer B1 Input when SIM_GPS3[13] is set
XBAR_OUT28	TB2	Quad Timer B2 Input when SIM_GPS3[14] is set
XBAR_OUT29	TB3	Quad Timer B3 Input when SIM_GPS3[15] is set

5.7.3 Interconnection of PWM Module and ADC Module

In addition to how PWM0_EXTA, PWM1_EXTA, PWM2_EXTA, and PWM3_EXTA connect to crossbar outputs, the ADC conversion high/low limit compare results of sample0, sample1, and sample2 are used to drive PWM0_EXTB, PWM1_EXTB, and PWM2_EXTB, respectively. PWM3_EXTB is permanently tied to GND.

State of PWM0_EXTB:

- If the ADC conversion result in SAMPLE0 is greater than the value programmed into the high limit register 0, PWM0_EXTB is driven low.
- If the ADC conversion result in SAMPLE0 is less than the value programmed into the low limit register 0, PWM0_EXTB is driven high.

State of PWM1_EXTB:

- If the ADC conversion result in SAMPLE1 is greater than the value programmed into the high limit register 1, PWM1_EXTB is driven low.

7.8 Power-On Reset, Low Voltage Detection Specification

Table 25. Power-On Reset and Low-Voltage Detection Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Voltage Interrupt for 3.3 V supply[1]	V_{LVI27}	2.6	2.7	2.8	V
Low-Voltage Interrupt for 2.5 V supply[2]	V_{LVI21}	—	2.18	—	V
Low-Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power-On Reset Threshold[3]	POR	2.6	2.7	2.8	V
Brown-Out Reset Threshold[4]	BOR	—	1.8	1.9	V

1 When V_{DD} drops below LVI27, an interrupt is generated.
2 When V_{DD} drops below LVI21, an interrupt is generated.
3 While power is ramping up, this signal remains active for as long as the internal 2.5 V is below 2.18 V or the 3.3 V V_{DD} voltage is below 2.7 V, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp-up until 2.5 V is reached, at which time it self-regulates.
4 Brown-Out Reset occurs whenever the internally regulated 2.5 V digital supply drops below 1.8 V.

7.9 Voltage Regulator Specifications

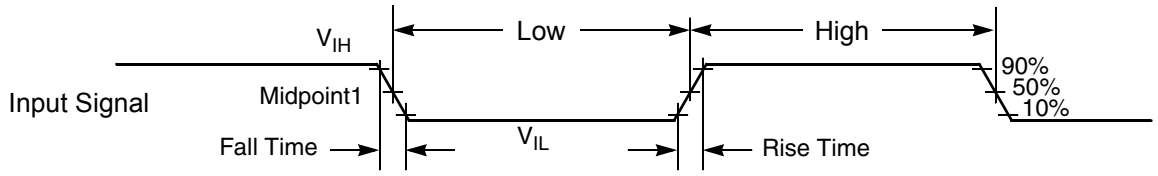
The MC56F825x/MC56F824x has two on-chip regulators. One supplies the PLL, crystal oscillator, NanoEdge placement PWM, and relaxation oscillator. It has no external pins and therefore has no external characteristics that must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.5 V to the MC56F825x/MC56F824x's core logic. For proper operation, this regulator requires an external capacitor of 2.2 µF or greater. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator appear in Table 26.

Table 26. Regulator Parameters

Characteristic	Symbol	Min	Typical	Max	Unit
Short Circuit Current	I_{SS}	—	900	1300	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	minutes

7.10 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 23. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 15.



The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 15. Input Signal Measurement References

7.15 External Crystal or Resonator Requirement

Table 31. Crystal or Resonator Requirement

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation	f_{XOSC}	4	8	16	MHz

7.16 Relaxation Oscillator Timing

Table 32. Relaxation Oscillator Timing

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
Relaxation oscillator output frequency[1] Normal Mode Standby Mode	f_{op}	—	 8.05 400	—	 MHz kHz
Relaxation oscillator stabilization time[2]	t_{roscs}	—	1	3	ms
Cycle-to-cycle jitter. This is measured on the CLKO signal (programmed prescaler_clock) over 264 clocks[3]	$t_{jitterrosc}$	—	400	—	ps
Variation over temperature –40°C to 150°C[4]		—	+1.5 to –1.5	+3.0 to –3.0	%
Variation over temperature 0°C to 105°C[4]		—	0 to +1	+2.0 to –2.0	%

1 Output frequency after factory trim.

2 This is the time required from standby to normal mode transition.

3 J_A is required to meet QSCI requirements.

4 See Figure 18.

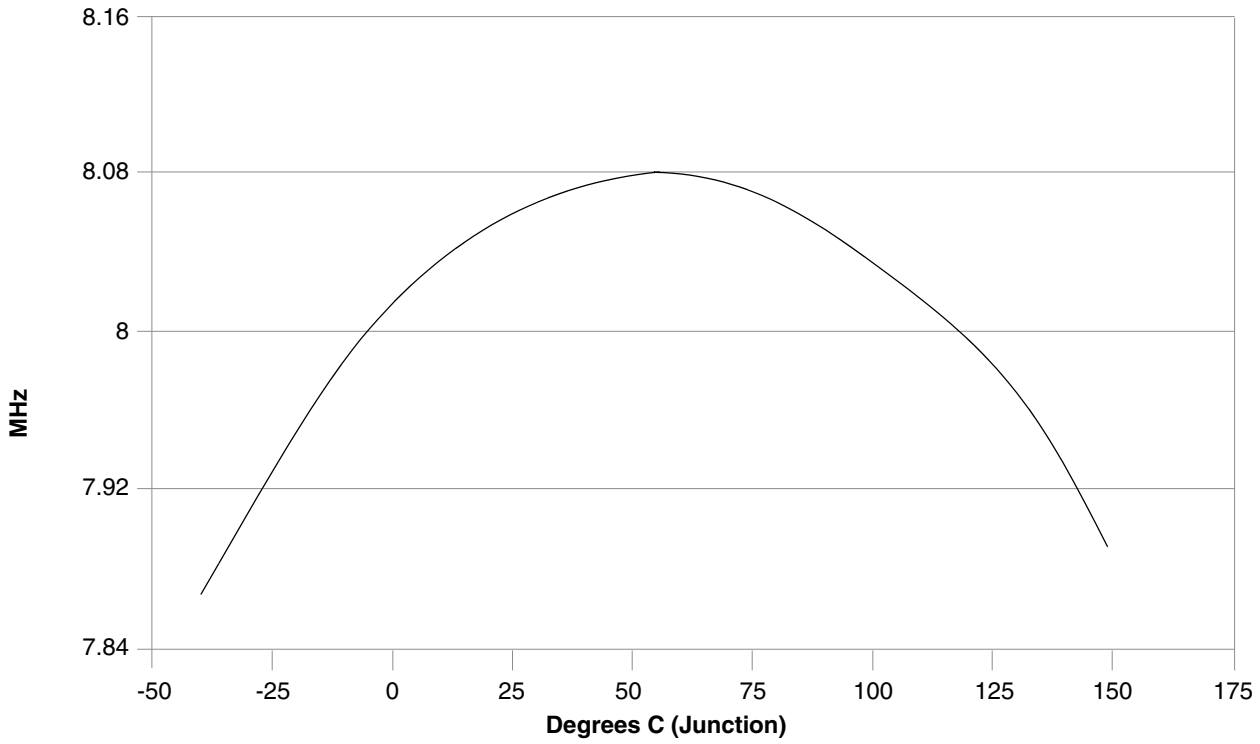


Figure 18. Relaxation Oscillator Temperature Variation (Typical) After Trim

Table 34. SPI Timing[1] (continued)

Characteristic	Symbol	Min	Max	Unit	Refer to
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Access time (time to data active from high-impedance state) Slave	t_A	 4.8	 15	 ns	Figure 23
Disable time (hold time to high-impedance state) Slave	t_D	 3.7	 15.2	 ns	Figure 23
Data valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23

[1] Parameters listed are guaranteed by design.

Table 41. ADC Parameters[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Input impedance	X_{IN}	—	See Figure 31	—	Ohms
AC Specifications[9] (gain of 1x, 2x, 4x and $f_{ADC} \leq$ 10 MHz)[4]					
Signal-to-noise ratio	SNR	—	59		dB
Total Harmonic Distortion	THD	—	64		dB
Spurious Free Dynamic Range	SFDR	—	65		dB
Signal-to-noise plus distortion	SINAD	—	59		dB
Effective Number Of Bits	ENOB	—	9.5		Bits

1 All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2 Includes power-up of ADC and V_{REF}
3 ADC clock cycles
4 Speed register setting must be 00 for ADC clock ≤ 5 MHz, 01 for 5 MHz < ADC clock ≤ 12 MHz, and 10 for ADC clock > 12 MHz
5 INL and DNL measured from V_{IN} = V_{REFL} to V_{IN} = V_{REFH}
6 LSB = Least Significant Bit = 0.806 mV at x1 gain
7 Pin groups are detailed following Table 17.
8 The current that can be injected or sourced from an unselected ADC signal input without affecting the performance of the ADC
9 ADC PGA gain is x1

7.25.1 Equivalent Circuit for ADC Inputs

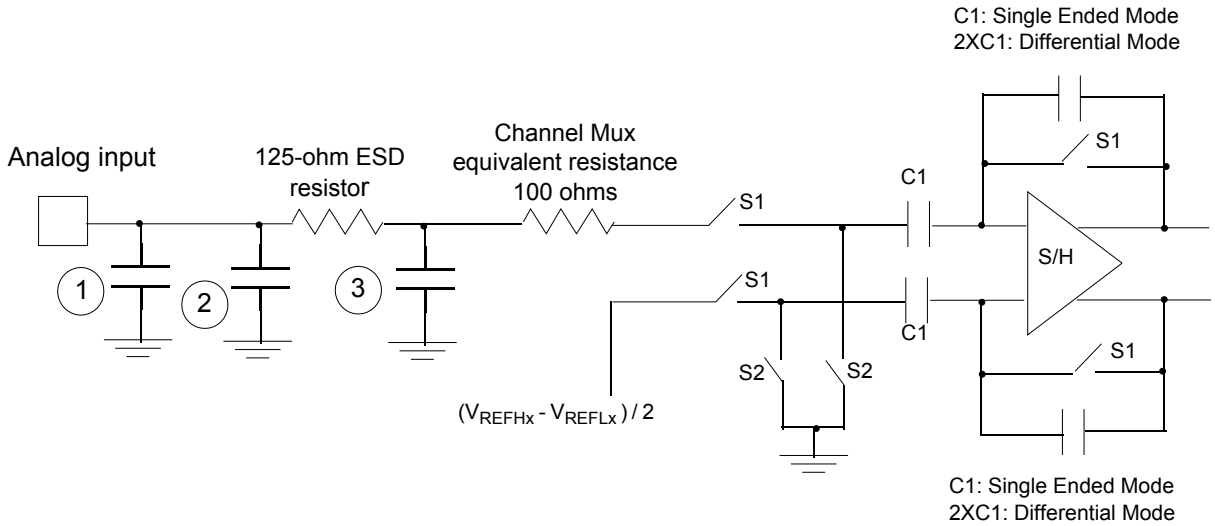
Figure 31 illustrates the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases and operate at the ADC clock frequency. Equivalent input impedance, when the input is selected, is as follows:

$$(2 \times k / ADCClockRate \times C_{gain}) + 100 \text{ ohms} + 125 \text{ ohms} \qquad \textit{Eqn. 1}$$

where k =

- 1 for first sample
- 6 for subsequent samples

and C_{gain} is as described in note 4 below.



1. Parasitic capacitance due to package, pin-to-pin, and pin-to-package base coupling: 1.8 pF

1 No guaranteed specification within 5% of V_{DDA} or V_{SSA}
2 LSB = 0.806 mV

7.27 5-Bit Digital-to-Analog Converter (DAC) Parameters

Table 43. 5-Bit DAC Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Reference Inputs	Vin	V_{DDA}	—	V_{DDA}	mV
Setup Delay	t_{PRGST}	TBD	TBD	TBD	ns
Step size	V_{STEP}	3Vin/128	Vin/32	5Vin/128	V
Output Range	V_{DACOUT}	Vin/32	—	Vin	ns

7.28 HSCMP Specifications

Table 44. HSCMP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Analog input voltage	V_{AIN}	V_{SSA} – 0.01	—	V_{DDA} + 0.01	V
Analog input offset voltage[1]	V_{AIO}	—	—	40	mV
Analog comparator hysteresis[2]	V_H	—	1 to 16	—	mV
Propagation Delay, high speed mode (EN=1, PMODE=1),	t_{DHSN}[3]	—	70	140	ns
Propagation Delay, Low Speed Mode (EN=1, PMODE=0),	t_{AINIT}[4]	—	400	600	ns

1 Offset when the degree of hysteresis is set to its minimum value.
2 The range of hysteresis is based on simulation only. This range varies from part to part.
3 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.
4 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.

7.29 Optimize Power Consumption

See Section 7.7, "Supply Current Characteristics," for a list of I_{DD} requirements for the MC56F825x/MC56F824x. This section provides additional details for optimizing power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static] component
+B: internal [state-dependent] component
+C: internal [dynamic] component
+D: external [dynamic] component
+E: external [static] component

A, the internal [static] component, consists of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent] component, reflects the supply current required by certain on-chip resources only when those resources are in use. These resources include RAM, flash memory, and the ADCs.

C, the internal [dynamic] component, is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic] component, reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This component is also commonly described as $C*V^2*F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 45. I/O Loading Coefficients at 10 MHz

	Intercept	Slope
8 mA drive	1.3	0.11 mW/pF
4 mA drive	1.15 mW	0.11 mW/pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. Table 45 provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases, Equation 2 applies.

$$TotalPower = \Sigma((Intercept + Slope*C_{load})*frequency/10\ MHz) \qquad Eqn.\ 2$$

where:

— Summation is performed over all output pins with capacitive loads.

— Total power is expressed in mW.

— C_{load} is expressed in pF.

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static] component, reflects the effects of placing resistive loads on the outputs of the device. Total all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of nine PWM outputs driving 10 mA into LEDs, then P = 8*0.5*0.01 = 40 mW.

In previous discussions, power consumption due to parasites associated with pure input pins is ignored and assumed to be negligible.

8 Design Considerations

8.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from Equation 3.

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad Eqn.\ 3$$

where:

T_A = Ambient temperature for the package (^oC)

$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^oC/W$)

P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which

Table 46. MC56F825x/MC56F824x Ordering Information

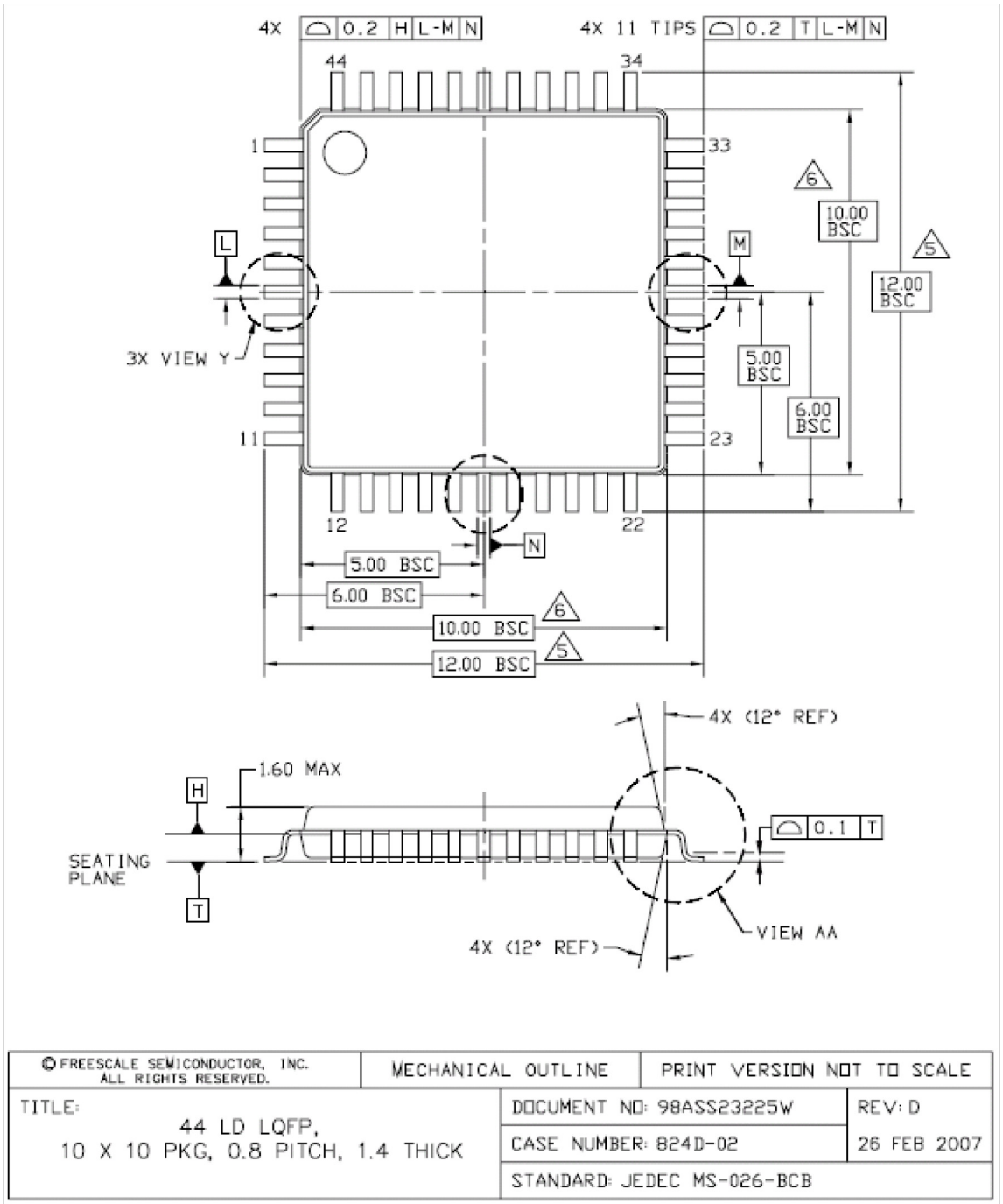
Device	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number[1]
MC56F8245	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	44	60	–40° to + 105° C –40° to + 125° C	MC56F8245VLD MC56F8245MLD
MC56F8246	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	–40° to + 105° C –40° to + 125° C	MC56F8246VLF MC56F8246MLF
MC56F8247	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	64	60	–40° to + 105° C –40° to + 125° C	MC56F8247VLH MC56F8247MLH
MC56F8255	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	44	60	–40° to + 105° C –40° to + 125° C	MC56F8255VLD MC56F8255MLD
MC56F8256	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	–40° to + 105° C –40° to + 125° C	MC56F8256VLF MC56F8256MLF
MC56F8257	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	64	60	–40° to + 105° C –40° to + 125° C	MC56F8257VLH MC56F8257MLH

[1] All of the packages are RoHS compliant.

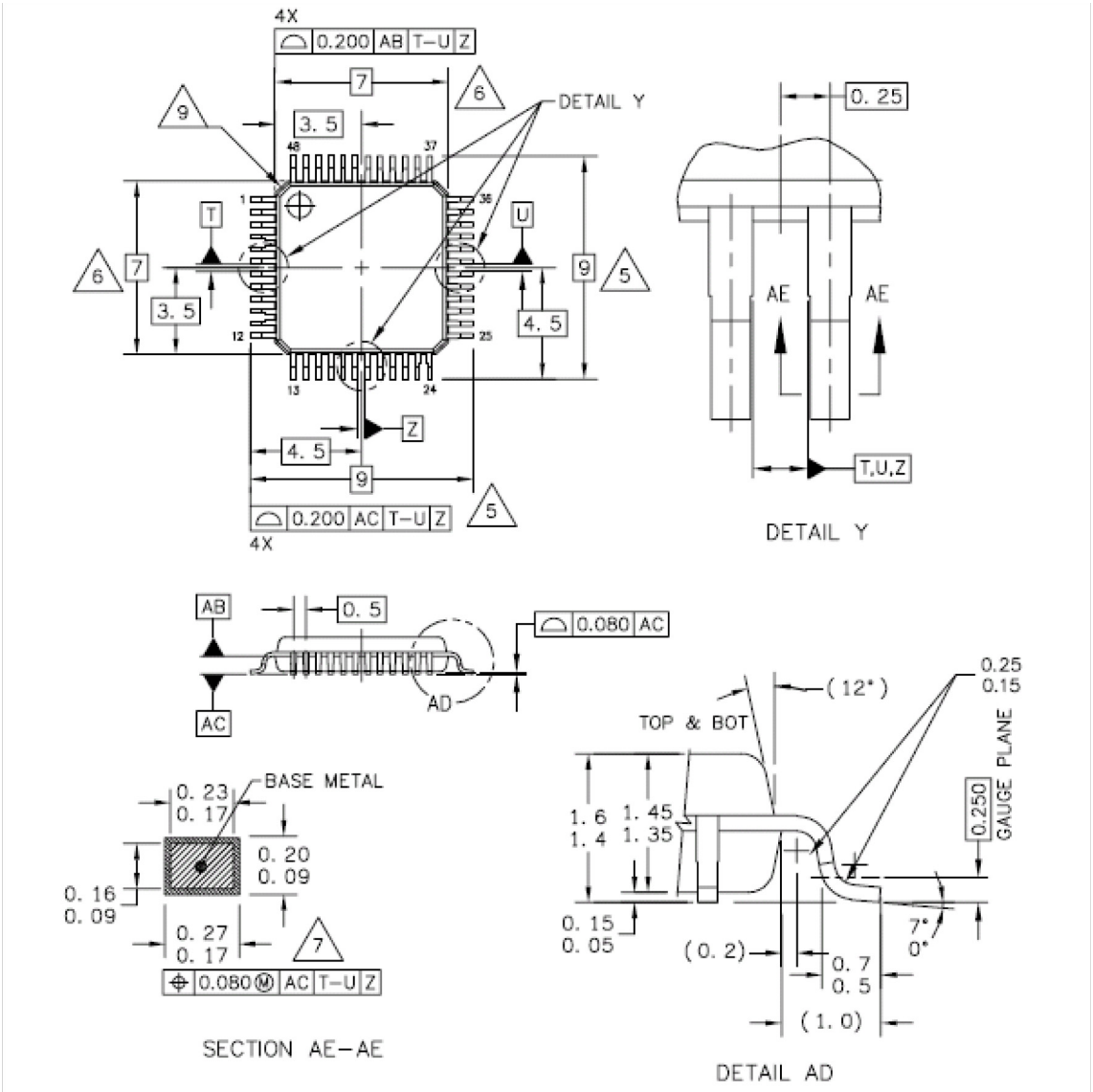
10 Package Mechanical Outline Drawings

To ensure you have the latest version of a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number (shown in the following sections for each package).

10.1 44-pin LQFP



10.2 48-pin LQFP



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TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	DOCUMENT NO: 98ASH00962A	REV: G
	CASE NUMBER: 932-03	14 APR 2005
	STANDARD: JEDEC MS-026-BBC	

11 Revision History

Table 47 summarizes changes to the document since the release of the previous version.

Table 47. Revision History

Revision	Date	Description
Rev. 3	2011-04-22	Table 46 on page 75: Added “M” orderable part numbers Table 24 on page 55: Updated data for run, wait, and stop modes, and added data for standby and powerdown modes Table 23 on page 54: Added minimum and maximum values for Internal Pull-Up Resistance Renumbered sections: Section 9 (was 8.3), Section 10 (was 9), Section 11 (was 10)