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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8257mlh

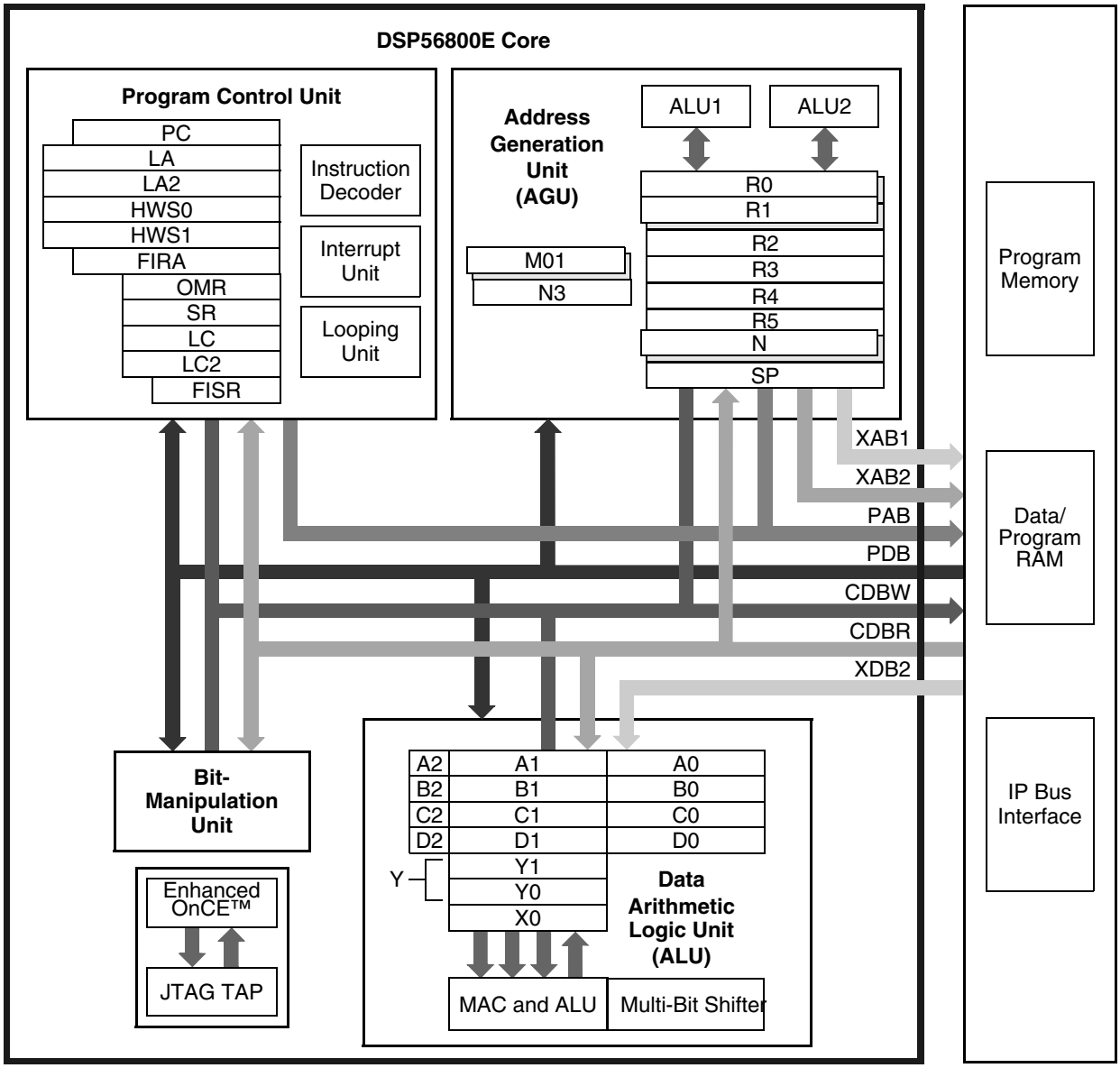


Figure 1. 56800E Core Block Diagram

Figure 2 shows the peripherals and control blocks connected to the IP bus bridge. Refer to the system integration module (SIM) section in the device's reference manual for information about which signals are multiplexed with those of other peripherals.

Table 4. MC56F825x/MC56F824x Pins (continued)

Pin Number			Pin Name	Peripherals												
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MS CAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
41	45	61	V_{SS}											V_{SS}		
42	46	62	TDO/*GPIOD1*	***GPIOD1***											**TDO**	
43	47	63	TMS/*GPIOD3*	***GIPOD3***											**TMS**	
44	48	64	TDI/*GPIOD0*	***GPIOD0***											**TDI**	

[1] The MSCAN module is not available on the MC56F824x devices.

3.2 Pin Assignment

Figure 3 shows the pin assignments of the 56F8245 and 56F8255's 44-pin low-profile quad flat pack (44LQFP). Figure 4 shows the pin assignments of the 56F8246 and 56F8256's 48-pin low-profile quad flat pack (48LQFP). Figure 5 shows the pin assignments of the 56F8247 and 56F8257's 64-pin low-profile quad flat pack (64LQFP).

NOTE

The CANRX and CANTX signals of the MSCAN module are not available on the MC56F824x devices.

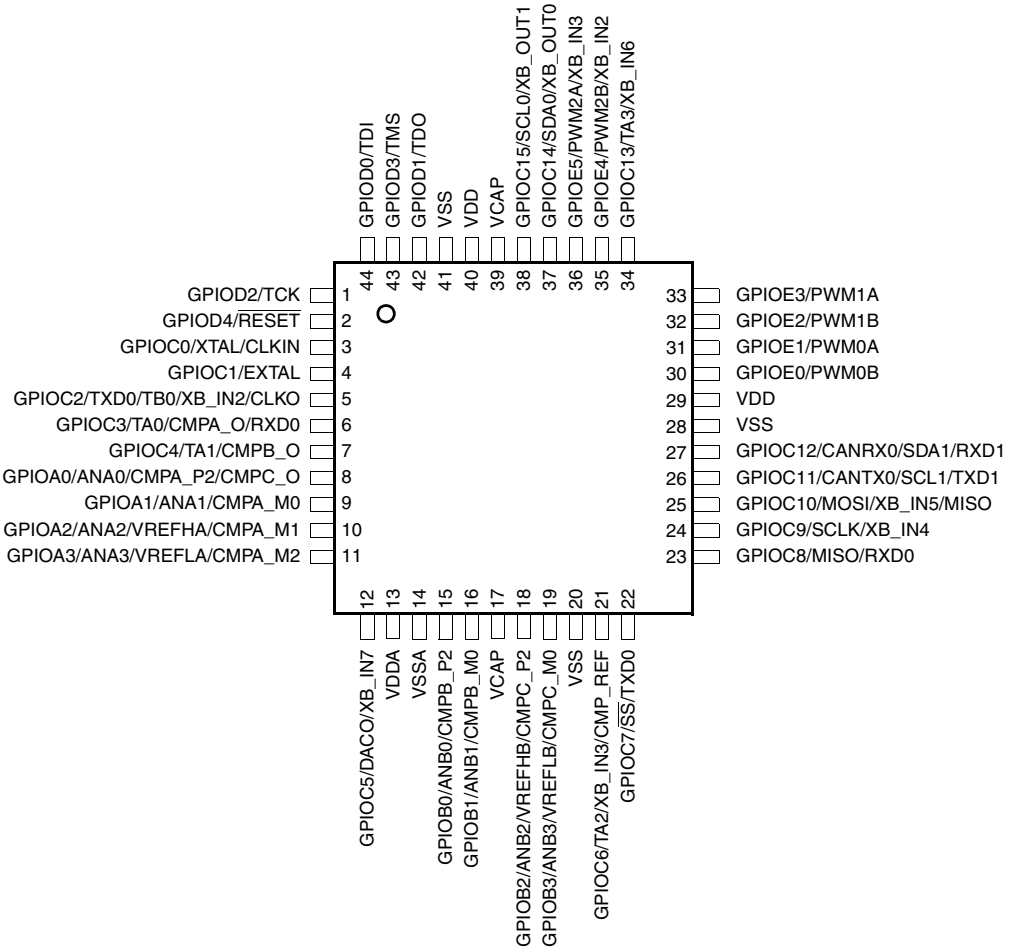


Figure 3. Top View: 56F8245 and 56F8255 44-Pin LQFP Package

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC2	5	5	5	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TXD0)				Output		TXD0 — The SCI0 transmit data output or transmit/receive in single wire operation.
(TB0)				Input/ Output		TB0 — Quad timer module B channel 0 input/output.
(XB_IN2)				Input		XB_IN2 — Crossbar module input 2
(CLKO)				Output		CLKO — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM. After reset, the default state is GPIOC2.
GPIOC3	6	6	7	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA0)				Input/ Output		TA0 — Quad timer module A channel 0 input/output.
(CMPA_O)				Output		CMPA_O— Analog comparator A output
(RXD0)				Input		RXD0 — The SCI0 receive data input. After reset, the default state is GPIOC3.
GPIOC4	7	7	8	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA1)				Input/ Output		TA1 — Quad timer module A channel 1input/output
(CMPB_O)				Output		CMPB_O — Analog comparator B output After reset, the default state is GPIOC4.
GPIOC5	12	13	18	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(DACO)				Analog Output		DACO — 12-bit Digital-to-Analog Controller output
(XB_IN7)				Input		XB_IN7 — Crossbar module input 7 After reset, the default state is GPIOC5.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC10	25	27	35	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(MOSI)				Input/ Output		MOSI — Master out/slave in. In master mode, this pin serves as the data output. In slave mode, this pin serves as the data input.
(XB_IN5)				Input		XB_IN5 — Crossbar module input 5
(MISO)				Input/ Output		MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. After reset, the default state is GPIOC10.
GPIOC11	26	29	37	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CANTX)				Open-drain Output		CANTX — CAN transmit data output (not available on 56F8245/46/47)
(SCL1)				Input/ Open-drain Output		SCL1 — I^2C1 serial clock
(TXD1)				Output		TXD1 — SCI1 transmit data output or transmit/receive in single wire operation After reset, the default state is GPIOC11.
GPIOC12	27	30	38	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CANRX)				Input		CANRX — CAN receive data input (not available on 56F8245/46/47)
(SDA1)				Input/ Open-drain Output		SDA1 — I^2C1 serial data line
(RXD1)				Input		RXD1 — SCI1 receive data input After reset, the default state is GPIOC12.
GPIOC13	34	37	49	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA3)				Input/ Output		TA3 — Quad timer module A channel 3input/output.
(XB_IN6)				Input		XB_IN6 — Crossbar module input 6 After reset, the default state is GPIOC13.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOF6 *(TB2)* *(PWM3X)*			58	Input/ Output Input/ Output Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. TB2 — Quad timer module B channel 2 input/output. PWM3X — Enhanced PWM submodule 3 output X or input capture X After reset, the default state is GPIOF6.
GPIOF7 *(TB3)*			59	Input/ Output Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. TB3 — Quad timer module B channel 3 input/output. After reset, the default state is GPIOF7.
GPIOF8 *(RXD0)* *(TB1)*			6	Input/ Output Input Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. RXD0 — The SCI0 receive data input. TB1 — Quad timer module B channel 1 input/output. After reset, the default state is GPIOF8.

1 If CLKIN is selected as the device's external clock input, both the GPS_C0 bit in GPS1 and the EXT_SEL bit in the OCCS oscillator control register (OSCTL) must be set. In this case, it is also recommended to power down the crystal oscillator.

4 Memory Maps

4.1 Introduction

The MC56F825x/MC56F824x device is based on the 56800E core. It uses a dual Harvard-style architecture with two independent memory spaces for data and program. On-chip RAM is shared by both data and program spaces; flash memory is used only in program space.

This section provides memory maps for:

- Program address space, including the interrupt vector table
- Data address space, including the EOnCE memory and peripheral memory maps

On-chip memory sizes for the device are summarized in Table 6. Flash memories' restrictions are identified in the "Use Restrictions" column of Table 6.

Table 6. Chip Memory Configurations

On-Chip Memory	56F8245 56F8246	56F8247	56F8255 56F8256 56F8357	Use Restrictions
Program Flash (PFLASH)	24K x 16 or 48 KB	24K x 16 or 48 KB	32K x 16 or 64 KB	Erase/program via flash interface unit and word writes to CDBW
Unified RAM (RAM)	3K x 16 or 6 KB	4K x 16 or 8 KB	4K x 16 or 8 KB	Usable by the program and data memory spaces

4.2 Program Map

The MC56F825x/MC56F824x series provide up to 64 KB on-chip flash memory. It primarily accesses through the program memory buses (PAB; PDB). PAB is used to select program memory addresses; instruction fetches are performed over PDB. Data can be read from and written to the program memory space through the primary data memory buses: CDBW for data write and CDBR for data read. Access time for accessing the program memory space over the data memory buses is longer than for accessing data memory space. The special MOVE instructions are provided to support these accesses. The benefit is that non-time-critical constants or tables can be stored and accessed in program memory.

The program memory map appears in Table 7, Table 8, and Table 9, depending on the device.

Table 7. Program Memory Map[1] for 56F8255/56/57 at Reset

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 8FFF P: 0x00 8000	On-chip RAM[2]: 8 KB
P: 0x00 7FFF P: 0x00 0000	• Internal program flash: 64 KB • Interrupt vector table locates from 0x00 0000 to 0x00 0085 • COP reset address = 0x00 0002 • Boot location = 0x00 0000

1 All addresses are 16-bit word addresses.

2 This RAM is shared with data space starting at address X: 0x00 0000. See Figure 6.

Table 8. Program Memory Map[1] for 56F82447 at Reset

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 8FFF P: 0x00 8000	On-chip RAM[2]: 8 KB
P: 0x00 7FFF P: 0x00 2000	• Internal program flash: 48 KB • Interrupt vector table locates from 0x00 2000 to 0x00 2085 • COP reset address = 0x00 2002 • Boot location = 0x00 2000
P: 0x00 2000 P: 0x00 0000	RESERVED

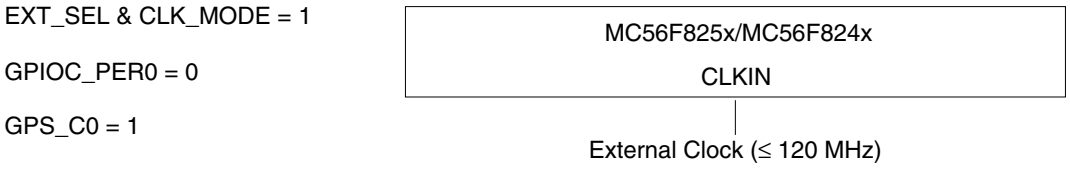


Figure 11. Connecting an External Clock Signal Using GPIO

5.5 Interrupt Controller

The MC56F825x/MC56F824x interrupt controller (INTC) module arbitrates the various interrupt requests (IRQs). When an interrupt of sufficient priority exists, the INTC signals to the 56800E core and provides the address to which to jump to service the interrupt.

The interrupt controller contains registers that allow each of the 66 interrupt sources to be set to one of three priority levels (excluding certain interrupt sources that have fixed priority) or to be disabled. Next, all interrupt requests of a given level are priority encoded to determine the lowest numeric value of the active interrupt requests for that level. Within a given priority level, the lowest vector number is the highest priority, and the highest vector number is the lowest priority.

Any two interrupt sources can be assigned to faster interrupts. Fast interrupts are described in the *DSP56800E Reference Manual*. The interrupt controller recognizes fast interrupts before the core does.

A fast interrupt is defined by:

1. Setting the priority of the interrupt as level 2 with the appropriate field in the Interrupt Priority Register (IPR) registers
2. Setting the Fast Interrupt Match (FIM*n*) register to the appropriate vector number
3. Setting the Fast Interrupt Vector Address Low (FIVAL*n)* and Fast Interrupt Vector Address High (FIVAH*n)* registers with the address of the code for the fast interrupt

When an interrupt occurs, its vector number is compared with the FIM0 and FIM1 register values. If a match occurs, and it is a level 2 interrupt, the INTC handles it as a Fast Interrupt. The INTC takes the vector address from the appropriate FIVAL*n* and FIVAH*n* registers, instead of generating an address that is an offset from the VBA.

The core then fetches the instruction from the indicated vector address instead of jumping to the vector table. If the instruction is not a JSR, the core starts its fast interrupt handling. Refer to section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for details.

Table 48 on page 85 provides the MC56F825x/MC56F824x's interrupt table contents and interrupt priority structure.

5.6 System Integration Module (SIM)

The SIM module consists of the glue logic that ties together the system-on-a-chip. It controls distribution of resets and clocks and provides a number of control features, including pin muxing control, inter-module connection control (such as connecting comparator output to eFlexPWM fault input), individual peripheral enabling/disabling, clock rate control for quad timers and SCIs, enabling peripheral operation in stop mode, and port configuration overwrite protection. For more information, refer to the device's reference manual.

The SIM is responsible for the following functions:

- Chip reset sequencing
- Core and peripheral clock control and distribution
- Stop/wait mode control
- System status control
- Registers containing the JTAG ID of the chip
- Controls for programmable peripheral and GPIO connections

- Peripheral clocks for Quad Timers and SCIs with a high-speed (2x) option
- Power-saving clock gating for peripherals
- Controls for enabling/disabling functions of large regulator standby mode with write protection capability
- Allowing selected peripherals to run in stop mode to generate stop recovery interrupts
- Controls for programmable peripheral and GPIO connections
- Software chip reset
- I/O short address base location control
- Peripheral protection control to provide runaway code protection for safety-critical applications
- Controls for output of internal clock sources to CLKO pin
- Four general-purpose software control registers that are reset only at power-on
- Peripheral stop mode clocking control

5.7 Inter-Module Connections

The operations between on-chip peripherals can be synchronized or cascaded through internal module connections to support particular applications. Examples include synchronization between ADC sampling and PWM waveform generation for a power conversion application, and synchronization between timer pulse outputs and DAC waveform generation for a printer application. The user can program the internal Crossbar Switch or Comparator input multiplexes to connect one on-chip peripheral's outputs to other peripherals' inputs.

5.7.1 Comparator Connections

The MC56F825x/MC56F824x includes three high-speed comparators. Each comparator input has a 4-to-1 input mux, allowing it to sample a variety of analog sources. Some of these inputs share package pins with the on-chip ADCs; see Table 5 on page 18.

Each comparator is paired with a dedicated, programmable, 5-bit on-chip voltage reference DAC (VREF_DAC). Optionally, an on-chip 12-bit DAC can be internally fed to each comparator's positive input 1 (CMPn_P1) or negative input 3 (CMPn_M3). In addition, all three comparators' positive input 3 (CMPn_P3) can be connected together to package pin CMP_REF. Other inputs can be routed to package pins when the corresponding pin is configured for peripheral mode in the GPIO module.

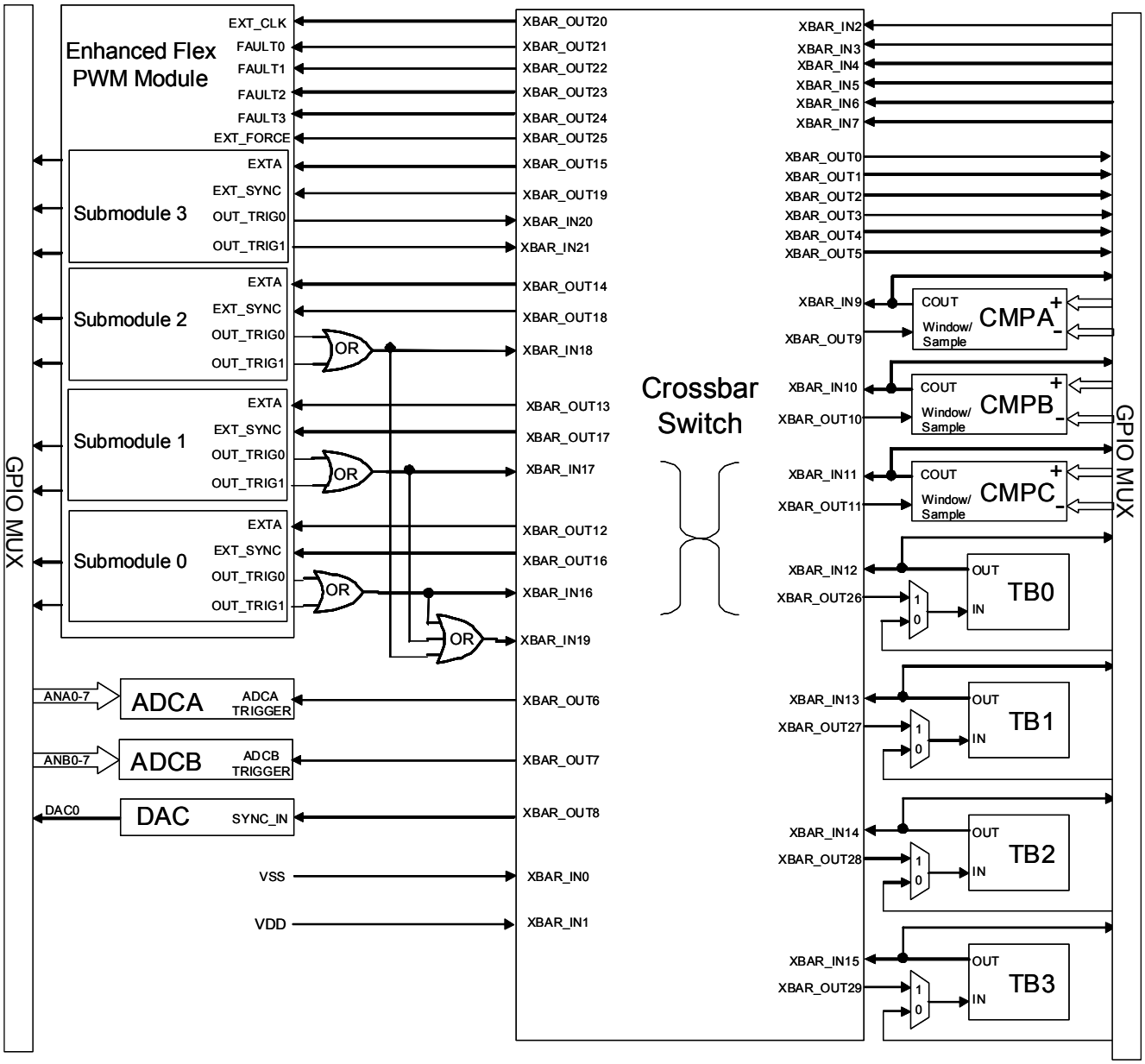


Figure 13. Crossbar Switch Connections

5.7.2.1 Crossbar Switch Inputs

Table 15 lists the signal assignments of Crossbar Switch inputs.

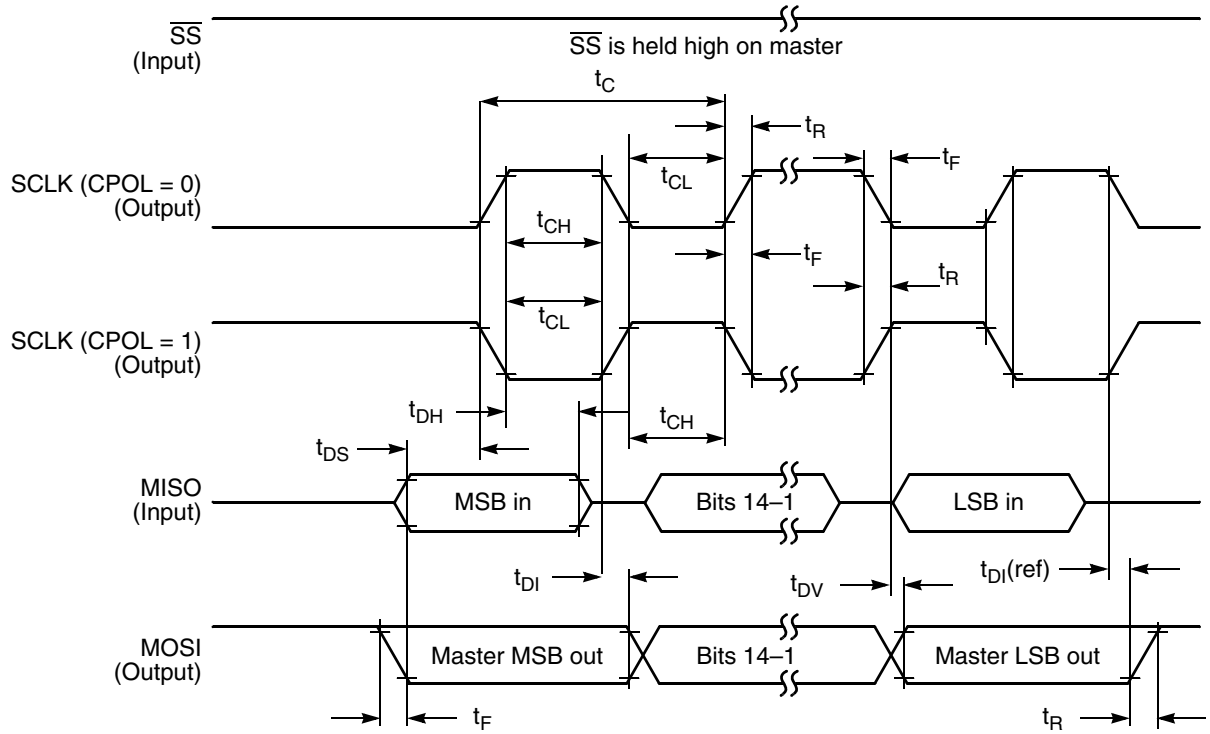


Figure 20. SPI Master Timing (CPHA = 0)

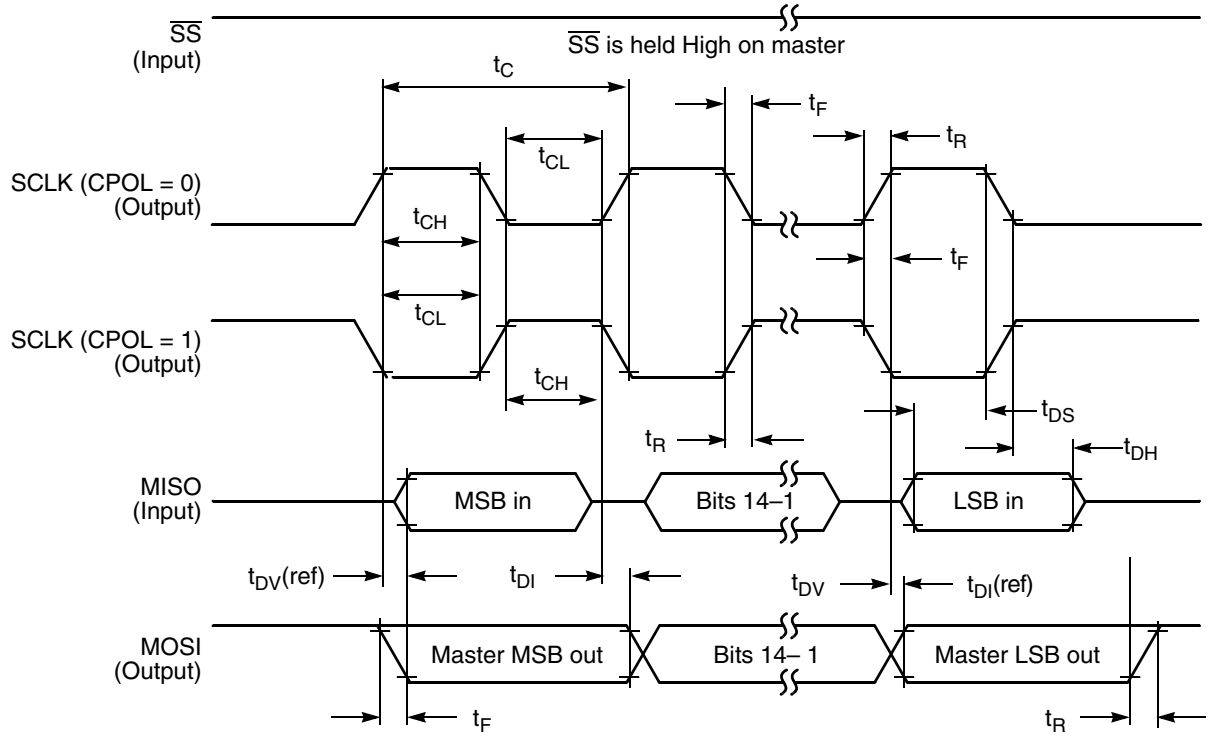


Figure 21. SPI Master Timing (CPHA = 1)

Table 41. ADC Parameters[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Input impedance	X_{IN}	—	See Figure 31	—	Ohms
AC Specifications[9] (gain of 1x, 2x, 4x and $f_{ADC} \leq$ 10 MHz)[4]					
Signal-to-noise ratio	SNR	—	59		dB
Total Harmonic Distortion	THD	—	64		dB
Spurious Free Dynamic Range	SFDR	—	65		dB
Signal-to-noise plus distortion	SINAD	—	59		dB
Effective Number Of Bits	ENOB	—	9.5		Bits

1 All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2 Includes power-up of ADC and V_{REF}
3 ADC clock cycles
4 Speed register setting must be 00 for ADC clock ≤ 5 MHz, 01 for 5 MHz < ADC clock ≤ 12 MHz, and 10 for ADC clock > 12 MHz
5 INL and DNL measured from V_{IN} = V_{REFL} to V_{IN} = V_{REFH}
6 LSB = Least Significant Bit = 0.806 mV at x1 gain
7 Pin groups are detailed following Table 17.
8 The current that can be injected or sourced from an unselected ADC signal input without affecting the performance of the ADC
9 ADC PGA gain is x1

7.25.1 Equivalent Circuit for ADC Inputs

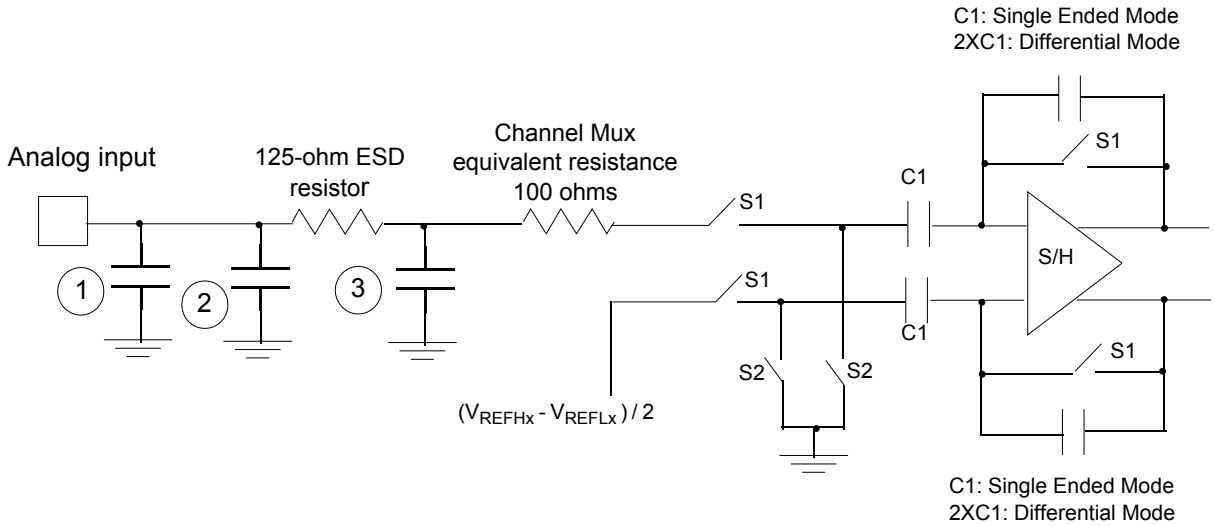
Figure 31 illustrates the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases and operate at the ADC clock frequency. Equivalent input impedance, when the input is selected, is as follows:

$$(2 \times k / ADCClockRate \times C_{gain}) + 100 \text{ ohms} + 125 \text{ ohms} \qquad \textit{Eqn. 1}$$

where k =

- 1 for first sample
- 6 for subsequent samples

and C_{gain} is as described in note 4 below.

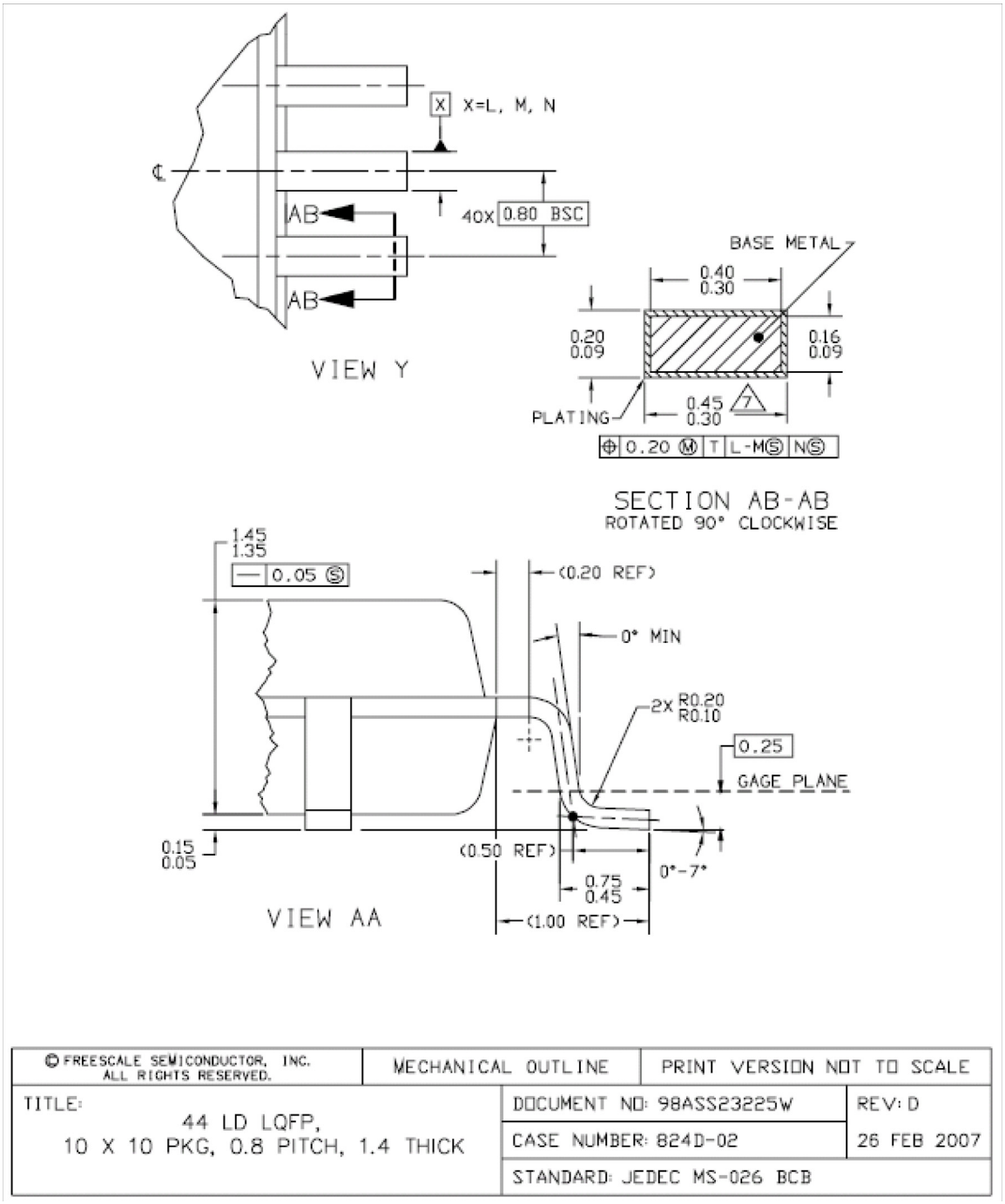


1. Parasitic capacitance due to package, pin-to-pin, and pin-to-package base coupling: 1.8 pF

Table 46. MC56F825x/MC56F824x Ordering Information

Device	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number[1]
MC56F8245	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	44	60	–40° to + 105° C –40° to + 125° C	MC56F8245VLD MC56F8245MLD
MC56F8246	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	–40° to + 105° C –40° to + 125° C	MC56F8246VLF MC56F8246MLF
MC56F8247	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	64	60	–40° to + 105° C –40° to + 125° C	MC56F8247VLH MC56F8247MLH
MC56F8255	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	44	60	–40° to + 105° C –40° to + 125° C	MC56F8255VLD MC56F8255MLD
MC56F8256	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	–40° to + 105° C –40° to + 125° C	MC56F8256VLF MC56F8256MLF
MC56F8257	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	64	60	–40° to + 105° C –40° to + 125° C	MC56F8257VLH MC56F8257MLH

[1] All of the packages are RoHS compliant.



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TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23225W	REV: D
	CASE NUMBER: 824D-02	26 FEB 2007
	STANDARD: JEDEC MS-026 BCB	

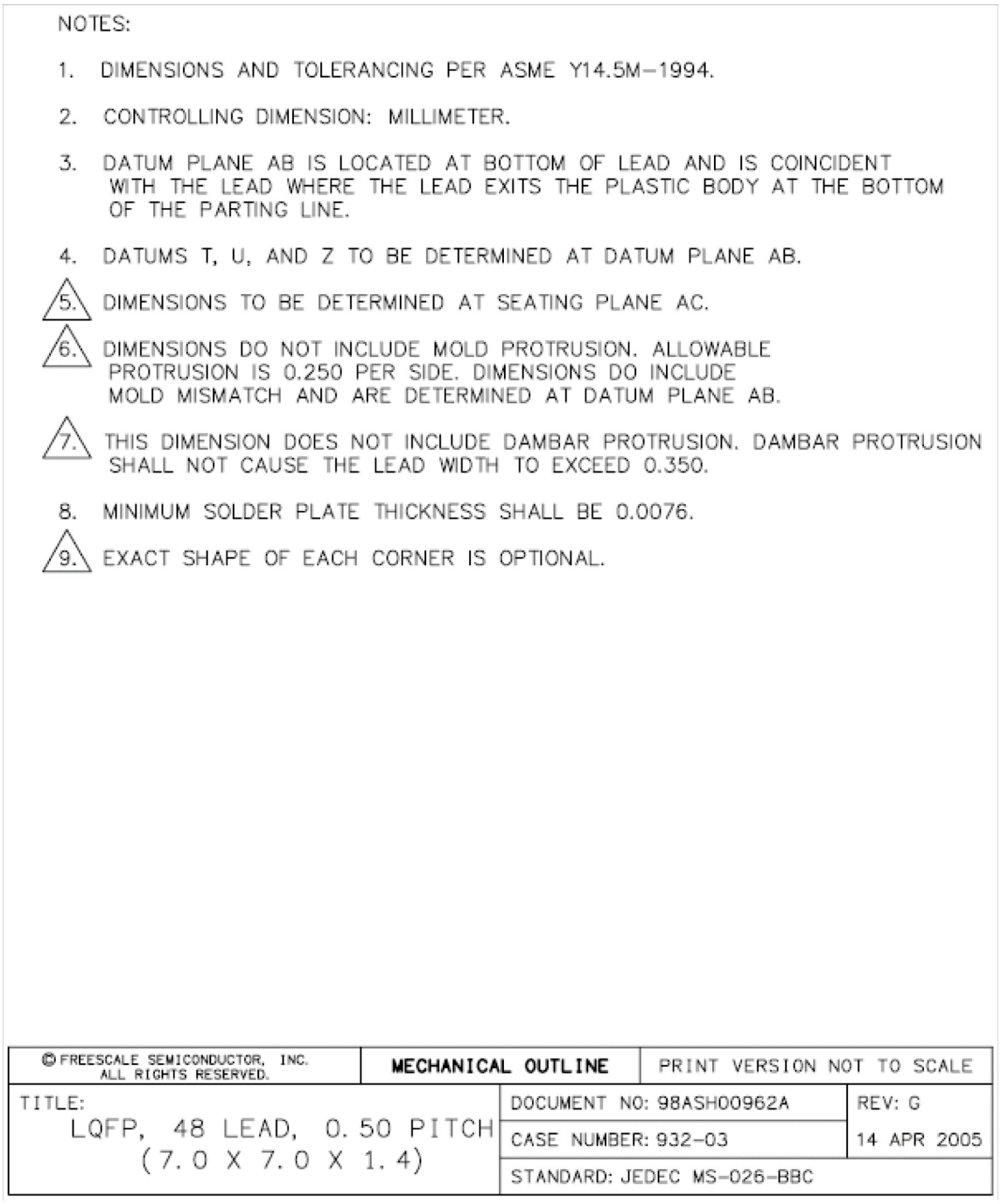
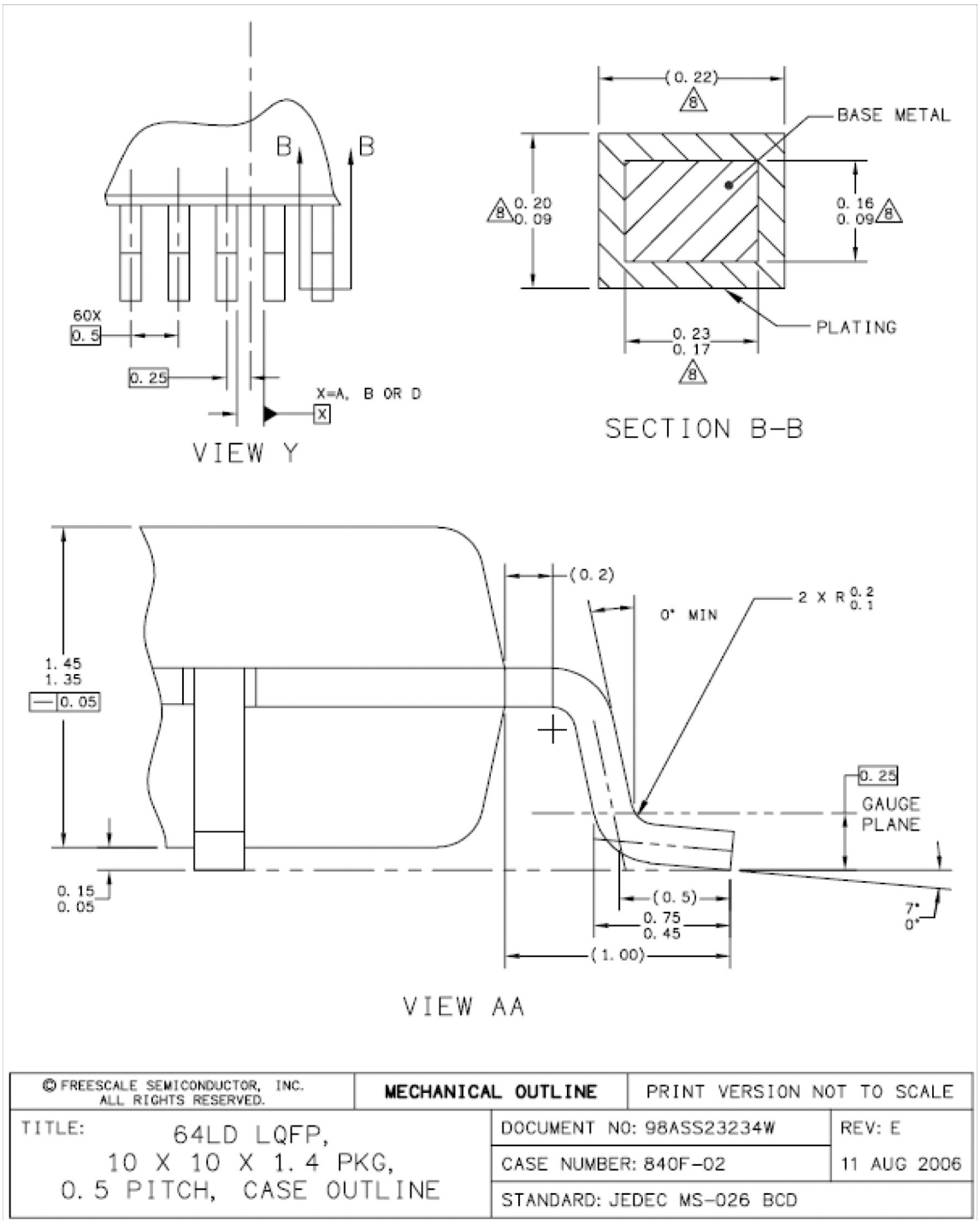


Figure 33. 56F8246 and 56F8256 48-Pin LQFP Mechanical Information



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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: E
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	

11 Revision History

Table 47 summarizes changes to the document since the release of the previous version.

Table 47. Revision History

Revision	Date	Description
Rev. 3	2011-04-22	Table 46 on page 75: Added “M” orderable part numbers Table 24 on page 55: Updated data for run, wait, and stop modes, and added data for standby and powerdown modes Table 23 on page 54: Added minimum and maximum values for Internal Pull-Up Resistance Renumbered sections: Section 9 (was 8.3), Section 10 (was 9), Section 11 (was 10)

Table 48. Interrupt Vector Table Contents[1] (continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
CAN	25	0 - 2	P:0x32	CAN Error Interrupt
CAN	26	0 - 2	P:0x34	CAN Wake-Up Interrupt
QSCI1	27	0 - 2	P:0x36	QSCI1 Receiver Overrun/Errors
QSCI1	28	0 - 2	P:0x38	QSCI1 Receiver Full
QSCI1	29	0 - 2	P:0x3A	QSCI1 Transmitter Idle
QSCI1	30	0 - 2	P:0x3C	QSCI1 Transmitter Empty
QSCI0	31	0 - 2	P:0x3E	QSCI0 Receiver Overrun/Errors
QSCI0	32	0 - 2	P:0x40	QSCI0 Receiver Full
QSCI0	33	0 - 2	P:0x42	QSCI0 Transmitter Idle
QSCI0	34	0 - 2	P:0x44	QSCI0 Transmitter Empty
QSPI	35	0 - 2	P:0x46	SPI Transmitter Empty
QSPI	36	0 - 2	P:0x48	SPI Receiver Full
I^2C1	37	0 - 2	P:0x4A	I^2C1 Interrupt
I^2C0	38	0 -2	P:0x4C	I^2C0 Interrupt
TMRA3	39	0 -2	P:0x4E	Quad Timer A, Channel 3 Interrupt
TMRA2	40	0 -2	P:0x50	Quad Timer A, Channel 2 Interrupt
TMRA1	41	0 -2	P:0x52	Quad Timer A, Channel 1 Interrupt
TMRA0	42	0 -2	P:0x54	Quad Timer A, Channel 0 Interrupt
eFlexPWM	43	0 -2	P:0x56	PWM Fault
eFlexPWM	44	0 -2	P:0x58	PWM Reload Error
eFlexPWM	45	0 -2	P:0x5A	PWM Sub-Module 3 Reload
eFlexPWM	46	0 -2	P:0x5C	PWM Sub-Module 3 input capture
eFlexPWM	47	0 -2	P:0x5E	PWM Sub-Module 3 Compare
eFlexPWM	48	0 -2	P:0x60	PWM Sub-Module 2 Reload
eFlexPWM	49	0 -2	P:0x62	PWM Sub-Module 2 Compare
eFlexPWM	50	0 -2	P:0x64	PWM Sub-Module 1 Reload
eFlexPWM	51	0 -2	P:0x66	PWM Sub-Module 1 Compare
eFlexPWM	52	0 -2	P:0x68	PWM Sub-Module 0 Reload
eFlexPWM	53	0 -2	P:0x6A	PWM Sub-Module 0Compare
FM	54	0 -2	P:0x6C	Flash Memory Access Error
FM	55	0 -2	P:0x6E	Flash Memory Programming Command Complete
FM	56	0 -2	P:0x70	Flash Memory Buffer Empty Request
CMPC	57	0 - 2	P:0x72	Comparator C Rising/Falling Flag
CMPB	58	0 - 2	P:0x74	Comparator B Rising/Falling Flag

Table 48. Interrupt Vector Table Contents[1] (continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
CMPA	59	0 - 2	P:0x76	Comparator A Rising/Falling Flag
GPIOF	60	0 - 2	P:0x78	GPIOF Interrupt
GPIOE	61	0 - 2	P:0x7A	GPIOE Interrupt
GPIOD	62	0 - 2	P:0x7C	GPIOD Interrupt
GPIOC	63	0 - 2	P:0x7E	GPIOC Interrupt
GPIOB	64	0 - 2	P:0x80	GPIOB Interrupt
GPIOA	65	0 - 2	P:0x82	GPIOA Interrupt
SWILP	66	-1	P:0x84	SW Interrupt Low Priority

1 Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.

2 If the VBA is set to the reset value, the first two locations of the vector table overlay the chip reset addresses because the reset address would match the base of this vector table.

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USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
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Tempe, Arizona 85284
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Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
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+44 1296 380 456 (English)
+46 8 52200080 (English)
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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China
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