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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8257vlh

  - Maximum ADC clock frequency: up to 10 MHz
    - Single conversion time of 8.5 ADC clock cycles (8.5 x 100 ns = 850 ns)
    - Additional conversion time of 6-ADC clock cycles (6 x 100 ns = 600 ns)
  - Sequential, parallel, and independent scan mode
  - First 8 samples have Offset, Limit and Zero-crossing calculation supported
  - ADC conversions can be synchronized by eFlexPWM and timer modules via internal crossbar module
  - Support for simultaneous and software triggering conversions
  - Support for multi-triggering mode with a programmable number of conversions on each trigger
- Inter-module Crossbar Switch (XBAR)
  - Programmable internal module connections among the eFlexPWM, ADCs, Quad Timers, 12-bit DAC, HSCMPs, and package pins
  - User-defined input/output pins for PWM fault inputs, Timer input/output, ADC triggers, and Comparator outputs
- Three analog comparators (CMPs)
  - Selectable input source includes external pins, internal DACs
  - Programmable output polarity
  - Output can drive timer input, eFlexPWM fault input, eFlexPWM source, external pin output, and trigger ADCs
  - Output falling and rising edge detection able to generate interrupts
  - 32-tap programmable voltage reference per comparator
- One 12-bit digital-to-analog converter (12-bit DAC)
  - 12-bit resolution
  - Power down mode
  - Output can be routed to internal comparator, or off chip
- Two four-channel 16-bit multi-purpose timer (TMR) modules
  - Four independent 16-bit counter/timers with cascading capability per module
  - Up to 120 MHz operating clock
  - Each timer has capture and compare and quadrature decoder capability
  - Up to 12 operating modes
  - Four external inputs and two external outputs
- Two queued serial communication interface (QSCI) modules with LIN slave functionality
  - Up to 120 MHz operating clock
  - Four-byte-deep FIFOs available on both transmit and receive buffers
  - Full-duplex or single-wire operation
  - Programmable 8- or 9-bit data format
  - 13-bit integer and 3-bit fractional baud rate selection
  - Two receiver wakeup methods:
    - Idle line
    - Address mark
  - 1/16 bit-time noise detection
  - Support LIN slave operation
- One queued serial peripheral interface (QSPI) module
  - Full-duplex operation
  - Four-word deep FIFOs available on both transmit and receive buffers
  - Master and slave modes
  - Programmable length transactions (2 to 16 bits)
  - Programmable transmit and receive shift order (MSB as first or last bit transmitted)

  - Maximum slave module frequency = module clock frequency/2
  - 13-bit baud rate divider for low speed communication
- Two inter-integrated circuit (I^2C) ports
  - Operation at up to 100 kbps
  - Support for master and slave operation
  - Support for 10-bit address mode and broadcasting mode
  - Support for SMBus, Version 2
- One Freescale Scalable Controller Area Network (MSCAN) module
  - Fully compliant with CAN protocol Version 2.0 A/B
  - Support for standard and extended data frames
  - Support for data rate up to 1 Mbit/s
  - Five receive buffers and three transmit buffers
- Computer operating properly (COP) watchdog timer capable of selecting different clock sources
  - Programmable prescaler and timeout period
  - Programmable wait, stop, and partial powerdown mode operation
  - Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
  - Choice of clock sources from four sources in support of EN60730 and IEC61508:
    - On-chip relaxation oscillator
    - External crystal oscillator/external clock source
    - System clock (IP bus to 60 MHz)
- Power supervisor (PS)
  - On-chip linear regulator for digital and analog circuitry to lower cost and reduce noise
  - Integrated low voltage detection to generate warning interrupt if VDD is below low voltage detection (LVI) threshold
  - Integrated power-on reset (POR)
    - Reliable reset process during power-on procedure
    - POR is released after VDD passes low voltage detection (LVI) threshold
  - Integrated brown-out reset
  - Run, wait, and stop modes
- Phase lock loop (PLL) providing a high-speed clock to the core and peripherals
  - 2x system clock provided to Quad Timers and SCIs
  - Loss of lock interrupt
  - Loss of reference clock interrupt
- Clock sources
  - On-chip relaxation oscillator with two user selectable frequencies: 400 kHz for low speed mode, 8 MHz for normal operation
  - External clock: crystal oscillator, ceramic resonator, and external clock source
- Cyclic Redundancy Check (CRC) Generator
  - Hardware CRC generator circuit using 16-bit shift register
  - CRC16-CCITT compliancy with x16 + x12 + x5 + 1 polynomial
  - Error detection for all single, double, odd, and most multi-bit errors
  - Programmable initial seed value
  - High-speed hardware CRC calculation
  - Optional feature to transpose input data and CRC result via transpose register, required on applications where bytes are in LSb (Least Significant bit) format.

2.4 Product Documentation

The documents listed in Table 2 are required for a complete description and proper design with the MC56F825x/MC56F824x. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at http://www.freescale.com.

Table 2. MC56F825x/MC56F824x Device Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F825x Reference Manual	Detailed description of peripherals of the MC56F825x/MC56F824x devices	MC56F825XRM
MC56F824x/5x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F800x family of devices	TBD
MC56F825x Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F825X
MC56F825x Errata	Detailed description of any chip issues that might be present	MC56F825XE

3 Signal/Connection Descriptions

3.1 Introduction

The input and output signals of the MC56F825x/MC56F824x are organized into functional groups, as detailed in Table 3.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins in 44 LQFP	Number of Pins in 48 LQFP	Number of Pins in 64 LQFP
Power inputs (V_{DD}, V_{DDA}, V_{CAP})	5	5	6
Ground (V_{SS}, V_{SSA})	4	4	4
Reset[1]	1	1	1
Enhanced Flex Pulse Width Modulator (eFlexPWM) ports[1]	6	6	9
Queued Serial Peripheral Interface (SPI) ports[1]	4	4	4
Queued Serial Communications Interface 0&1 (QSCI0 & QSCI1) ports[1]	6	6	9
Inter-Integrated Circuit Interface 0&1 (I^2C0 & I^2C0) ports[1]	4	4	6
Analog-to-Digital Converter (ADC) inputs[1]	8	10	16
High Speed Analog Comparator inputs/outputs[1]	11	12	15
12-bit Digital-to-Analog Converter (DAC_12B) output	1	1	1
Quad Timer Module (TMRA & TMRB) ports[1]	5	5	8
Freescale's Scalable Controller-Area-Network (MSCAN)[1, 2]	2	2	2
Inter-Module Cross Bar package inputs/outputs[1]	10	12	17
Clock[1]	3	4	4
JTAG/Enhanced On-Chip Emulation (EOnCE)[1]	4	4	4

1 Pins may be shared with other peripherals. See Table 4.

2 Exclude MC56F824x.

Table 4 summarizes all device pins. Each table row describes the signal or signals present on a pin, sorted by pin number. Peripheral pins in bold identify reset state.

Table 4. MC56F825x/MC56F824x Pins

Pin Number			Pin Name	Peripherals													
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MS CAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
1	1	1	TCK/*GPIOD2*	*GPIOD2*											**TCK**	
2	2	2	$\overline{\text{RESET}}$ / *GPIOD4*	*GPIOD4*												**$\overline{\text{RESET}}$**
3	3	3	GPIOC0/*XTAL/CLKIN*	**GPIOC0**												*XTAL/ CLKIN*
4	4	4	GPIOC1/*EXTAL*	**GPIOC1**												*EXTAL*
5	5	5	GPIOC2/*TXD0/TB0/XB_IN2/ CLKO*	**GPIOC2**		*TXD0*				*XB_IN2*		*TB0*				*CLKO*
		6	GPIOF8/*RXD0/TB1*	**GPIOF8**		*RXD0*						*TB1*				
6	6	7	GPIOC3/*TA0/CMPA_O/RXD0*	**GPIOC3**		*RXD0*					*CMPA_O*	*TA0*				
7	7	8	GPIOC4/*TA1/CMPB_O*	**GPIOC4**							*CMPB_O*	*TA1*				
		9	GPIOA7/*ANA7*	**GPIOA7**					*ANA7*							
		10	GPIOA6/*ANA6*	**GPIOA6**					*ANA6*							
		11	GPIOA5/*ANA5*	**GPIOA5**					*ANA5*							
	8	12	GPIOA4/*ANA4*	**GPIOA4**					*ANA4*							
8	9	13	GPIOA0/*ANA0& CMPA_P2/CMPC_O*	**GPIOA0**					*ANA0*		*CMPA_P2/ CMPC_O*					
9	10	14	GPIOA1/ *ANA1&CMPA_M0*	**GPIOA1**					*ANA1*		*CMPA_M0*					
10	11	15	GPIOA2/*ANA2&VREFHA& CMPA_M1*	**GPIOA2**					*ANA2& VREFHA*		*CMPA_M1*					
11	12	16	GPIOA3/*ANA3&VREFLA& CMPA_M2*	**GPIOA3**					*ANA3& VREFLA*		*CMPA_M2*					
		17	GPIOB7/*ANB7&CMPB_M2*	**GPIOB7**					*ANB7*		*CMPB_M2*					
12	13	18	GPIOC5/*DACO/XB_IN7*	**GPIOC5**						*XB_IN7*						*DACO*
		19	GPIOB6/*ANB6&CMPB_M1*	**GPIOB6**					*ANB6*		*CMPB_M1*					
		20	GPIOB5/*ANB5&CMPC_M2*	**GPIOB5**					*ANB5*		*CMPC_M2*					
	14	21	GPIOB4/*ANB4&CMPC_M1*	**GPIOB4**					*ANB4*		*CMPC_M1*					
13	15	22	V_{DDA}											**V_{DDA}**		
14	16	23	V_{SSA}											**V_{SSA}**		
15	17	24	GPIOB0/ *ANB0&CMPB_P2*	**GPIOB0**					*ANB0*		*CMPB_P2*					
16	18	25	GPIOB1/ *ANB1&CMPB_M0*	**GPIOB1**					*ANB1*		*CMPB_M0*					
17	19	26	V_{CAP}											**V_{CAP}**		
18	20	27	GPIOB2/ *ANB2&VREFHB&CMPC_P2*	**GPIOB2**					*ANB2& VREFHB*		*CMPC_P2*					

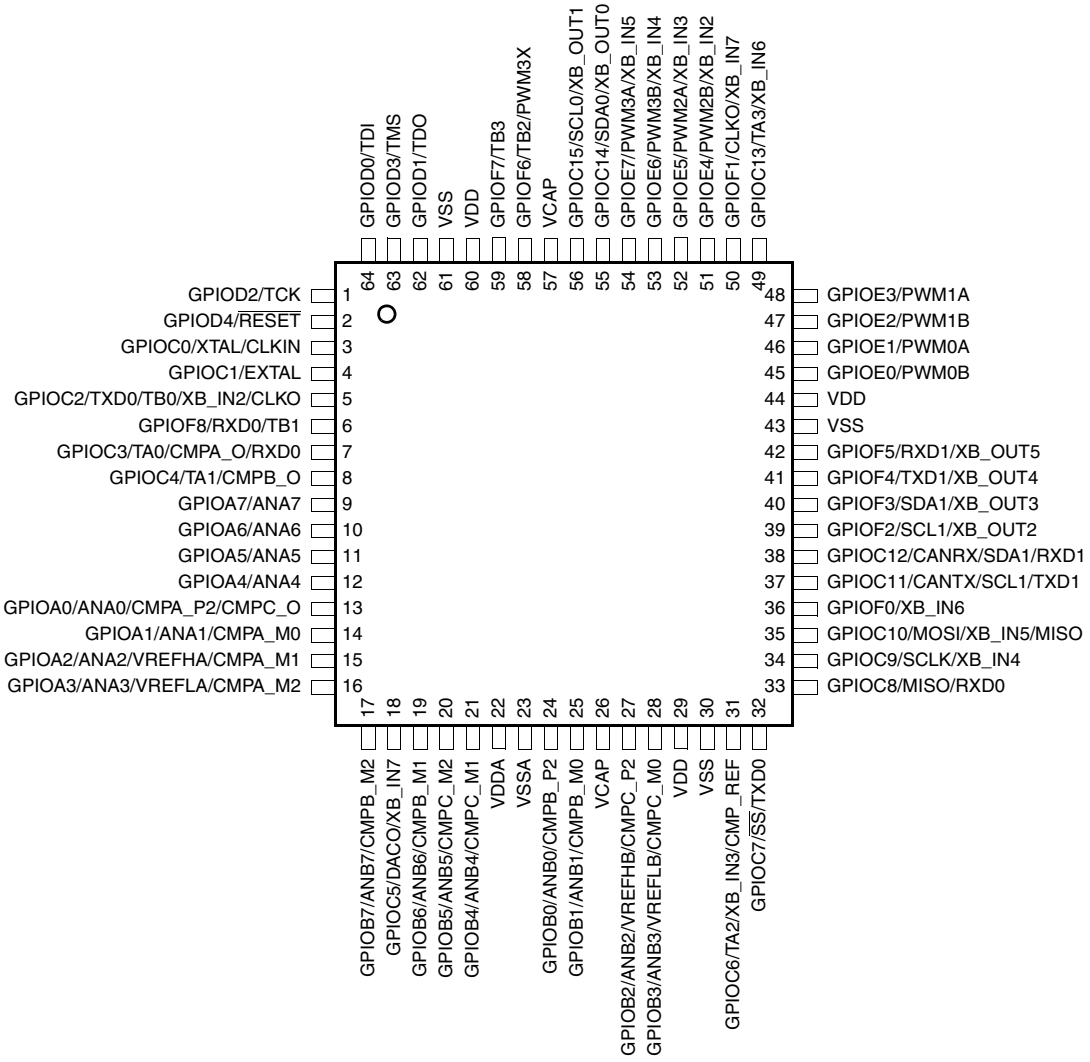


Figure 5. Top View: 56F8247 and 56F8257 64-Pin LQFP Package

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
TMS *(GPIOD3)*	43	47	63	input Input/ Output	Input, internal pullup enabled	Test Mode Select Input — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TMS **Note**: Always tie the TMS pin to VDD through a 2.2K resistor if need to keep on-board debug capability. Otherwise directly tie to VDD
$\overline{\text{RESET}}$ *(GPIOD4)*	2	2	2	Input Input/ Open-drain Output	Input, internal pullup enabled	Reset — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. Port D GPIO — This GPIO pin can be individually programmed as an input or open-drain output pin.If $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can be reset only via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOA0 *(ANA0& CMPA_P2)* *(CMPC_O)*	8	9	13	Input/ Output Input Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA0 and CMPA_P2 — Analog input to channel 0 of ADCA and positive input 2 of analog comparator A. CMPC_O— Analog comparator C output When used as an analog input, the signal goes to the ANA0 and CMPA_P2. After reset, the default state is GPIOA0.
GPIOA1 *(ANA1& CMPA_M0)*	9	10	14	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA1 and CMPA_M0 — Analog input to channel 1of ADCA and negative input 0 of analog comparator A. When used as an analog input, the signal goes to the ANA1 and CMPA_M0. After reset, the default state is GPIOA1.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC2	5	5	5	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TXD0)				Output		TXD0 — The SCI0 transmit data output or transmit/receive in single wire operation.
(TB0)				Input/ Output		TB0 — Quad timer module B channel 0 input/output.
(XB_IN2)				Input		XB_IN2 — Crossbar module input 2
(CLKO)				Output		CLKO — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM. After reset, the default state is GPIOC2.
GPIOC3	6	6	7	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA0)				Input/ Output		TA0 — Quad timer module A channel 0 input/output.
(CMPA_O)				Output		CMPA_O— Analog comparator A output
(RXD0)				Input		RXD0 — The SCI0 receive data input. After reset, the default state is GPIOC3.
GPIOC4	7	7	8	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA1)				Input/ Output		TA1 — Quad timer module A channel 1input/output
(CMPB_O)				Output		CMPB_O — Analog comparator B output After reset, the default state is GPIOC4.
GPIOC5	12	13	18	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(DACO)				Analog Output		DACO — 12-bit Digital-to-Analog Controller output
(XB_IN7)				Input		XB_IN7 — Crossbar module input 7 After reset, the default state is GPIOC5.

[2] This RAM is shared with program space starting at P: 0x00 8000. See Figure 6 and Figure 7.

On-chip RAM is also mapped into program space starting at P: 0x00 8000. This mapping eases online reprogramming of on-chip flash.

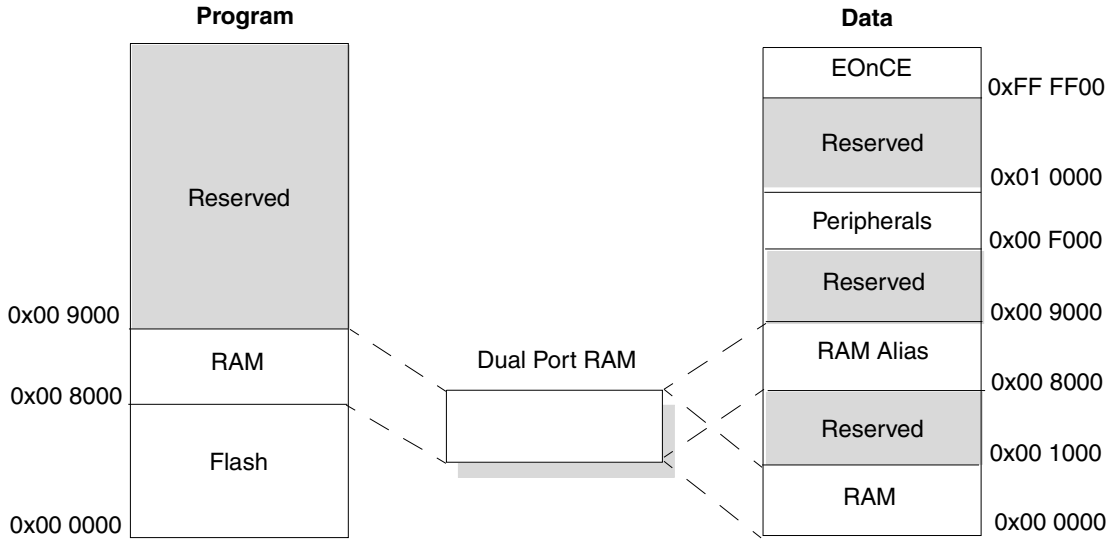


Figure 6. 56F8255/56/57 Dual Port RAM Map

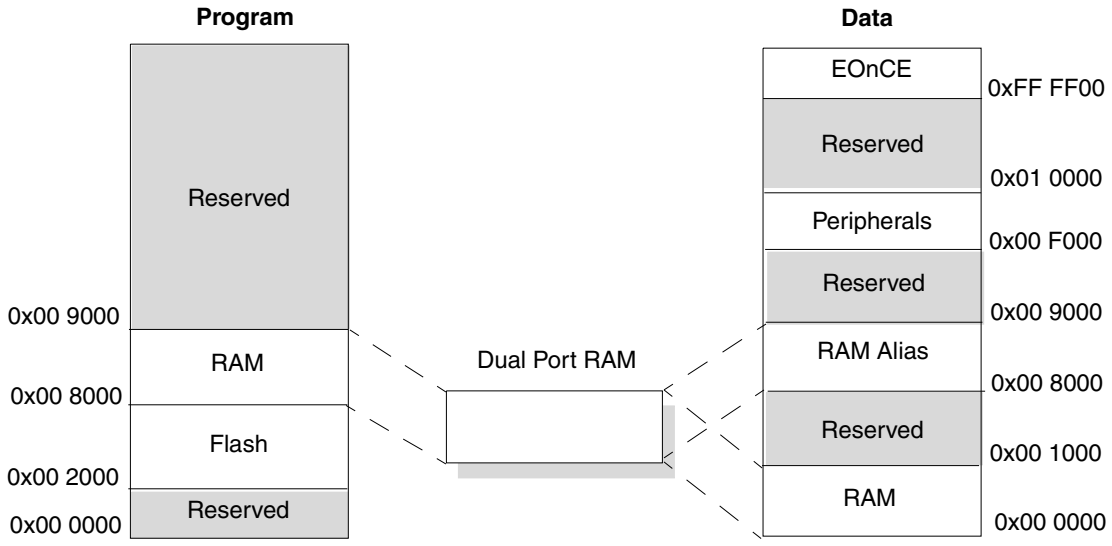


Figure 7. 56F8247 Dual Port RAM Map

Table 15. Crossbar Input Signal Assignments

XBAR_INn	Input from	Function
XBAR_IN0	Logic Zero	V_{SS}
XBAR_IN1	Logic One	V_{DD}
XBAR_IN2	XB_IN2	Package pin
XBAR_IN3	XB_IN3	Package pin
XBAR_IN4	XB_IN4	Package pin
XBAR_IN5	XB_IN5	Package pin
XBAR_IN6	XB_IN6	Package pin
XBAR_IN7	XB_IN7	Package pin
XBAR_IN8	Unused	
XBAR_IN9	CMPA_OUT	Comparator A Output
XBAR_IN10	CMPB_OUT	Comparator B Output
XBAR_IN11	CMPC_OUT	Comparator C Output
XBAR_IN12	TB0	Quad Timer B0 Output
XBAR_IN13	TB1	Quad Timer B1 Output
XBAR_IN14	TB2	Quad Timer B2 Output
XBAR_IN15	TB3	Quad Timer B3 Output
XBAR_IN16	PWM0_TRIG_COMB	eFlexPWM submodule 0: PWM0_OUT_TRIG0 or PWM0_OUT_TRIG1
XBAR_IN17	PWM1_TRIG_COMB	eFlexPWM submodule 1: PWM1_OUT_TRIG0 or PWM1_OUT_TRIG1
XBAR_IN18	PWM2_TRIG_COMB	eFlexPWM submodule 2: PWM2_OUT_TRIG0 or PWM2_OUT_TRIG1
XBAR_IN19	PWM[012]_TRIG_COMB	eFlexPWM submodule 0, 1, or 2; PWM0_TRIG_COMB or PWM1_TRIG_COMB or PWM2_TRIG_COMB
XBAR_IN20	PWM3_TRIG0	eFlexPWM submodule 3: PWM3_OUT_TRIG0
XBAR_IN21	PWM3_TRIG1	eFlexPWM submodule 3: PWM3_OUT_TRIG1

5.7.2.2 Crossbar Switch Outputs

Table 16 lists the signal assignments of Crossbar Switch outputs.

Table 16. Crossbar Output Signal Assignments

XBAR_OUTn	Output to	Function
XBAR_OUT0	XB_OUT0	Package pin
XBAR_OUT1	XB_OUT1	Package pin
XBAR_OUT2	XB_OUT2	Package pin
XBAR_OUT3	XB_OUT3	Package pin
XBAR_OUT4	XB_OUT4	Package pin
XBAR_OUT5	XB_OUT5	Package pin
XBAR_OUT6	ADCA	ADCA Trigger

- If the ADC conversion result in SAMPLE1 is less than the value programmed into the low limit register 1, PWM1_EXTB is driven high.

State of PWM2_EXTB:

- If the ADC conversion result in SAMPLE2 is greater than the value programmed into the high limit register 2, PWM2_EXTB is driven low.
- If the ADC conversion result in SAMPLE2 is less than the value programmed into the low limit register 2, PWM2_EXTB is driven high.

5.8 Joint Test Action Group (JTAG)/Enhanced On-Chip Emulator (EOnCE)

The 56800E family includes extensive integrated support for application software development and real-time debugging. Two modules, the Enhanced On-Chip Emulation (EOnCE) module and the core test access port (TAP, commonly called the JTAG port), work together to provide these capabilities. Both are accessed through a common 4-pin JTAG/EOnCE interface. These modules allow you to insert the MC56F825x/MC56F824x into a target system while retaining debug control. This capability is especially important for devices without an external bus, because it eliminates the need for a costly cable to bring out the footprint of the chip, as is required by a traditional emulator system.

The 56800E's EOnCE module is a Freescale-designed module for developing and debugging application software used with the chip. This module allows non-intrusive interaction with the CPU and is accessible through the pins of the JTAG interface or by software program control of the 56800E core. Among the many features of the EOnCE module is support, in real-time program execution, for data communication between the controller and the host software development and debug systems. Other features allow for hardware breakpoints, the monitoring and tracking of program execution, and the ability to examine and modify the contents of registers, memory, and on-chip peripherals, all in a special debug environment. No user-accessible resources must be sacrificed to perform debugging operations.

The 56800E's JTAG port provides an interface for the EOnCE module to the JTAG pins. The Joint Test Action Group (JTAG) boundary scan is an IEEE 1149.1 standard methodology enabling access to test features using a test access port (TAP). A JTAG boundary scan consists of a TAP controller and boundary scan registers. Contact your Freescale sales representative or authorized distributor for device-specific BSDL information.

NOTE

In normal operation, an external pullup on the TMS pin is highly recommend to place the JTAG state machine in reset state (if this pin is not configured as GPIO).

6 Security Features

The MC56F825x/MC56F824x offers security features intended to prevent unauthorized users from gaining access to and reading the contents of the flash memory (FM) array. The MC56F825x/MC56F824x's flash memory security consists of several hardware interlocks.

After flash memory security is set, the application software can allow an authorized user to access on-chip memory by including a user-defined software subroutine that reads and transfers the contents of internal memory via peripherals. This application software can communicate over a serial port, for example, to validate the authenticity of the requested access and then to grant it until the next device reset. The system designer must use discretion when deciding whether to support this type of "back door" access technique.

6.1 Operation with Security Enabled

After you have programmed flash with the application code, or as part of programming the flash with the application code, you can secure the MC56F825x/MC56F824x by programming the values 1 and 0 into bits 1 and 0, respectively, of program memory location 0x00_7FF7. The CodeWarrior IDE menu flash lock command can also accomplish this task. The nonvolatile security

6.2.4 Flash Lockout Recovery without Mass Erase

6.2.4.1 Without Presenting Back Door Access Keys to the Flash Unit

A user can unsecure a secured device by programming the word 0x0000 into program flash location 0x00 7FF7. After completing the programming, the JTAG TAP controller and the device must be reset to return to normal unsecured operation.

The user is responsible for directing the device to invoke the flash programming subroutine to reprogram the word 0x0000 into program flash location 0x00 7FF7. You can do so, for example, by toggling a specific pin or downloading a user-defined key through serial interfaces.

NOTE

Flash contents can be programmed only from ones to zeroes.

6.2.4.2 Presenting Back Door Access Key to the Flash Unit

The user can temporarily bypass security through a "back door" access scheme, using a four-word key to temporarily unlock the flash. "Back door" access requires support from the embedded software. This software would typically permit an external user to enter the four-word code through one of the communications interfaces and then use it to attempt the unlock sequence. If the input matches the four-word code stored at location 0x00 7FFC–0x00 7FFF in the flash memory, the device immediately becomes unsecured (at runtime) and internal memory is accessible via the JTAG/EOnCE port. Refer to the device's reference manual for details. The key must be entered in four consecutive accesses to the flash, so this routine should be designed to run in RAM.

6.3 Product Analysis

To analyze a product's failures in the field, the recommended method of unsecuring a secured device appears in Section 6.2.4.2, "Presenting Back Door Access Key to the Flash Unit." The customer must supply technical-support details about the protocol to access the subroutines in flash memory. An alternative method for performing analysis on a secured device is to mass-erase and reprogram the flash memory with the original code, but also to modify or not program the security word.

7 Specifications

7.1 General Characteristics

The MC56F825x/MC56F824x is fabricated in high-density, low-power, low-leakage CMOS process with 5 V–tolerant, TTL-compatible digital inputs. The term *5 V–tolerant* refers to the capability of an I/O pin, built on a 3.3 V–compatible process technology, to withstand a voltage up to 5.5 V without damaging the device. Many systems have a mixture of devices designed for 3.3 V and 5 V power supplies. In such systems, a bus may carry both 3.3 V–compatible and 5 V–compatible I/O voltage levels (a standard 3.3 V I/O is designed to receive a maximum voltage of 3.3 V ± 10% during normal operation without causing damage). This 5 V–tolerant capability therefore combines the power savings of 3.3 V I/O levels with the ability to receive 5 V levels without damage.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

7.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed.

CAUTION

Stress beyond the limits specified in Table 17 may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this section apply over the ambient temperature range of –40 ºC to +105 ºC over the following supply ranges: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0$ V to 3.6 V, CL ≤ 50 pF, $f_{OP} = 60$ MHz.

For functional operating conditions, refer to the remaining tables in the section.

Table 17. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply Voltage Range	V_{DD}		- 0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		- 0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		- 0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		- 0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Groups 1, 2	- 0.3	6.0	V
Oscillator Voltage Range	V_{OSC}	Pin Group 4	- 0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	- 0.3	4.0	V
Input clamp current, per pin ($V_{IN} < 0$)[1]	V_{IC}		—	-20.0	mA
Output clamp current, per pin ($V_O < 0$)[1]	V_{OC}		—	-20.0	mA
Output Voltage Range (Normal Push-Pull mode)	V_{OUT}	Pin Group 1	- 0.3	4.0	V
Output Voltage Range (Open Drain mode)	V_{OUTOD}	Pin Group 2	- 0.3	6.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	- 0.3	4.0	V
Ambient Temperature Industrial	T_A		- 40	105	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		- 55	150	°C

[1] Continuous clamp current per pin is –2.0 mA

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC and Comparator Analog Inputs

Pin Group 4: XTAL, EXTAL

Pin Group 5: DAC analog output

Table 23. DC Electrical Characteristics at Recommended Operating Conditions

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High (a) pull-up enabled or disabled	I_{IH}	Pin Groups 1, 2	—	0	+/- 2.5	µA	V_{IN} = 2.4 V to 5.5 V
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low[1] pull-up enabled pull-up disabled	I_{IL}	Pin Groups 1, 2	-15 —	-30 0	-60 +/- 2.5	µA	V_{IN} = 0 V
Internal Pull-Up Resistance	$R_{Pull-Up}$		60	110	220	kΩ	—
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0 V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0 V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40 mV	—	Typically V_{DDA} – 40 mV	V	—
Output Current [1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 2.5	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	—	0.35	—	V	—
Input Capacitance	C_{IN}		—	10	—	pF	—
Output Capacitance	C_{OUT}		—	10	—	pF	—

[1] See Figure 14.

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK
Pin Group 2: $\overline{\text{RESET}}$, GPIOA7
Pin Group 3: ADC and Comparator Analog Inputs
Pin Group 4: XTAL, EXTAL
Pin Group 5: DAC Analog Output

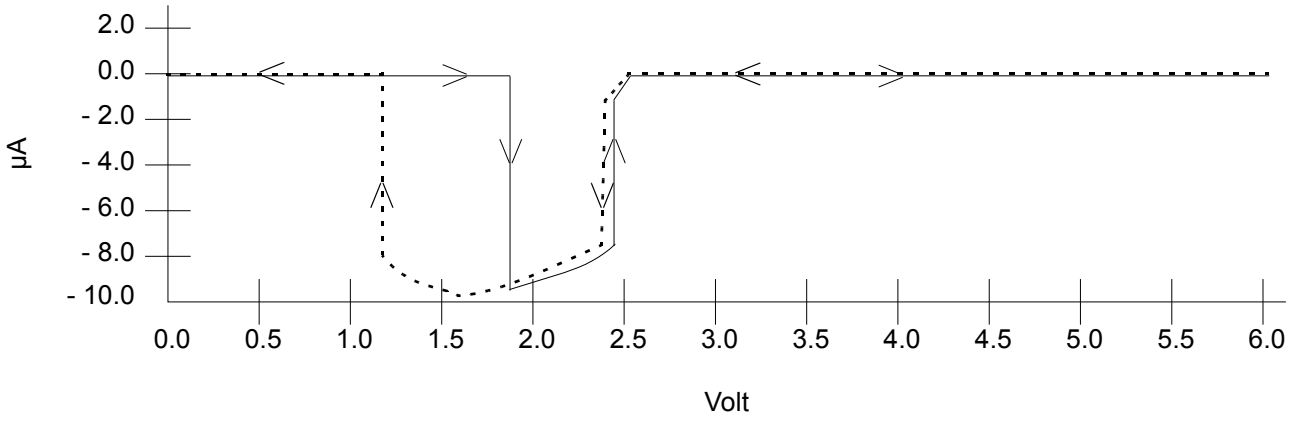


Figure 14. I_{IN}/I_{OZ} versus V_{IN} (Typical; Pull-Up Disabled)

7.17 Reset, Stop, Wait, Mode Select, and Interrupt Timing

NOTE

All address and data buses described here are internal.

Table 33. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration [3]	t_{RA}	4T	—	ns	—
Minimum GPIO pin Assertion for Interrupt	t_{IW}	2T	—	ns	Figure 19
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	$96T_{OSC}$ + 64T	$97T_{OSC}$ + 65T	ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	—	6T	ns	—

1 In the formulas, T = system clock cycle and T_{osc} = oscillator clock cycle. For an operating frequency of 32 MHz, T = 31.25 ns. At 4 MHz (used coming out of reset and stop modes), T = 250 ns.

2 Parameters listed are guaranteed by design.

3 This minimum number guarantees that a reliable reset occurs.

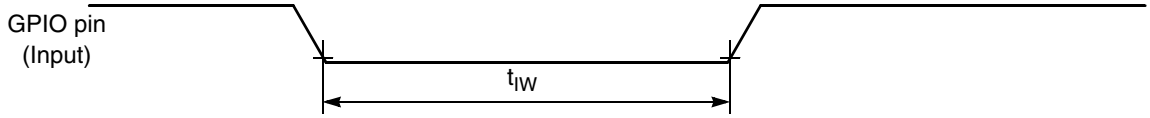


Figure 19. GPIO Interrupt Timing (Negative Edge-Sensitive)

7.18 Queued Serial Peripheral Interface (SPI) Timing

Table 34. SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	Refer to
Cycle time Master Slave	t_C	 125 62.5	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Enable lead time Master Slave	t_{ELD}	 — 31	 — —	 ns ns	Figure 23
Enable lag time Master Slave	t_{ELG}	 — 125	 — —	 ns ns	Figure 23
Clock (SCK) high time Master Slave	t_{CH}	 50 31	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Clock (SCK) low time Master Slave	t_{CL}	 50 31	 — —	 ns ns	Figure 23

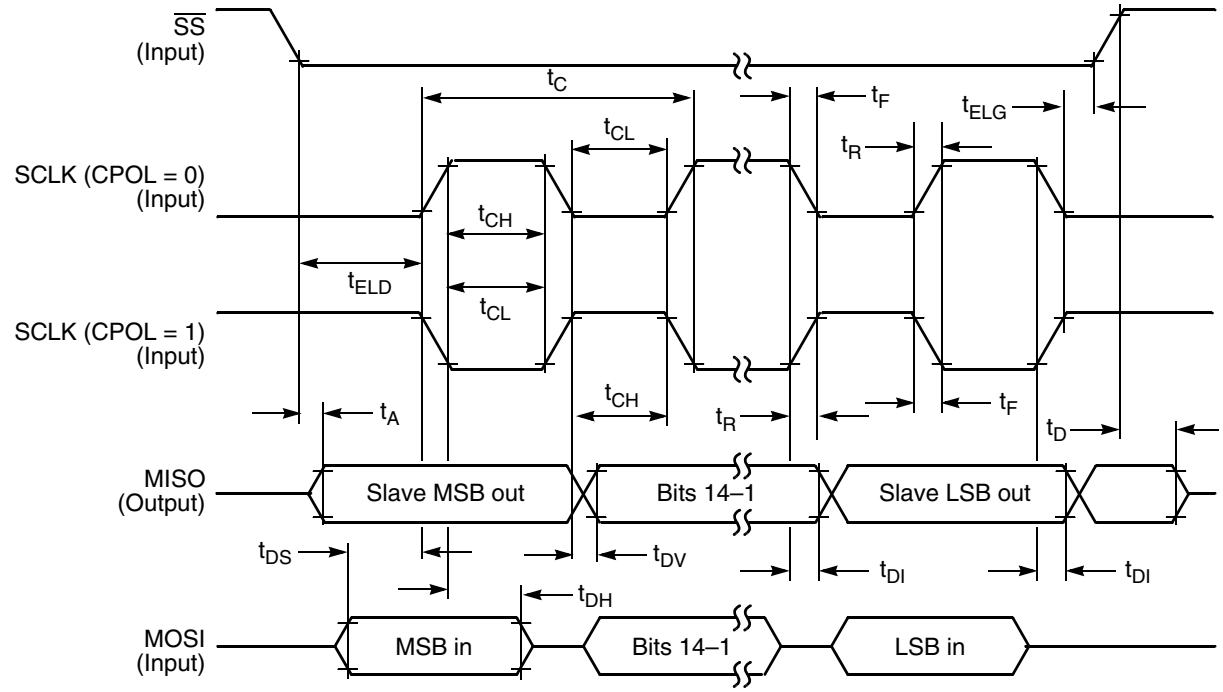


Figure 22. SPI Slave Timing (CPHA = 0)

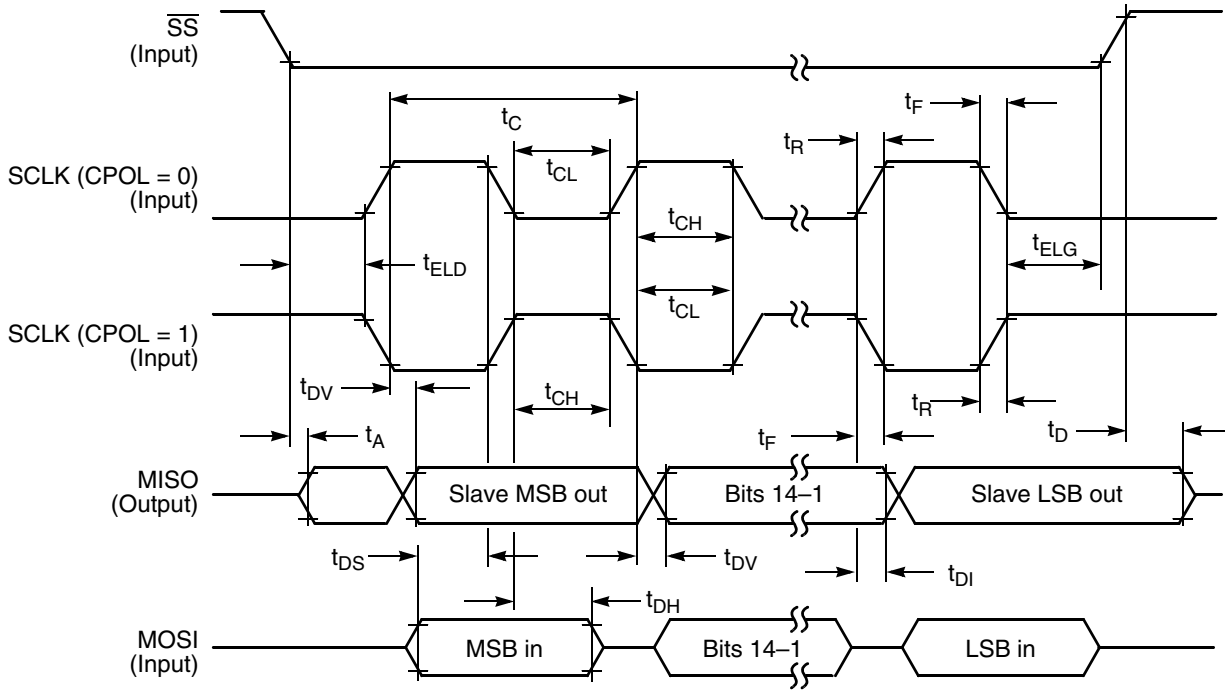


Figure 23. SPI Slave Timing (CPHA = 1)

7.24 COP Specifications

Table 40. COP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Oscillator output frequency	LPFosc	500	1000	1500	Hz
Oscillator current consumption in partial power down mode	IDD		TBD		nA

7.25 Analog-to-Digital Converter (ADC) Parameters

Table 41. ADC Parameters[1]

Parameter	Symbol	Min	Typ	Max	Unit
DC Specifications					
Resolution	R_{ES}	12	—	12	Bits
ADC internal clock	f_{ADIC}	0.1	—	15	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC and VREF power-up time[2](from power down mode)	t_{ADPU}	—	13	—	t_{AIC} cycles[3]
VREF power-up time (from low power mode)	t_{REFPU}	—	6	—	t_{AIC} cycles[3]
ADC RUN current (Speed Control setting) at 100 kHz ADC clock (Standby Mode) at ADC clock ≤ 5 MHz (00) at 5 MHz < ADC clock ≤ 12 MHz (01) at 12 MHz < ADC clock ≤ 15 MHz (10)	I_{ADRUN}	 — — — —	 0.6 10 17 27	 — — — —	mA
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Accuracy (DC or absolute) (gain of 1x, 2x, 4x and f_{ADC} ≤ 10 MHz) (all data in single-ended mode)[4]					
Integral non-linearity[5] (Full input signal range)	INL	—	+/- 3	+/- 6	LSB[6]
Differential non-linearity[5]	DNL	—	+/- 0.6	+/- 1	LSB[5]
Monotonicity	GUARANTEED				
Offset Voltage Internal Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Offset Voltage External Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Gain Error (transfer gain)	E_{GAIN}	—	0.995 to 1.005	1.01 to 0.99	—
ADC Inputs[7] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0.001	—	µA
Input injection current[8], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See Figure 31	—	pF

Table 41. ADC Parameters[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Input impedance	X_{IN}	—	See Figure 31	—	Ohms
AC Specifications[9] (gain of 1x, 2x, 4x and $f_{ADC} \leq$ 10 MHz)[4]					
Signal-to-noise ratio	SNR	—	59		dB
Total Harmonic Distortion	THD	—	64		dB
Spurious Free Dynamic Range	SFDR	—	65		dB
Signal-to-noise plus distortion	SINAD	—	59		dB
Effective Number Of Bits	ENOB	—	9.5		Bits

1 All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2 Includes power-up of ADC and V_{REF}
3 ADC clock cycles
4 Speed register setting must be 00 for ADC clock ≤ 5 MHz, 01 for 5 MHz < ADC clock ≤ 12 MHz, and 10 for ADC clock > 12 MHz
5 INL and DNL measured from V_{IN} = V_{REFL} to V_{IN} = V_{REFH}
6 LSB = Least Significant Bit = 0.806 mV at x1 gain
7 Pin groups are detailed following Table 17.
8 The current that can be injected or sourced from an unselected ADC signal input without affecting the performance of the ADC
9 ADC PGA gain is x1

7.25.1 Equivalent Circuit for ADC Inputs

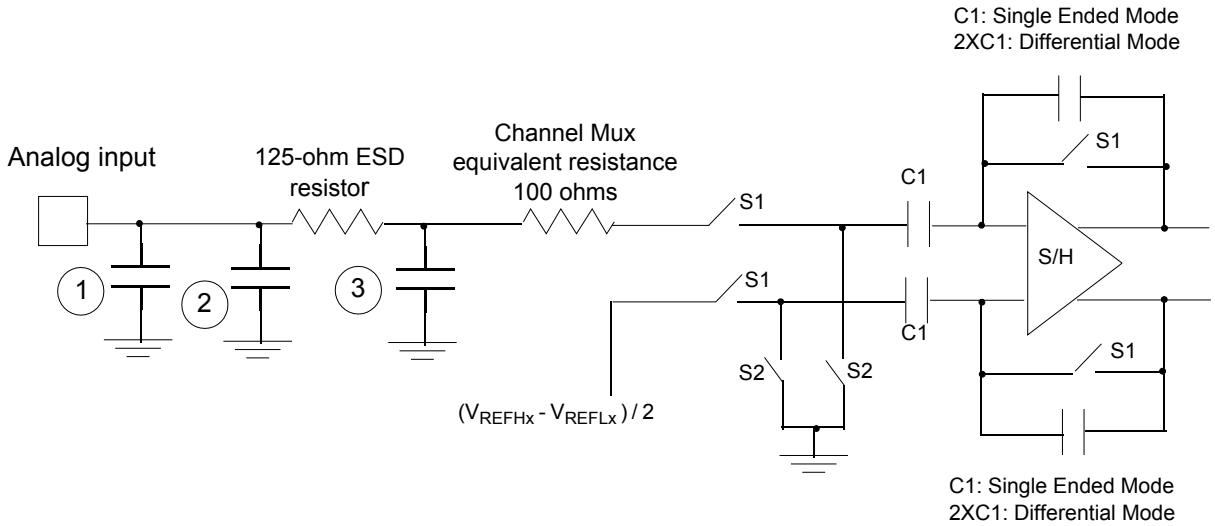
Figure 31 illustrates the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases and operate at the ADC clock frequency. Equivalent input impedance, when the input is selected, is as follows:

$$(2 \times k / ADCClockRate \times C_{gain}) + 100 \text{ ohms} + 125 \text{ ohms} \qquad \textit{Eqn. 1}$$

where k =

- 1 for first sample
- 6 for subsequent samples

and C_{gain} is as described in note 4 below.



1. Parasitic capacitance due to package, pin-to-pin, and pin-to-package base coupling: 1.8 pF

1 No guaranteed specification within 5% of V_{DDA} or V_{SSA}
2 LSB = 0.806 mV

7.27 5-Bit Digital-to-Analog Converter (DAC) Parameters

Table 43. 5-Bit DAC Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Reference Inputs	Vin	V_{DDA}	—	V_{DDA}	mV
Setup Delay	t_{PRGST}	TBD	TBD	TBD	ns
Step size	V_{STEP}	3Vin/128	Vin/32	5Vin/128	V
Output Range	V_{DACOUT}	Vin/32	—	Vin	ns

7.28 HSCMP Specifications

Table 44. HSCMP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Analog input voltage	V_{AIN}	V_{SSA} – 0.01	—	V_{DDA} + 0.01	V
Analog input offset voltage[1]	V_{AIO}	—	—	40	mV
Analog comparator hysteresis[2]	V_H	—	1 to 16	—	mV
Propagation Delay, high speed mode (EN=1, PMODE=1),	t_{DHSN}[3]	—	70	140	ns
Propagation Delay, Low Speed Mode (EN=1, PMODE=0),	t_{AINIT}[4]	—	400	600	ns

1 Offset when the degree of hysteresis is set to its minimum value.
2 The range of hysteresis is based on simulation only. This range varies from part to part.
3 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.
4 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.

7.29 Optimize Power Consumption

See Section 7.7, "Supply Current Characteristics," for a list of I_{DD} requirements for the MC56F825x/MC56F824x. This section provides additional details for optimizing power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static] component
+B: internal [state-dependent] component
+C: internal [dynamic] component
+D: external [dynamic] component
+E: external [static] component

A, the internal [static] component, consists of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent] component, reflects the supply current required by certain on-chip resources only when those resources are in use. These resources include RAM, flash memory, and the ADCs.

C, the internal [dynamic] component, is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic] component, reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This component is also commonly described as $C*V^2*F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 45. I/O Loading Coefficients at 10 MHz

	Intercept	Slope
8 mA drive	1.3	0.11 mW/pF
4 mA drive	1.15 mW	0.11 mW/pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. Table 45 provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases, Equation 2 applies.

$$TotalPower = \Sigma((Intercept + Slope*C_{load})*frequency/10\ MHz) \qquad Eqn.\ 2$$

where:

— Summation is performed over all output pins with capacitive loads.

— Total power is expressed in mW.

— C_{load} is expressed in pF.

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static] component, reflects the effects of placing resistive loads on the outputs of the device. Total all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of nine PWM outputs driving 10 mA into LEDs, then P = 8*0.5*0.01 = 40 mW.

In previous discussions, power consumption due to parasites associated with pure input pins is ignored and assumed to be negligible.

8 Design Considerations

8.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from Equation 3.

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad Eqn.\ 3$$

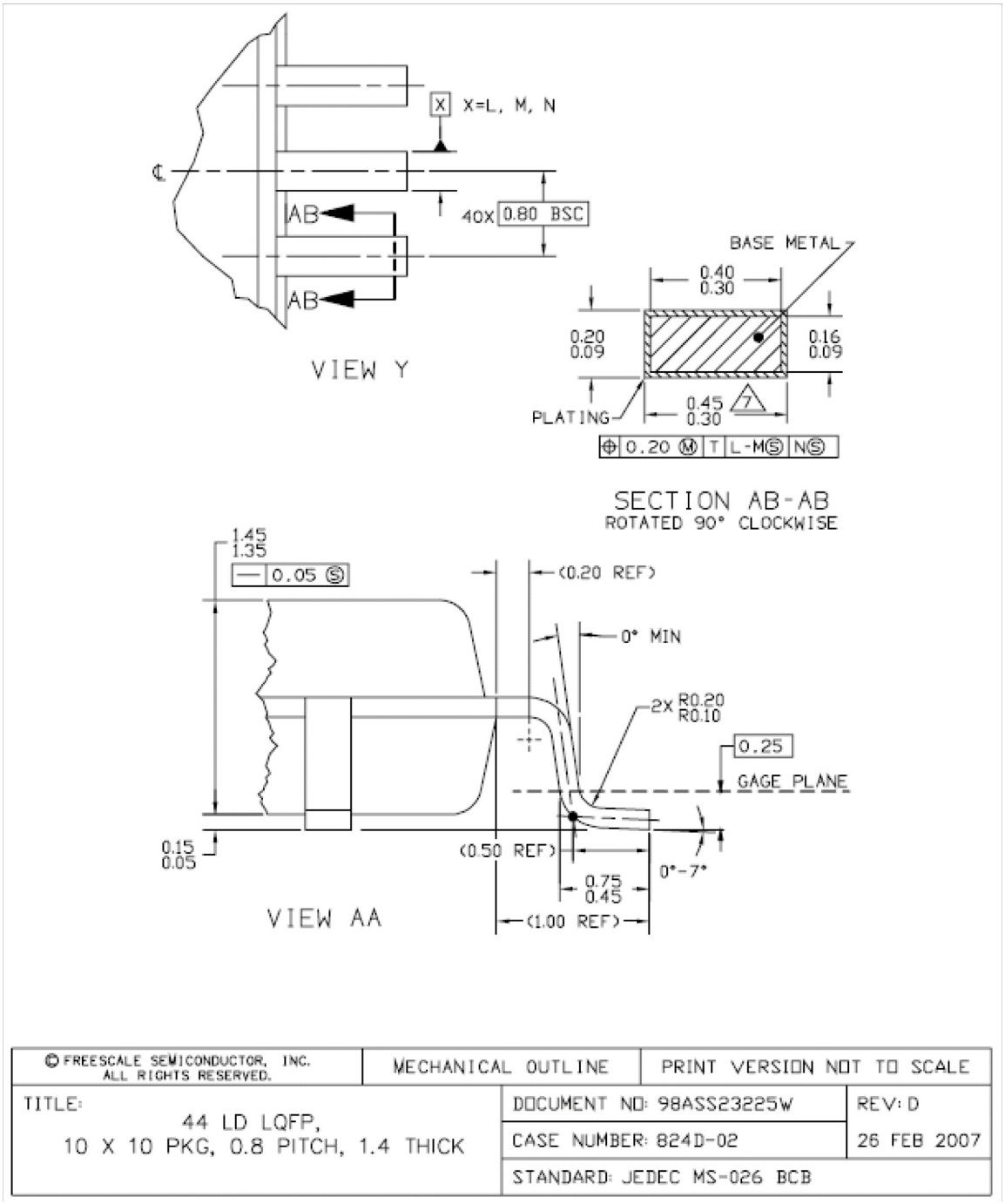
where:

T_A = Ambient temperature for the package (^oC)

$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^oC/W$)

P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which



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