Analog Devices Inc./Maxim Integrated - DS80C310+FCG Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Brown-out Detect/Reset, POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds80c310-fcg

PIN DESCRIPTION

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
				Port 1 (I/O). Port 1 functions as both an 8-bit bidirectional I/O port and an alternate functional interface for Timer 2 I/O and new external interrupts. The reset condition of Port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS80C310 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port once again becomes the output high (and input) state. The alternate modes of Port 1 are outlined as follows:

PIN			PORT	ALTERNATE	FUNCTION
PDIP	PLCC	TQFP			

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
				Port 3 (I/O). Port 3 functions as both an 8-bit bidirectional I/O port and an alternate functional interface for external Interrupts, Serial Port 0, Timer 0 and 1 Inputs, RD and WR strobes. The reset

machine cycle takes 4 clocks. Thus the fastest instruction, 1 machine cycle, executes three times faster for the same crystal frequency. Note that these are identical instructions. The majority of instructions on the DS80C310 will see the full 3-to-1 speed improvement. Some instructions will get between 1.5 and 2.4 to 1 improvement. All instructions are faster than the original 8051.

The numerical average of all op codes gives approximately a 2.5-to-1 speed improvement. Improvement of individual programs depends on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3-to-1 improved op codes makes dramatic speed improvements likely for any code. These architecture improvements and 0.8µm CMOS produce a peak instruction cycle in 160ns (6.25MIPS). The dual data pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions in the DS80C310 perform the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops can be calculated using a table in the *High-Speed Microcontroller User's Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at 4 clocks per increment to take advantage of faster processor operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture the "MOVX A, @ DPTR" instruction and the "MOV direct, direct" instruction used 2 machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS80C310, the MOVX instruction takes as little as 2 machine cycles or 8 oscillator cycles but the "MOV direct, direct" uses 3 machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS80C310 usually uses 1 instruction cycle for each instruction byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only 1 cycle, but some require 5. In the original architecture, all were 1 or 2 cycles except for MUL and DIV. Refer to the *High-Speed Microcontroller User's Guide* for details and individual instruction timing.

MEMORY ACCESS

The DS80C310 has 256 bytes of scratchpad RAM, but contains no on-chip ROM. Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. Timing diagrams are provided in the *Absolute Maximum Ratings* section. Program memory (ROM) is accessed at a fixed rate determined by the crystal frequency and the actual instructions. As mentioned above, an instruction cycle requires 4 clocks. Data memory (RAM) is accessed according to a variable speed MOVX instruction as described below.

STRETCH MEMORY CYCLE

The DS80C310 allows the application software to adjust the speed of data memory access. The microcontroller can perform the MOVX in as few as 2 instruction cycles. However, this value can be stretched as needed so that both fast memory and slow memory or peripherals can be accessed with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCD displays or UARTs that are not fast.

The stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. This allows the user to select a stretch value between 0 and 7. A stretch of 0 results in a 2-machine-cycle MOVX. A stretch of 7 results in a MOVX of 9 machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the stretch value defaults to 1, resulting in a 3-cycle MOVX. Therefore, RAM access is not performed at full speed. This is a convenience to existing designs that may not have fast RAM in place. When maximum speed is desired, the software should select a stretch value of 0. When using very slow RAM or peripherals, a larger stretch value can be selected. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a stretch value between 1 and 7 causes the microcontroller to stretch the read/write strobe and all related timing. This results in a wider read/write strobe allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is shown in the *Absolute Maximum Ratings* section. Note that full speed access is not the reset default case. Table 2 shows the resulting strobe widths for each stretch value. The memory stretch is implemented using the Clock Control Special Function Register at SFR location 8Eh. The stretch value is selected using bits CKCON.2–CKCON.0. In the table, these bits are referred to as M2 through M0. The first stretch (default) allows the use of common 120ns or 150ns RAMs without dramatically lengthening the memory access.

Table 2. Data Memory Cycle Stretch Values

CKCON.2–CKCON.0			MEMORY CYCLES	RD OR WR STROBE WIDTH IN CLOCKS	25MHz STROBE WIDTH (ns)
M2	M1	M0			
0	0	0	2	2	80
0	0	1	3 (default)	4	160
0	1	0	4	8	320
0	1	1	5	12	480
1	0	0	6	16	640
1	0	1	7	20	800
1	1	0	8	24	960
1	1	1	9	28	1120

DUAL DATA POINTER (DPTR)

Data memory block moves can be accelerated using the DS80C310 dual data pointer (DPTR). The standard 8032 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the DS80C310, the standard data pointer is called DPTR and is located at SFR addresses 82h and 83h. These are the standard locations. No modification of standard code is needed to use DPTR. The new DPTR is located at SFR 84h and 85h and is called DPTR1. The DPTR select bit (DPS) chooses the active pointer and is located at the LSB of the SFR location 86h. No other bits in register 86h have any effect and are set to 0. The user switches between data pointers by toggling the LSB of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore, only one instruction is required to switch from a source to a destination address. Using the DPTR saves code from needing to save source and destination addresses when doing a block move. Once loaded, the software simply switches between DPTR0 and 1. The relevant register locations are as follows.

DPL	82h	Low byte original DPTR
DPH	83h	High byte original DPTR
DPL1	84h	Low byte new DPTR
DPH1	85h	High byte new DPTR
DPS	86h	DPTR Select (lsb)

STOP MODE ENHANCEMENTS

Setting bit 1 of the Power Control Register (PCON; 87h) invokes the stop mode. Stop mode is the lowest power state because it turns off all internal clocking. The I_{CC} of a standard stop mode is approximately 1µA (but is specified in the *Absolute Maximum Ratings* section). The CPU exits stop mode from an external interrupt or a reset condition. Internally generated interrupts are not useful since they require clocking activity.

The DS80C310 allows a resume from stop using INT2–INT5, which are edge-triggered interrupts. An internal crystal counter manages the startup timing. A delay of 65,536 clocks occurs to allow the crystal time to stabilize. Software must also insert a delay of 100 machine cycles following the exit from stop mode. This ensures stabilization of internal timing prior to time-critical software tasks such as serial port operations or bus access to memory-mapped I/O devices.

PERIPHERAL OVERVIEW

The DS80C310 provides the same peripheral functions as the standard 80C32. The device is compatible with the DS80C320, but it does not offer all the peripherals.

TIMER RATE CONTROL

There is one important difference between the DS80C310 and 8051 regarding timers. The original 8051 used 12 clocks per cycle for timers and machine cycles. The DS80C310 architecture normally uses 4 clocks per machine cycle. However, in the area of timers and serial ports, the DS80C310 defaults to 12 clocks per cycle on reset. This allows existing code with real-time dependencies such as baud rates to operate properly.

If an application needs higher speed timers or serial baud rates, the user can select individual timers to run at the 4-clock rate. The Clock Control Register (CKCON; 8Eh) determines these timer speeds. When the relevant CKCON bit is logic 1, the DS80C310 uses 4 clocks per cycle to generate timer speeds. When the bit is 0, the DS80C310 uses 12 clocks for timer speeds. The reset condition is 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Note that unless a user desires very fast timing, it is unnecessary to alter these bits. Also note that the timer controls are independent.

POWER-ON RESET

The DS80C310 holds itself in reset during a power-up until 65,536 clock cycles have elapsed. The power-on reset used by the DS80C310 differs somewhat from other members of the high-speed microcontroller family. The crystal oscillator can start anywhere between 1.0V and 4.5V, but is not specified. This eliminates the need for an RC reset circuit. For voltage-specific precision-brownout detection, an external component is needed. When the device goes through a power-on reset, the POR flag is set in the WDCON (D8h) register at bit 6.

INTERRUPTS

The DS80C310 provides 10 interrupt sources with two priority levels. Software can assign high or low priority to all sources. All interrupts that are new to the 8051 have a lower natural priority than the originals.

Table 3. Interrupt Sources and Priorities

NAME	DESCRIPTION	VECTOR	NATURAL PRIORITY
$\overline{\text{INT0}}$	External Interrupt 0	03h	1
TF0	Timer 0	0Bh	2
$\overline{\text{INT1}}$	External Interrupt 1	13h	3
TF1	Timer 1	1Bh	4
SCON	T1 or R1 from the serial port	23h	5
TF2	Timer 2	2Bh	6
INT2	External Interrupt 2	43h	7
$\overline{\text{INT3}}$	External Interrupt 3	4Bh	8
INT4	External Interrupt 4	53h	9
$\overline{\text{INT5}}$	External Interrupt 5	5Bh	10

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……...-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground…….-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature Range…….-55°C to +125°C
Soldering Temperature…….See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.0	5.0	5.5	V	2
Supply Current Active Mode at 25MHz	I_{CC}		30		mA	3
Supply Current Idle Mode at 25MHz	I_{IDLE}		15		mA	4
Supply Current Stop Mode	I_{STOP}		1		µA	5
Input Low Level	V_{IL}	-0.3		+0.8	V	2
Input High Level (Except XTAL1 and RST)	V_{IH}	2.0		V_{CC} + 0.3	V	2
Input High Level XTAL1 and RST	V_{IH2}	3.5		V_{CC} + 0.3	V	2
Output Low Voltage Ports 1, 3 at I_{OL} = 1.6mA	V_{OL1}		0.15	0.45	V	2
Output Low Voltage Port 0, 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA	V_{OL2}		0.15	0.45	V	2, 6
Output High Voltage Port 1, 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA	V_{OH1}	2.4			V	2, 7
Output High Voltage Ports 1, 3 at I_{OH} = -1.5mA	V_{OH2}	2.4			V	2, 8
Output High Voltage Port 0, 2, ALE, $\overline{PSEN}$ at I_{OH} = -8mA	V_{OH3}	2.4			V	2, 6
Input Low Current Ports 1, 3 at 0.45V	I_{IL}			-55	µA	9
Transition Current from 1 to 0 Ports 1, 3 at 2V	I_{TL}			-650	µA	10
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	11
RST Pulldown Resistance	R_{RST}	50		170	kΩ	

Note 1: All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and not product tested.
Note 2: All voltages are referenced to ground.
Note 3: Active current is measured with a 25MHz clock source driving XTAL1, V_{CC} = RST = 5.5V, all other pins disconnected.
Note 4: Idle mode current is measured with a 25MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground, all other pins disconnected.
Note 5: Stop mode current measured with XTAL1 and RST grounded, V_{CC} =5.5V, all other pins disconnected.

Note 6: When addressing external memory. This specification applies to the first clock cycle following the transition. On subsequent cycles following 1 to 0 transitions, the typical current sink capability of Port 0 and Port 2 is approximately 150µA, and the minimum current sink capability of ALE and PSENis approximately 400µA. On subsequent cycles following 0 to 1 transitions, the typical current drive capability of Port 0 and Port 2 is approximately 110µA.

Note 7: RST = V_{CC}. This condition mimics operation of pins in I/O mode.

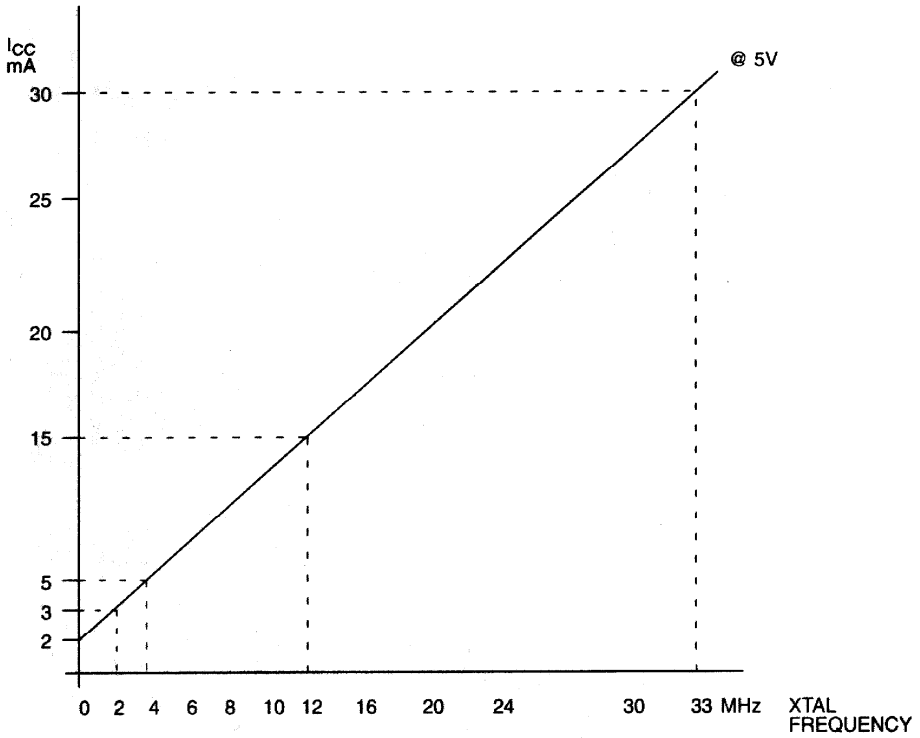
Note 8: During a 0 to 1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.

Note 9: Current required from external circuit to hold a logic-low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to hold the low level; transitions from 1 to 0 on an I/O pin must also overcome the transition current.

Note 10: Ports 1 and 3 source transition current when being pulled down externally. The current reaches its maximum at approximately 2V.

Note 11: $0.45 < V_{IN} < V_{CC}$. Not a high-impedance input. This port is a weak address holding latch because Port 0 is dedicated as an address bus on the DS80C310. Peak current occurs near the input transition point of the latch, approximately 2V.

Figure 2. Typical I_{CC} vs. Frequency



AC ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER		SYMBOL	25MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	25	0	25	MHz
	External Crystal		1	25	1	25	
ALE Pulse Width		t_{LHLL}	40		$1.5t_{CLCL}$-5		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	10		$0.5t_{CLCL}$-5		ns
Address Hold after ALE Low		t_{LLAX1}	2	(Note 2)	$0.5t_{CLCL}$-18	(Note 2)	ns
ALE Low to Valid Instruction In		t_{LLIV}		56		$2.5t_{CLCL}$-20	ns
ALE Low to PSENLow		t_{LLPL}	7		$0.5t_{CLCL}$-13		ns
PSENPulse Width		t_{PLPH}	55		$2t_{CLCL}$-5		ns
PSENLow to Valid Instruction In		t_{PLIV}		41		$2t_{CLCL}$-20	ns
Input Instruction Hold after PSEN		t_{PXIX}	0		0		ns
Input Instruction Float after PSEN		t_{PXIZ}		26		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		71		$3t_{CLCL}$-20	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		81		$3.5t_{CLCL}$-25	ns
PSENLow to Address Float		t_{PLAZ}		(Note 2)		(Note 2)	ns

Note 1: All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Specifications to -40°C are guaranteed by design and not product tested. AC electrical characteristics assume 50% duty cycle for the oscillator, and are not 100% tested but are guaranteed by design. All signals characterized with load capacitance of 80pF except Port 0, ALE, PSEN and WR with 100pF. Interfacing to memory devices with float times (turn-off times) over 25ns can cause contention. This does not damage the parts, but rather causes an increase in operating current. Port 2 and ALE timing changes in relation to duty cycle variation.

Note 2: Address is held in a weak latch until overdriven by external memory.

MOVX CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK MIN	VARIABLE CLOCK MAX	UNITS	STRETCH (Note 1)
Data Access ALE Pulse Width	t_{LHLL2}	$1.5t_{CLCL}-5$		ns	$t_{MCS}=0$
		$2t_{CLCL}-5$			$t_{MCS}>0$
Port 0 Address Valid to ALE Low	t_{AVLL2}	$0.5t_{CLCL}-5$		ns	$t_{MCS}=0$
		$t_{CLCL}-5$			$t_{MCS}>0$
Address Hold after ALE Low for MOVX Write	t_{LLAX2}	$0.5t_{CLCL}-15$		ns	$t_{MCS}=0$
		$t_{CLCL}-7$			$t_{MCS}>0$
RD Pulse Width	t_{RLRH}	$2t_{CLCL}-5$		ns	$t_{MCS}=0$
		$t_{MCS}-10$			$t_{MCS}>0$
WR Pulse Width	t_{WLWH}	$2t_{CLCL}-5$		ns	$t_{MCS}=0$
		$t_{MCS}-10$			$t_{MCS}>0$
RD Low to Valid Data In	t_{RLDV}		$2t_{CLCL}-20$	ns	$t_{MCS}=0$
			$t_{MCS}-20$		$t_{MCS}>0$
Data Hold after Read	t_{RHDX}	0		ns	
Data Float after Read	t_{RHDZ}		$t_{CLCL}-5$	ns	$t_{MCS}=0$
			$2t_{CLCL}-5$		$t_{MCS}>0$
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}-28$	ns	$t_{MCS}=0$
			$t_{CLCL}+t_{MCS}-40$		$t_{MCS}>0$
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}-22$	ns	$t_{MCS}=0$
			$2.0t_{CLCL}+t_{MCS}-25$		$t_{MCS}>0$
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}-35$	ns	$t_{MCS}=0$
			$2.5t_{CLCL}+t_{MCS}-35$		$t_{MCS}>0$
ALE Low to RD or WR Low	t_{LLWL}	$0.5t_{CLCL}-14$	$0.5t_{CLCL}+5$	ns	$t_{MCS}=0$
		$t_{CLCL}-8$	$t_{CLCL}+5$		$t_{MCS}>0$
Port 0 Address to RD or WR Low	t_{AVWL1}	$t_{CLCL}-9$		ns	$t_{MCS}=0$
		$2t_{CLCL}-8$			$t_{MCS}>0$
Port 2 Address to RD or WR Low	t_{AVWL2}	$1.5t_{CLCL}-10$		ns	$t_{MCS}=0$
		$2.5t_{CLCL}-10$			$t_{MCS}>0$
Data Valid to WR Transition	t_{QVWX}	-14		ns	
Data Hold after Write	t_{WHQX}	$t_{CLCL}-11$		ns	$t_{MCS}=0$
		$2t_{CLCL}-10$			$t_{MCS}>0$
RD Low to Address Float	t_{RLAZ}		(Note 2)	ns	
RD or WR High to ALE High	t_{WHLH}	0	10	ns	$t_{MCS}=0$
		$t_{CLCL}-5$	$t_{CLCL}+9$		$t_{MCS}>0$

Note 1: t_{MCS} is a time period related to the stretch memory cycle selection. The following table shows the value of t_{MCS} for each stretch selection.

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

Note 2: Address is held in a weak latch until overdriven by external memory.

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCL}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

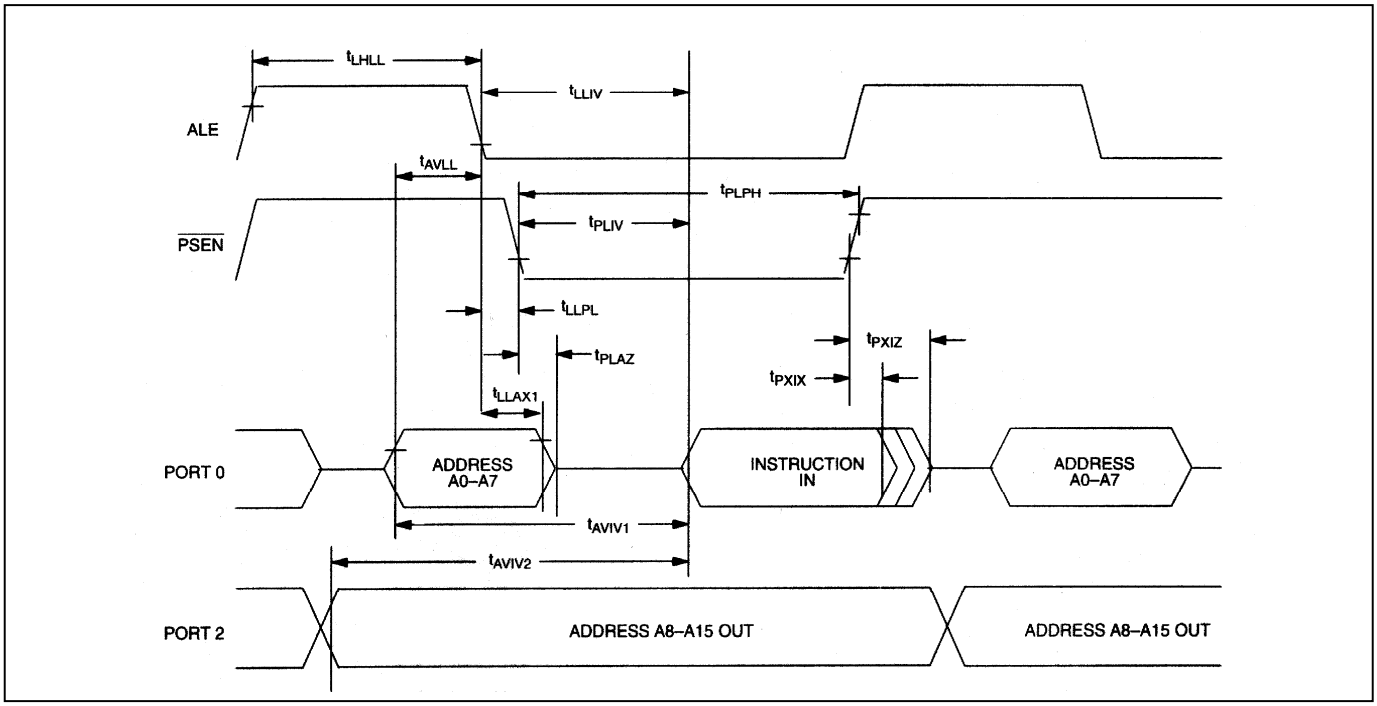
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0, 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0, 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0, 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Input Data Hold after Clock Rising	t_{XHDX}	SM2 = 0, 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0, 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		

DEFINITION OF AC SYMBOLS

In an effort to remain compatible with the original 8051 family, this device specifies the same parameters as such devices, using the same symbols. For completeness, the following are description of the symbols.

t Time
A Address
C Clock
D Input Data
H Logic Level High
L Logic Level Low
I Instruction
P $\overline{PSEN}$
Q Output Data
R $\overline{RD}$ Signal
V Valid
W $\overline{WR}$ Signal
X No longer a valid logic level
Z Tri-State

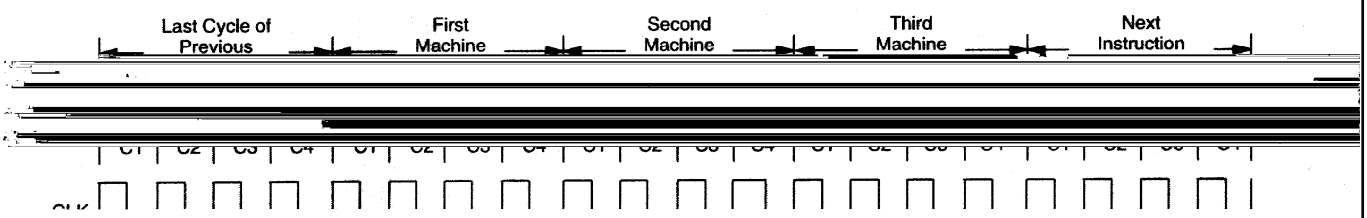
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE

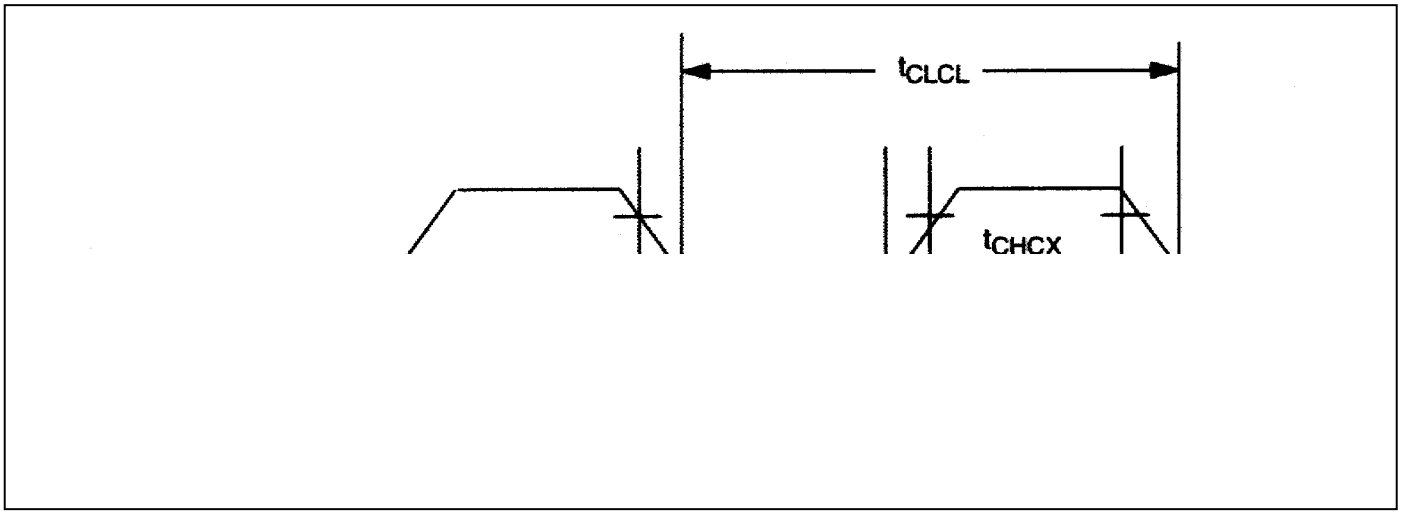
DATA MEMORY WRITE CYCLE

DATA MEMORY WRITE WITH STRETCH = 1



DATA MEMORY WRITE WITH STRETCH = 2

EXTERNAL CLOCK DRIVE



SERIAL PORT MODE 0 TIMING

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
44 TQFP	C44+2	**21-0293**
40 PDIP	P40+1	**21-0044**
44 PLCC	Q44+1	**21-0049**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
090198	1) Added note to clarify I_{IL} specification. 2) Changed serial port mode 0 timing diagram label from t_{QVXL} to t_{QVXH}. 3) Changed minimum oscillator frequency to 1MHz when using external crystal. 4) Corrected "Data memory write with stretch" diagrams to show falling edge of ALE coincident with rising edge of C3 clock.	
012401	1) Added errata disclaimer to page 1.	
102405	1) Device moved to qualified status. Removed "Preliminary" status from data sheet. 2) Removed references to 33MHz versions of the device. 3) Added note requiring 100 machine cycles delay following stop mode exit. This edit transfers existing erratum from errata sheet into data sheet. 4) Updated Absolute Maximum Ratings table to match current format. 5) Displayed Electrical Characteristics test conditions. 6) Added notation that -40°C specifications are guaranteed by design but not tested. 7) Clarified DC Electrical Characteristics note that the specification only applies to the first clock cycle following the transition. 8) Added lead-free part numbers to Ordering Information table. 9) Added t_{AVLL2} specification. 10) Updated AC timing characteristics with full characterization data.	
042106	1) Changed lead-free ordering information part numbers to correctly reflect that the "+" comes after part numbers (e.g., DS80C310-MCG+). 2) Added Note 2 to the AC Electrical Characteristics and MOVX Characteristics tables.	13, 14
8/09	Removed additional references to 33MHz versions of the device.	1, 11

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