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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	11
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301t016f0008aaxuma1

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1300 series devices.

The document describes the characteristics of a superset of the XMC1300 series devices. For simplicity, the various device types are referred to by the collective term XMC1300 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
 - describes the functionality of the superset of devices.
- **Data Sheets**
 - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
 - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc1000> to get access to the latest versions of those documents.

1 Summary of Features

The XMC1300 devices are members of the XMC1000 family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1300 series addresses the real-time control needs of motor control, digital power conversion. It also features peripherals for LED Lighting applications.

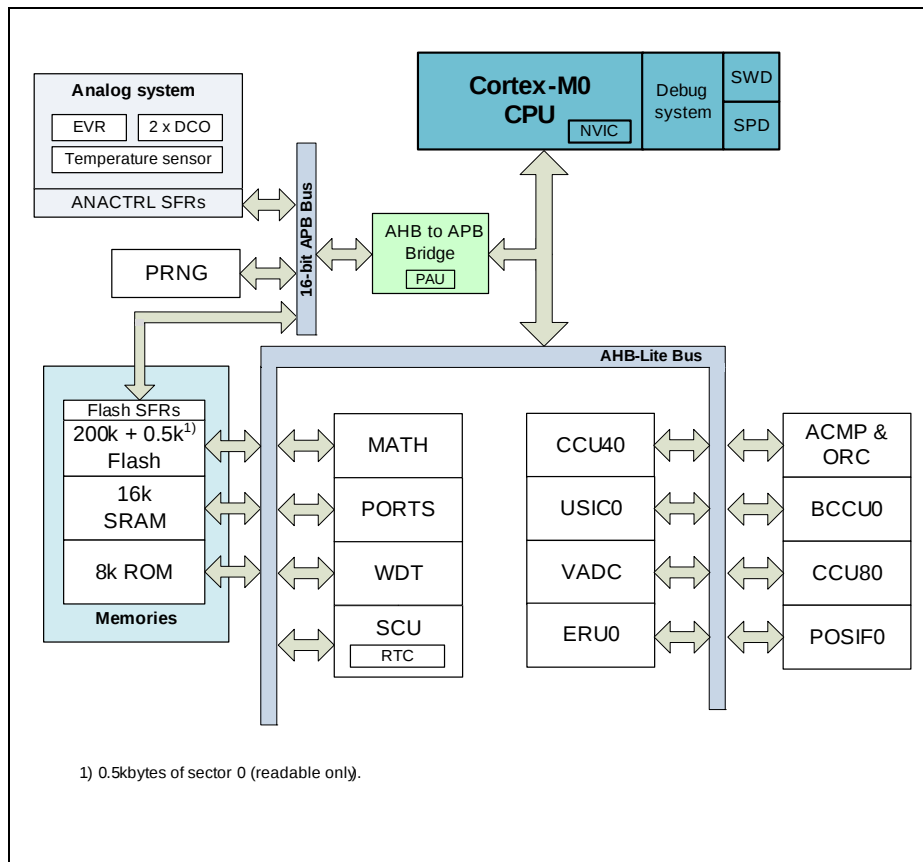


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
 - High Performance 32-bit ARM Cortex-M0 CPU
 - Most of 16-bit Thumb instruction set

Table 4 XMC1300 Chip Identification Number

Derivative	Value	Marking
XMC1301-T016F0008	00013032 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1301-T016F0016	00013032 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1301-T016X0008	00013033 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1301-T016X0016	00013033 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1302-T016X0008	00013033 01FF00FF 00001FF7 0000900F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1302-T016X0016	00013033 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1302-T016X0032	00013033 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1301-T038F0008	00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1301-T038F0016	00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1301-T038F0032	00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1302-T038X0016	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1302-T038X0032	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1302-T038X0064	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083 _H	AA
XMC1302-T038X0128	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00021000 101ED083 _H	AA
XMC1302-T038X0200	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00033000 101ED083 _H	AA
XMC1301-Q024F0008	00013062 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1301-Q024F0016	00013062 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083 _H	AA

Summary of Features
Table 4 XMC1300 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1302-Q024F0016	00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1302-Q024F0032	00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1302-Q024F0064	00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083 _H	AA
XMC1302-Q024X0016	00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1302-Q024X0032	00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1302-Q024X0064	00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083 _H	AA
XMC1301-Q040F0008	00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1301-Q040F0016	00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1301-Q040F0032	00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1302-Q040X0016	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1302-Q040X0032	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1302-Q040X0064	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083 _H	AA
XMC1302-Q040X0128	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00021000 101ED083 _H	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

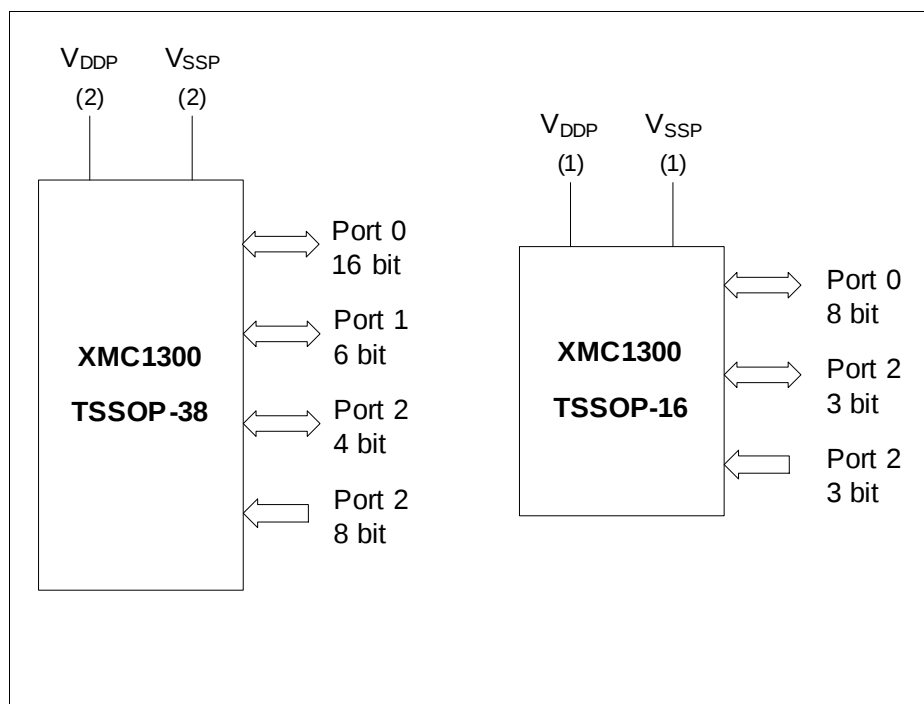


Figure 2 XMC1300 Logic Symbol for TSSOP-38 and TSSOP-16

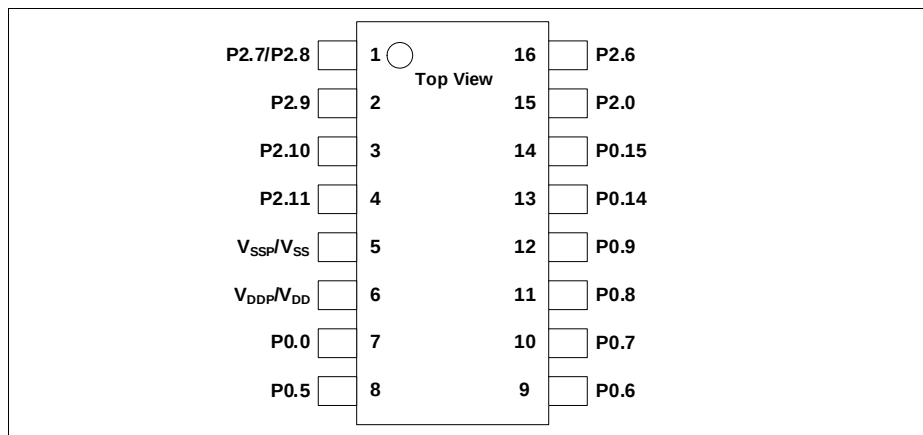


Figure 5 XMC1300 PG-TSSOP-16 Pin Configuration (top view)

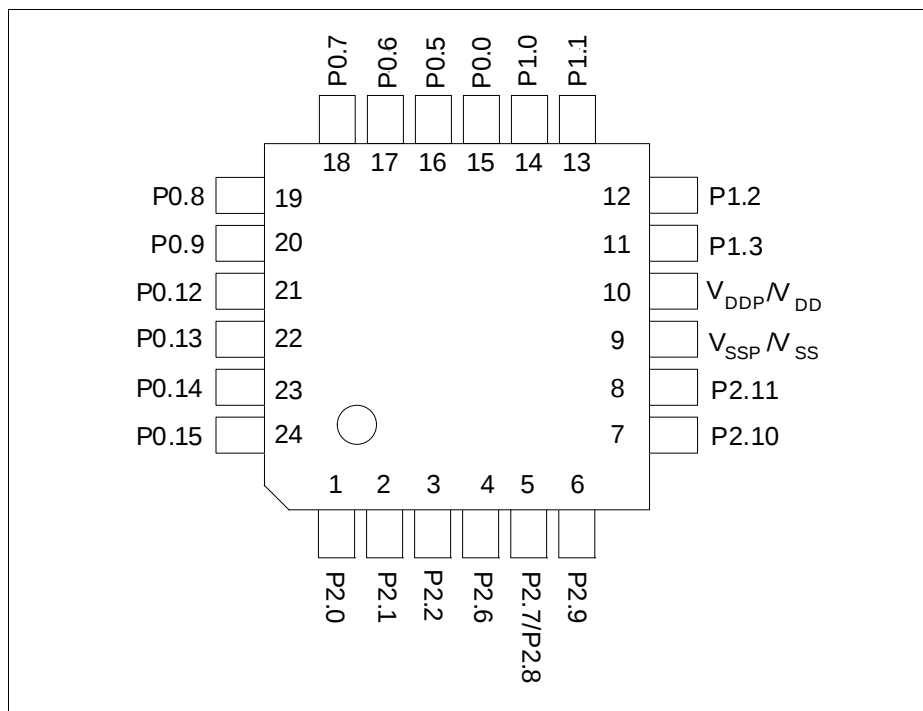


Figure 6 XMC1300 PG-VQFN-24 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 5 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT(standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	15	7	STD_INOUT	
P0.1	24	18	-	-	STD_INOUT	
P0.2	25	19	-	-	STD_INOUT	
P0.3	26	20	-	-	STD_INOUT	
P0.4	27	21	-	-	STD_INOUT	
P0.5	28	22	16	8	STD_INOUT	
P0.6	29	23	17	9	STD_INOUT	
P0.7	30	24	18	10	STD_INOUT	
P0.8	33	27	19	11	STD_INOUT	
P0.9	34	28	20	12	STD_INOUT	
P0.10	35	29	-	-	STD_INOUT	
P0.11	36	30	-	-	STD_INOUT	
P0.12	37	31	21	-	STD_INOUT	

General Device Information
Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	VQFN 24	TSSOP 16	Pad Type	Notes
P0.13	38	32	22	-	STD_INOUT	
P0.14	39	33	23	13	STD_INOUT	
P0.15	40	34	24	14	STD_INOUT	
P1.0	22	16	14	-	High Current	
P1.1	21	15	13	-	High Current	
P1.2	20	14	12	-	High Current	
P1.3	19	13	11	-	High Current	
P1.4	18	12	-	-	High Current	
P1.5	17	11	-	-	High Current	
P1.6	16	-	-	-	STD_INOUT	
P2.0	1	35	1	15	STD_INOUT/AN	
P2.1	2	36	2	-	STD_INOUT/AN	
P2.2	3	37	3	-	STD_IN/AN	
P2.3	4	38	-	-	STD_IN/AN	
P2.4	5	1	-	-	STD_IN/AN	
P2.5	6	2	-	-	STD_IN/AN	
P2.6	7	3	4	16	STD_IN/AN	
P2.7	8	4	5	1	STD_IN/AN	
P2.8	9	5	5	1	STD_IN/AN	
P2.9	10	6	6	2	STD_IN/AN	
P2.10	11	7	7	3	STD_INOUT/AN	
P2.11	12	8	8	4	STD_INOUT/AN	
VSS	13	9	9	5	Power	Supply GND, ADC reference GND
VDD	14	10	10	6	Power	Supply VDD, ADC reference voltage/ ORC reference voltage. VDD has to be supplied with the same voltage as VDDP

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 9 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_S	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on any pin with respect to V_{SSP}	V_{IN}	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	whichever is lower
Voltage on any analog input pin with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	–
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	$\Sigma I_{IN} $	SR	–	–	50	mA	–
Analog comparator input voltage	V_{CM}	SR	-0.3	–	$V_{DDP} + 0.3$	V	

3.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1300. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 10 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	105	°C	Temp. Range X
Digital supply voltage ¹⁾	V_{DDP} SR	1.8	–	5.5	V	
MCLK Frequency	f_{MCLK} CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	f_{PCLK} CC	–	–	66.4	MHz	Peripherals clock

1) See also the Supply Monitoring thresholds, [Chapter 3.3.3](#).

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 11 provides the characteristics of the input/output pins of the XMC1300.

Table 11 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC	–	1.0	V	$I_{OL} = 11 \text{ mA (5 V)}$ $I_{OL} = 7 \text{ mA (3.3 V)}$
			–	0.4	V	$I_{OL} = 5 \text{ mA (5 V)}$ $I_{OL} = 3.5 \text{ mA (3.3 V)}$
Output low voltage on high current pads	V_{OLP1}	CC	–	1.0	V	$I_{OL} = 50 \text{ mA (5 V)}$ $I_{OL} = 25 \text{ mA (3.3 V)}$
			–	0.32	V	$I_{OL} = 10 \text{ mA (5 V)}$
			–	0.4	V	$I_{OL} = 5 \text{ mA (3.3 V)}$
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	$V_{DDP} - 1.0$	–	V	$I_{OH} = -10 \text{ mA (5 V)}$ $I_{OH} = -7 \text{ mA (3.3 V)}$
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4.5 \text{ mA (5 V)}$ $I_{OH} = -2.5 \text{ mA (3.3 V)}$
Output high voltage on high current pads	V_{OHP1}	CC	$V_{DDP} - 0.32$	–	V	$I_{OH} = -6 \text{ mA (5 V)}$
			$V_{DDP} - 1.0$	–	V	$I_{OH} = -8 \text{ mA (3.3 V)}$
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4 \text{ mA (3.3 V)}$
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	$0.19 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	$0.7 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	V_{ILPL}	SR	–	$0.08 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V) ³⁾

3.2.2 Analog to Digital Converters (ADC)

Table 12 shows the Analog to Digital Converter (ADC) characteristics.

Table 12 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	1.8	–	3.0	V	SHSCFG.AREF = 11 _B
		3.0	–	5.5	V	SHSCFG.AREF = 10 _B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00 _B
Analog input voltage range	V_{AIN} SR	$V_{SSP} - 0.05$	–	$V_{DDP} + 0.05$	V	
Auxiliary analog reference ground (SH0-CH0, SH1-CH0)	V_{REFGND} SR	$V_{SSP} - 0.05$	–	$V_{DDP} + 0.05$	V	
Internal reference voltage (full scale value)	V_{REFINT} CC	4.82	5	5.18	V	-40°C - 105°C
		4.9	5	5.1	V	0°C - 85°C ¹⁾
Switched capacitance of an analog input ¹⁾	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00 _B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01 _B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10 _B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11 _B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	¹⁾
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	¹⁾

Electrical Parameter

Table 17 provides the active current consumption of some modules operating at 5 V power supply at 25 °C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 17 Typical Active Current Consumption¹⁾

Active Current Consumption	Symbol	Limit Values	Unit	Test Condition
		Typ.		
Baseload current	I_{CPUDDC}	5.04	mA	Modules including Core, SCU, PORT, memories, ANATOP ²⁾
VADC and SHS	$I_{ADCCDDC}$	3.4	mA	Set CGATCLR0.VADC to 1 ³⁾
USIC0	$I_{USIC0DDC}$	0.87	mA	Set CGATCLR0.USIC0 to 1 ⁴⁾
CCU40	$I_{CCU40DDC}$	0.94	mA	Set CGATCLR0.CCU40 to 1 ⁵⁾
CCU80	$I_{CCU80DDC}$	0.42	mA	Set CGATCLR0.CCU80 to 1 ⁶⁾
POSIF0	$I_{PIF0DDC}$	0.26	mA	Set CGATCLR0.POSIF0 to 1 ⁷⁾
BCCU0	$I_{BCCU0DDC}$	0.24	mA	Set CGATCLR0.BCCU0 to 1 ⁸⁾
MATH	$I_{MATHDDC}$	0.35	mA	Set CGATCLR0.MATH to 1 ⁹⁾
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1 ¹⁰⁾
RTC	$I_{RTCCDDC}$	0.01	mA	Set CGATCLR0.RTC to 1 ¹¹⁾

1) Not subject to production test, verified by design/characterisation.

2) Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.

3) Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode

4) Active current is measured with: module enabled, alternating messages sent to PC at 57.6kbaud every 200ms

5) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500Hz and 1000Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle

6) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU8 slice with PWM frequency at 1500Hz and a period match interrupt used to toggle duty cycle between 10% and 90%

7) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, hall sensor mode

8) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, FCLK=0.8MHz, Normal mode (BCCU Clk = FCLK/4), 3 BCCU Channels and 1 Dimming Engine, change color or dim every 1s

9) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, tangent calculation in while loop; CORDIC circular rotation, no keep, autostart; 32-by-32 bit signed DIV, autostart, DVS right shift by 11

10) Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1s

11) Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled

3.2.7 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 18 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per page	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	$t_{\text{PSE}}^{\text{CC}}$	102	152	204	μs	
Wake-Up time	t_{WU} CC	–	32.2	–	μs	
Read time per word	t_{a} CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States ¹⁾	N_{WSFLASH} CC	0	0.5	–		$f_{\text{MCLK}} = 8 \text{ MHz}$
		0	1.4	–		$f_{\text{MCLK}} = 16 \text{ MHz}$
		1	1.9	–		$f_{\text{MCLK}} = 32 \text{ MHz}$
Erase Cycles per page	N_{ECCY} CC	–	–	$5 \cdot 10^4$	cycles	
Total Erase Cycles	N_{TECCY} CC	–	–	$2 \cdot 10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3 AC Parameters

3.3.1 Testing Waveforms

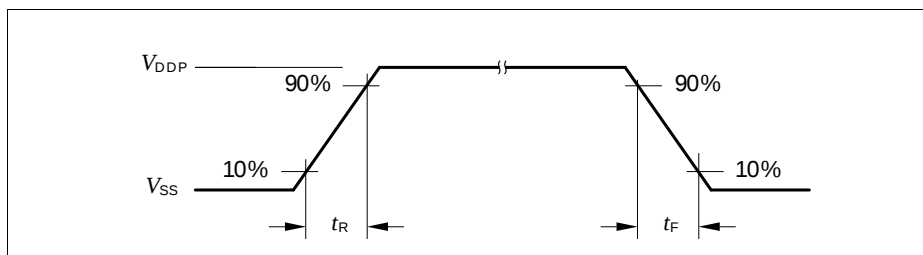


Figure 10 Rise/Fall Time Parameters

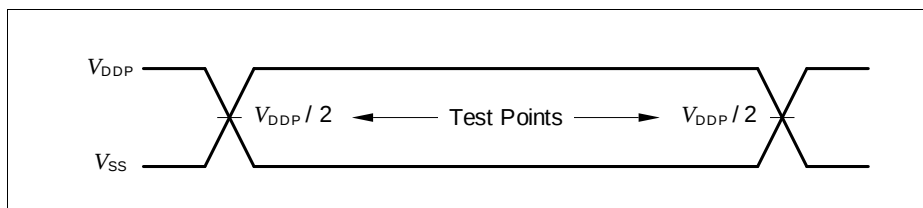


Figure 11 Testing Waveform, Output Delay

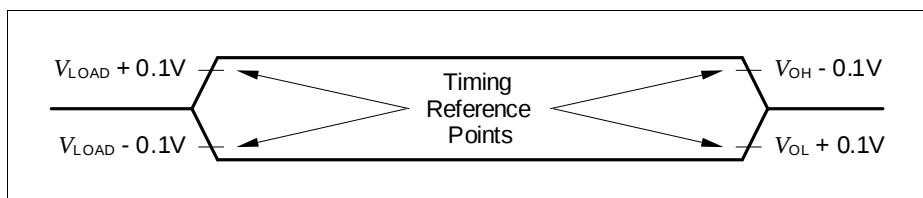


Figure 12 Testing Waveform, Output High Impedance

Electrical Parameter

Figure 14 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

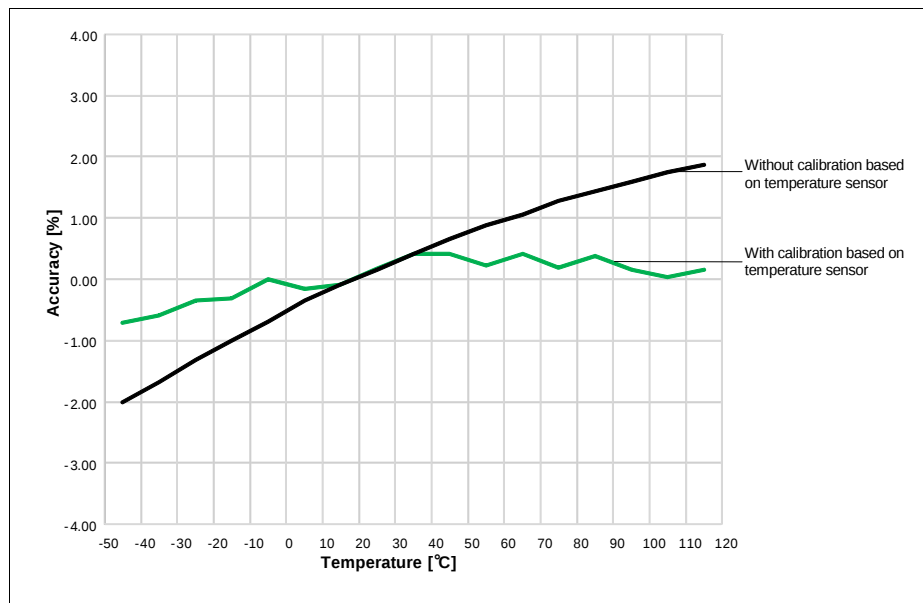


Figure 14 Typical DCO1 accuracy over temperature

Table 22 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1300.

Table 22 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	32.5	32.75	33	kHz	under nominal conditions ¹⁾ after trimming
Accuracy	Δf_{LT}	CC	-1.7	—	3.4	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (0 °C to 85 °C) ²⁾
			-3.9	—	4.0	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (-40 °C to 105 °C) ²⁾

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and $T_{\text{A}} = + 25\text{ °C}$.

2) Not subject to production test, verified by design/characterisation.

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	—	500000	ns	—
SWDCLK low time	t_2 SR	50	—	500000	ns	—
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	—	—	ns	—
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	—	—	ns	—
SWDIO output valid time after SWDCLK rising edge	t_5 CC	—	—	68	ns	$C_L = 50$ pF
		—	—	62	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	—	—	ns	

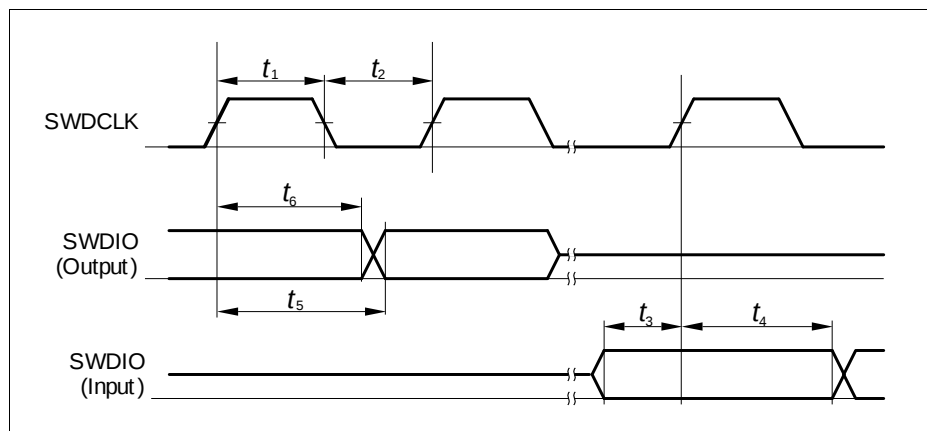


Figure 15 SWD Timing

Table 26 USIC SSC Slave Mode Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive data input DX0/DX[5:3] setup time to shift clock receive edge ¹⁾	t_{12} SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14} CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

3.3.7.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 27 USIC IIC Standard Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	μs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	μs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	μs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	μs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	μs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	μs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

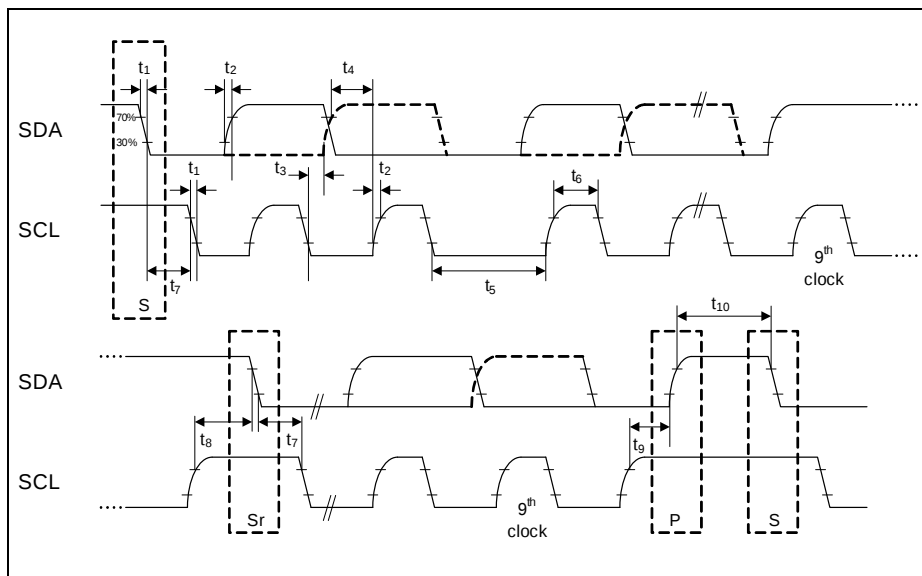


Figure 17 USIC IIC Stand and Fast Mode Timing

3.3.7.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 29 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$2/f_{MCLK}$	-	-	ns	$V_{DDP} \geq 3\text{ V}$
		$4/f_{MCLK}$	-	-	ns	$V_{DDP} < 3\text{ V}$
Clock HIGH	t_2 CC	$0.35 \times t_{1min}$	-	-	ns	
Clock Low	t_3 CC	$0.35 \times t_{1min}$	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	$0.15 \times t_{1min}$	ns	