# Infineon Technologies - XMC1301T016F0016AAXUMA1 Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, I²S, POR, PWM, WDT |
| Number of I/O | 11 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 11x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 16-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | PG-TSSOP-16-8 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301t016f0016aaxuma1 |

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# Table of Contents

**Table 4 XMC1300 Chip Identification Number**

| Derivative | Value | Marking |
|---|---|---|
| XMC1301-T016F0008 | 00013032 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 $101ED083_H$ | AA |
| XMC1301-T016F0016 | 00013032 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 $101ED083_H$ | AA |
| XMC1301-T016X0008 | 00013033 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 $101ED083_H$ | AA |
| XMC1301-T016X0016 | 00013033 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 $101ED083_H$ | AA |
| XMC1302-T016X0008 | 00013033 01FF00FF 00001FF7 0000900F 00000B00 00001000 00003000 $101ED083_H$ | AA |
| XMC1302-T016X0016 | 00013033 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 $101ED083_H$ | AA |
| XMC1302-T016X0032 | 00013033 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 $101ED083_H$ | AA |
| XMC1301-T038F0008 | 00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 $101ED083_H$ | AA |
| XMC1301-T038F0016 | 00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 $101ED083_H$ | AA |
| XMC1301-T038F0032 | 00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00009000 $101ED083_H$ | AA |
| XMC1302-T038X0016 | 00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 $101ED083_H$ | AA |
| XMC1302-T038X0032 | 00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 $101ED083_H$ | AA |
| XMC1302-T038X0064 | 00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 $101ED083_H$ | AA |
| XMC1302-T038X0128 | 00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00021000 $101ED083_H$ | AA |
| XMC1302-T038X0200 | 00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00033000 $101ED083_H$ | AA |
| XMC1301-Q024F0008 | 00013062 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 $101ED083_H$ | AA |
| XMC1301-Q024F0016 | 00013062 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 $101ED083_H$ | AA |

**Table 4 XMC1300 Chip Identification Number** (cont'd)

| Derivative | Value | Marking |
|---|---|---|
| XMC1302-Q024F0016 | 00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083$_H$ | AA |
| XMC1302-Q024F0032 | 00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083$_H$ | AA |
| XMC1302-Q024F0064 | 00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083$_H$ | AA |
| XMC1302-Q024X0016 | 00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083$_H$ | AA |
| XMC1302-Q024X0032 | 00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083$_H$ | AA |
| XMC1302-Q024X0064 | 00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083$_H$ | AA |
| XMC1301-Q040F0008 | 00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083$_H$ | AA |
| XMC1301-Q040F0016 | 00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083$_H$ | AA |
| XMC1301-Q040F0032 | 00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00009000 101ED083$_H$ | AA |
| XMC1302-Q040X0016 | 00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083$_H$ | AA |
| XMC1302-Q040X0032 | 00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083$_H$ | AA |
| XMC1302-Q040X0064 | 00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083$_H$ | AA |
| XMC1302-Q040X0128 | 00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00021000 101ED083$_H$ | AA |

## 2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

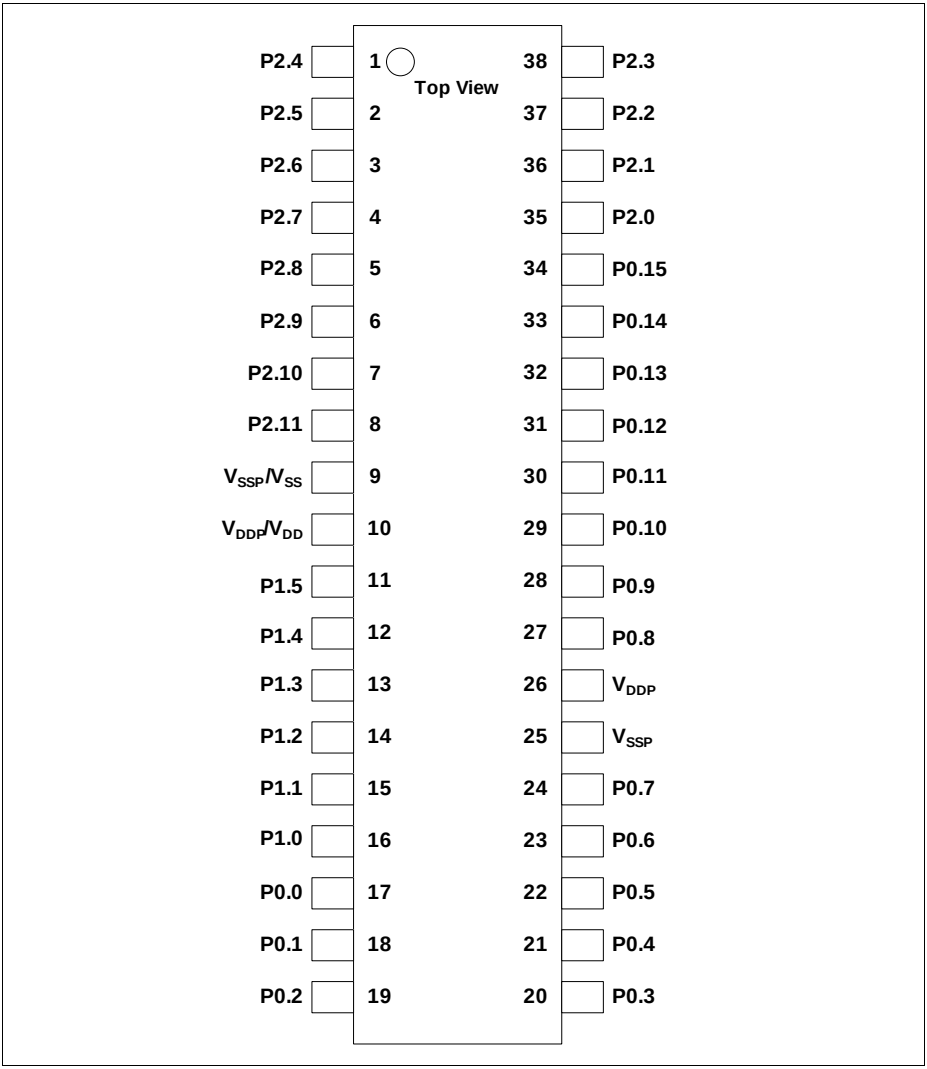


**Figure 4 XMC1300 PG-TSSOP-38 Pin Configuration** (top view)

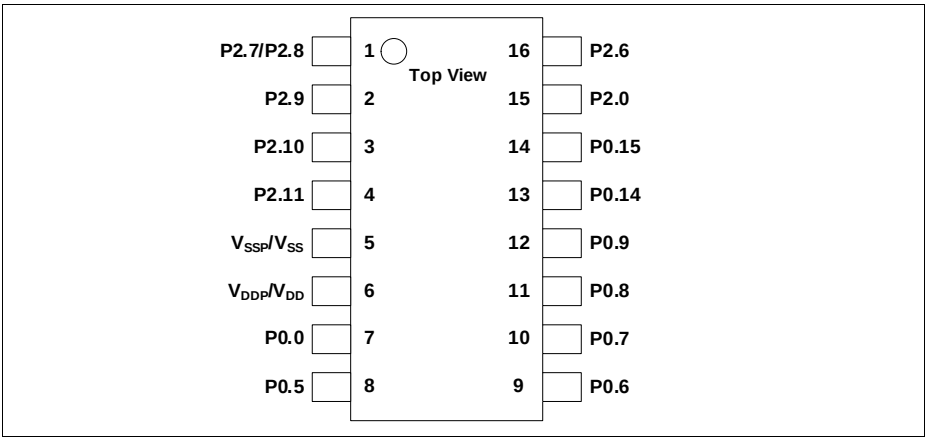


**Figure 5 XMC1300 PG-TSSOP-16 Pin Configuration** (top view)

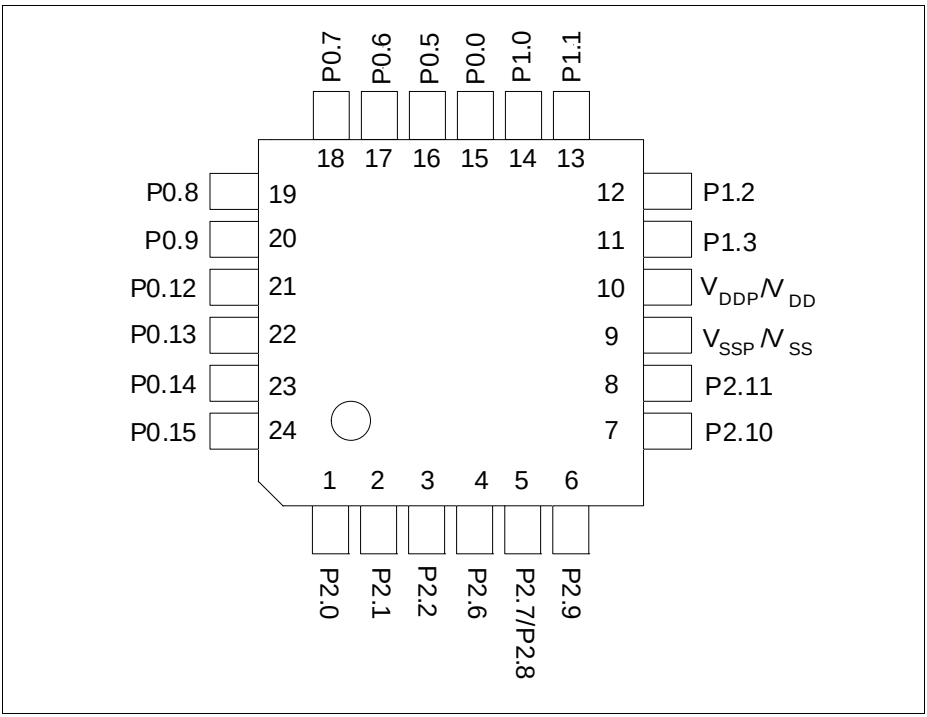


**Figure 6 XMC1300 PG-VQFN-24 Pin Configuration** (top view)

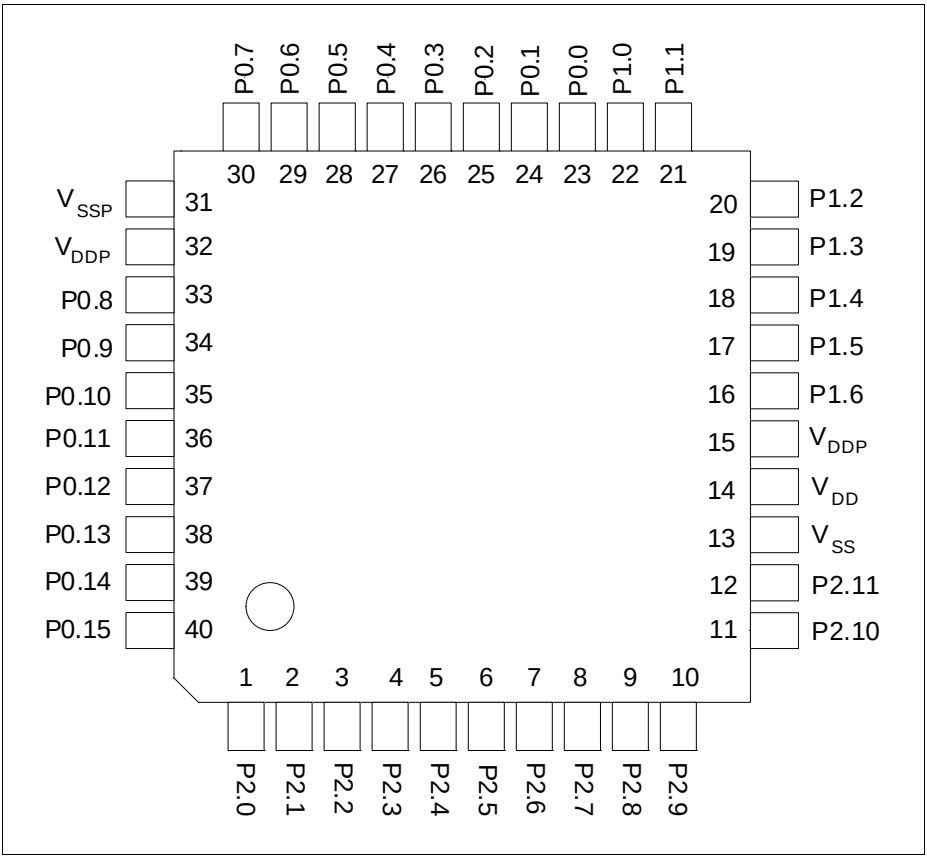


**Figure 7 XMC1300 PG-VQFN-40 Pin Configuration** (top view)

**Table 6 Package Pin Mapping**

| Function | VQFN 40 | TSSOP 38 | VQFN 24 | TSSOP 16 | Pad Type | Notes |
|---|---|---|---|---|---|---|
| VDDP | 15 | 10 | 10 | 6 | Power | I/O port supply |
| VSSP | 31 | 25 | - | - | Power | I/O port ground |
| VDDP | 32 | 26 | - | - | Power | I/O port supply |
| VSSP | Exp. Pad | - | Exp. Pad | - | Power | **Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter. |

# 3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1300.

## 3.1 General Parameters

### 3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1300 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1300 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1300 is designed in.

### 3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 9 Absolute Maximum Rating Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Junction temperature | $T_J$ | SR | -40 | – | 115 | °C | – |
| Storage temperature | $T_S$ | SR | -40 | – | 125 | °C | – |
| Voltage on power supply pin with respect to $V_{SSP}$ | $V_{DDP}$ | SR | -0.3 | – | 6 | V | – |
| Voltage on any pin with respect to $V_{SSP}$ | $V_{IN}$ | SR | -0.5 | – | $V_{DDP}$ + 0.5 or max. 6 | V | whichever is lower |
| Voltage on any analog input pin with respect to $V_{SSP}$ | $V_{AIN}$<br>$V_{AREF}$ | SR | -0.5 | – | $V_{DDP}$ + 0.5 or max. 6 | V | – |
| Input current on any pin during overload condition | $I_{IN}$ | SR | -10 | – | 10 | mA | – |
| Absolute sum of all input currents during overload condition | $\Sigma\|I_{IN}\|$ | SR | – | – | 50 | mA | – |
| Analog comparator input voltage | $V_{CM}$ | SR | -0.3 | – | $V_{DDP}$ + 0.3 | V | |

### 3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages ($V_{AIN}$) above the $V_{DDP}$ on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 13 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; $V_{DDP}$ = 3.0 V - 5.5 V; $C_L$ = 0.25 pF)**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| DC Switching Level | $V_{ODC}$ | CC | 60 | – | 120 | mV | $V_{AIN} \geq V_{DDP} + V_{ODC}$ |
| Hysteresis | $V_{OHYS}$ | CC | 25 | – | $V_{ODC}$ | mV | |
| Always detected Overvoltage Pulse | $t_{OPDD}$ | CC | 103 | – | – | ns | $V_{AIN} \geq V_{DDP}$ + 150 mV |
| | | | 88 | – | – | ns | $V_{AIN} \geq V_{DDP}$ + 350 mV |
| Never detected Overvoltage Pulse | $t_{OPDN}$ | CC | – | – | 21 | ns | $V_{AIN} \geq V_{DDP}$ + 150 mV |
| | | | – | – | 11 | ns | $V_{AIN} \geq V_{DDP}$ + 350 mV |
| Detection Delay | $t_{ODD}$ | CC | 39 | – | 132 | ns | $V_{AIN} \geq V_{DDP}$ + 150 mV |
| | | | 31 | – | 121 | ns | $V_{AIN} \geq V_{DDP}$ + 350 mV |
| Release Delay | $t_{ORD}$ | CC | 44 | – | 240 | ns | $V_{AIN} \leq V_{DDP}$; $V_{DDP}$ = 5 V |
| | | | 57 | – | 340 | ns | $V_{AIN} \leq V_{DDP}$; $V_{DDP}$ = 3.3 V |
| Enable Delay | $t_{OED}$ | CC | – | – | 300 | ns | ORCCTRL.ENORCx = 1 |

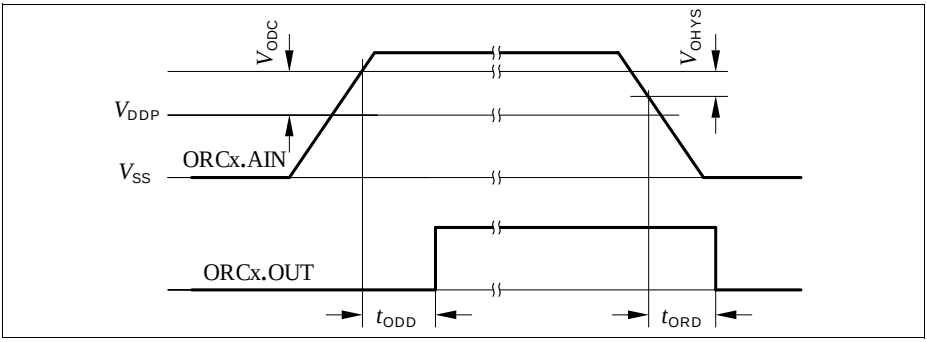


**Figure 9 ORCx.OUT Trigger Generation**

### 3.2.7 Flash Memory Parameters

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 18 Flash Memory Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Erase Time per page | $t_{ERASE}$ CC | 6.8 | 7.1 | 7.6 | ms | |
| Program time per block | $t_{PSER}$ CC | 102 | 152 | 204 | µs | |
| Wake-Up time | $t_{WU}$ CC | – | 32.2 | – | µs | |
| Read time per word | $t_a$ CC | – | 50 | – | ns | |
| Data Retention Time | $t_{RET}$ CC | 10 | – | – | years | Max. 100 erase / program cycles |
| Flash Wait States [1] | $N_{WSFLASH}$ CC | 0 | 0.5 | – | | $f_{MCLK}$ = 8 MHz |
| | | 0 | 1.4 | – | | $f_{MCLK}$ = 16 MHz |
| | | 1 | 1.9 | – | | $f_{MCLK}$ = 32 MHz |
| Erase Cycles per page | $N_{ECYC}$ CC | – | – | $5*10^4$ | cycles | |
| Total Erase Cycles | $N_{TECYC}$ CC | – | – | $2*10^6$ | cycles | |

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

**Figure 14** shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

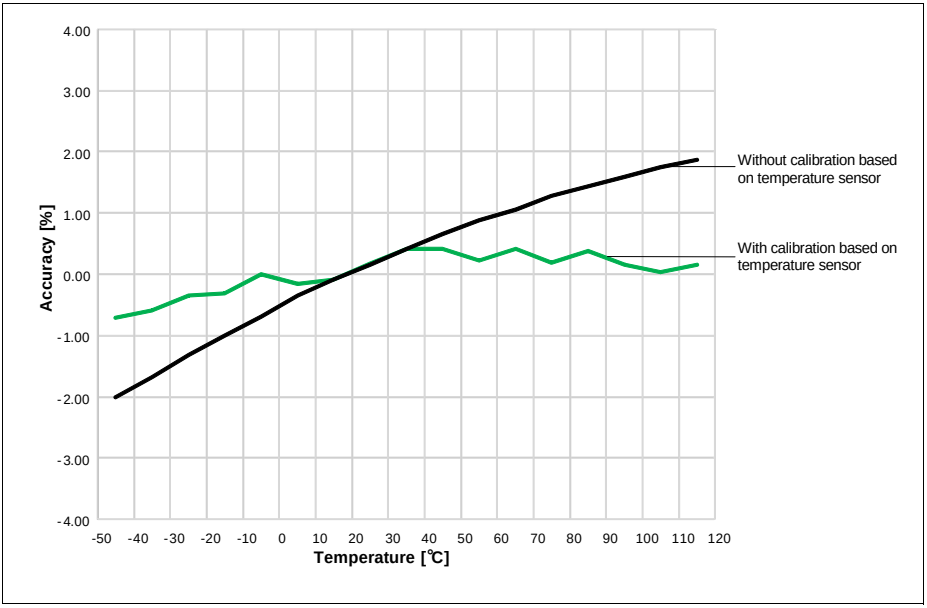


**Figure 14 Typical DCO1 accuracy over temperature**

**Table 22** provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1300.

**Table 22 32 kHz DCO2 Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{NOM}$ | CC | 32.5 | 32.75 | 33 | kHz | under nominal conditions[1] after trimming |
| Accuracy | $\Delta f_{LT}$ | CC | -1.7 | – | 3.4 | % | with respect to $f_{NOM}$(typ), over temperature (0 °C to 85 °C)[2] |
| | | | -3.9 | – | 4.0 | % | with respect to $f_{NOM}$(typ), over temperature (-40 °C to 105 °C)[2] |

1) The deviation is relative to the factory trimmed frequency at nominal $V_{DDC}$ and $T_A$ = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

### 3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 23 SWD Interface Timing Parameters**(Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SWDCLK high time | $t_1$ SR | 50 | – | 500000 | ns | – |
| SWDCLK low time | $t_2$ SR | 50 | – | 500000 | ns | – |
| SWDIO input setup to SWDCLK rising edge | $t_3$ SR | 10 | – | – | ns | – |
| SWDIO input hold after SWDCLK rising edge | $t_4$ SR | 10 | – | – | ns | – |
| SWDIO output valid time after SWDCLK rising edge | $t_5$ CC | – | – | 68 | ns | $C_L$ = 50 pF |
| | | – | – | 62 | ns | $C_L$ = 30 pF |
| SWDIO output hold time from SWDCLK rising edge | $t_6$ CC | 4 | – | – | ns | |

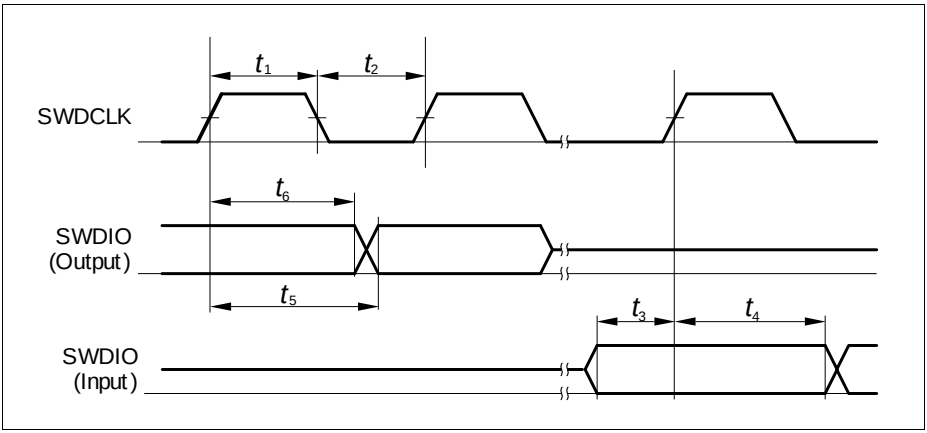


**Figure 15 SWD Timing**

**Table 26 USIC SSC Slave Mode Timing** (cont'd)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1] | $t_{12}$ | SR | 10 | – | – | ns | |
| Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1] | $t_{13}$ | SR | 10 | – | – | ns | |
| Data output DOUT[3:0] valid time | $t_{14}$ | CC | - | – | 80 | ns | |

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

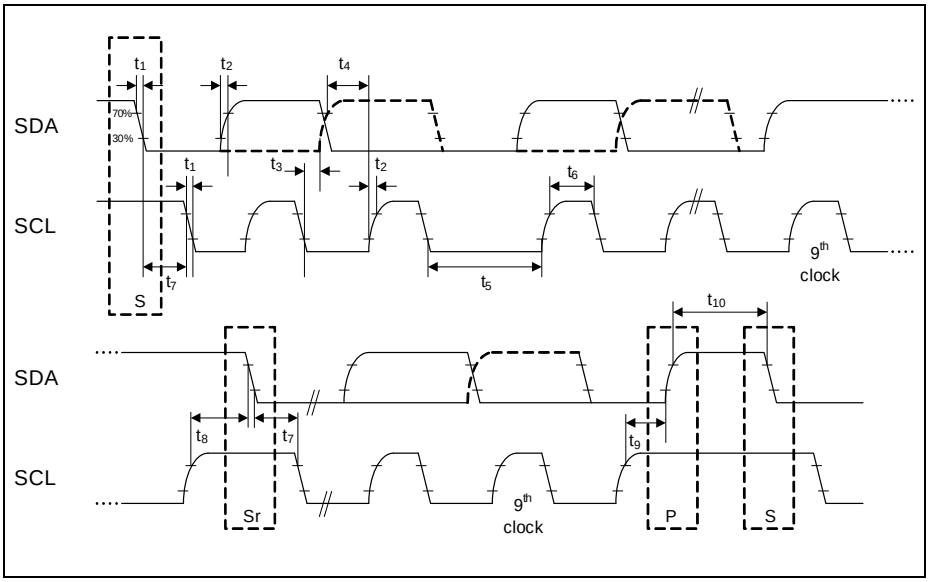


**Figure 17 USIC IIC Stand and Fast Mode Timing**

### 3.3.7.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

*Note: Operating Conditions apply.*

**Table 29 USIC IIS Master Transmitter Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_1$ CC | $2/f_{MCLK}$ | - | - | ns | $V_{DDP} \geq 3$ V |
| | | $4/f_{MCLK}$ | - | - | ns | $V_{DDP} < 3$ V |
| Clock HIGH | $t_2$ CC | 0.35 x $t_{1min}$ | - | - | ns | |
| Clock Low | $t_3$ CC | 0.35 x $t_{1min}$ | - | - | ns | |
| Hold time | $t_4$ CC | 0 | - | - | ns | |
| Clock rise time | $t_5$ CC | - | - | 0.15 x $t_{1min}$ | ns | |

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers ($P_{IODYN}$) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce $V_{DDP}$, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

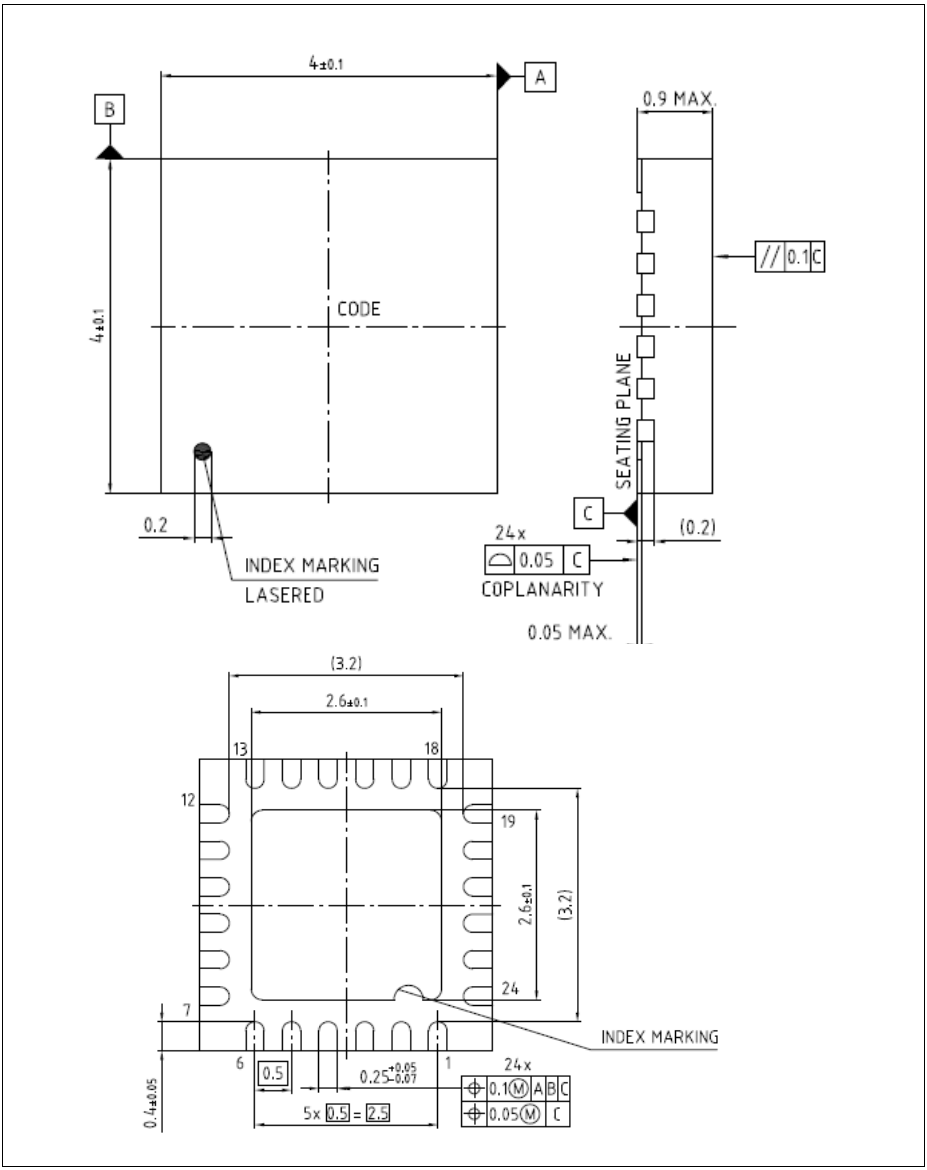


**Figure 22 PG-VQFN-24-19**

# 5 Quality Declaration

Table 32 shows the characteristics of the quality parameters in the XMC1300.

**Table 32 Quality Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ SR | - | 2000 | V | Conforming to EIA/JESD22-A114-B |
| ESD susceptibility according to Charged Device Model (CDM) pins | $V_{CDM}$ SR | - | 500 | V | Conforming to JESD22-C101-C |
| Moisture sensitivity level | $MSL$ CC | - | 3 | - | JEDEC J-STD-020C |

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