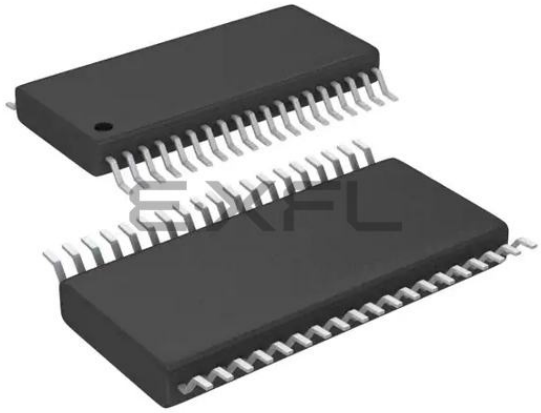
Infineon Technologies - XMC1301T038F0008AAXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301t038f0008aaxuma1

XMC1300 Data Sheet

Revision History: V1.4 2014-05

Previous Version: V1.3	
Page	Subjects
Page 12	ADC channels of Table 2 is updated. Table 3 is added.
Page 12	Description for Chip Identification Number of Section 1.4 is updated.
Page 20	The pad type is corrected for P1.6 in Table 6.
Page 32	The t_{C12} , f_{C12}, t_{C10}, f_{C10}, t_{C8} and f_{C8} parameters are updated in Table 12.
Page 35	Figure 8 is added.
Page 38	The t_{SR} and t_{TSAL} parameters are updated in Table 15.
Page 41	Parameter name for t_{PSER} is updated. The $N_{WSFLASH}$ parameter and test condition for t_{RET} are added to Table 18.
Page 44	The min value for V_{DDPBO} parameter is added to Table 20. Footnote 1 is updated.
Page 46	The Δf_{LTT} parameter is added to Table 21.
Page 47	Figure 14 is added.

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Table of Contents

Input/Output Lines

- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

On-Chip Debug Support

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - T: TSSOP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1300 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1300 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC1300** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC1300 **Device Types**

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1301-T016F0008	PG-TSSOP-16-8	8	16
XMC1301-T016F0016	PG-TSSOP-16-8	16	16
XMC1301-T016X0008	PG-TSSOP-16-8	8	16
XMC1301-T016X0016	PG-TSSOP-16-8	16	16

Table 1 Synopsis of XMC1300 Device Types (cont'd)

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1302-T016X0008	PG-TSSOP-16-8	8	16
XMC1302-T016X0016	PG-TSSOP-16-8	16	16
XMC1302-T016X0032	PG-TSSOP-16-8	32	16
XMC1301-T038F0008	PG-TSSOP-38-9	8	16
XMC1301-T038F0016	PG-TSSOP-38-9	16	16
XMC1301-T038F0032	PG-TSSOP-38-9	32	16
XMC1302-T038X0016	PG-TSSOP-38-9	16	16
XMC1302-T038X0032	PG-TSSOP-38-9	32	16
XMC1302-T038X0064	PG-TSSOP-38-9	64	16
XMC1302-T038X0128	PG-TSSOP-38-9	128	16
XMC1302-T038X0200	PG-TSSOP-38-9	200	16
XMC1301-Q024F0008	PG-VQFN-24-19	8	16
XMC1301-Q024F0016	PG-VQFN-24-19	16	16
XMC1302-Q024F0016	PG-VQFN-24-19	16	16
XMC1302-Q024F0032	PG-VQFN-24-19	32	16
XMC1302-Q024F0064	PG-VQFN-24-19	64	16
XMC1302-Q024X0016	PG-VQFN-24-19	16	16
XMC1302-Q024X0032	PG-VQFN-24-19	32	16
XMC1302-Q024X0064	PG-VQFN-24-19	64	16
XMC1301-Q040F0008	PG-VQFN-40-13	8	16
XMC1301-Q040F0016	PG-VQFN-40-13	16	16
XMC1301-Q040F0032	PG-VQFN-40-13	32	16
XMC1302-Q040X0016	PG-VQFN-40-13	16	16
XMC1302-Q040X0032	PG-VQFN-40-13	32	16
XMC1302-Q040X0064	PG-VQFN-40-13	64	16
XMC1302-Q040X0128	PG-VQFN-40-13	128	16

1.3 Device Type Features

The following table lists the available features per device type.

Table 4 XMC1300 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1302-Q024F0016	00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1302-Q024F0032	00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1302-Q024F0064	00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1302-Q024X0016	00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1302-Q024X0032	00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1302-Q024X0064	00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1301-Q040F0008	00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083$_H$	AA
XMC1301-Q040F0016	00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1301-Q040F0032	00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1302-Q040X0016	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1302-Q040X0032	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1302-Q040X0064	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1302-Q040X0128	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00021000 101ED083$_H$	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

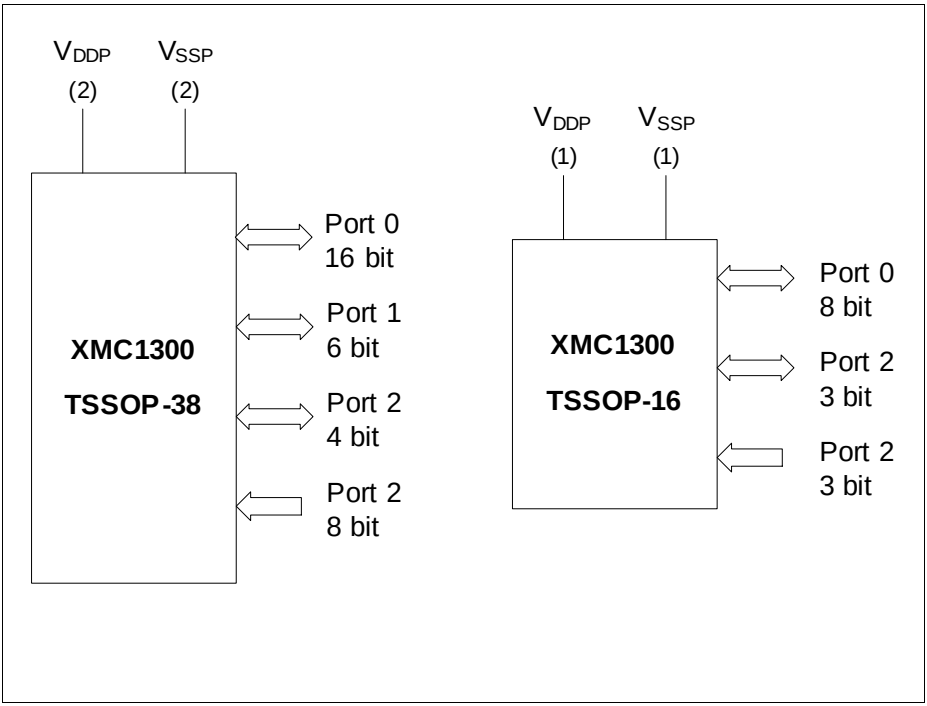

Figure 2 XMC1300 Logic Symbol for TSSOP-38 and TSSOP-16

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

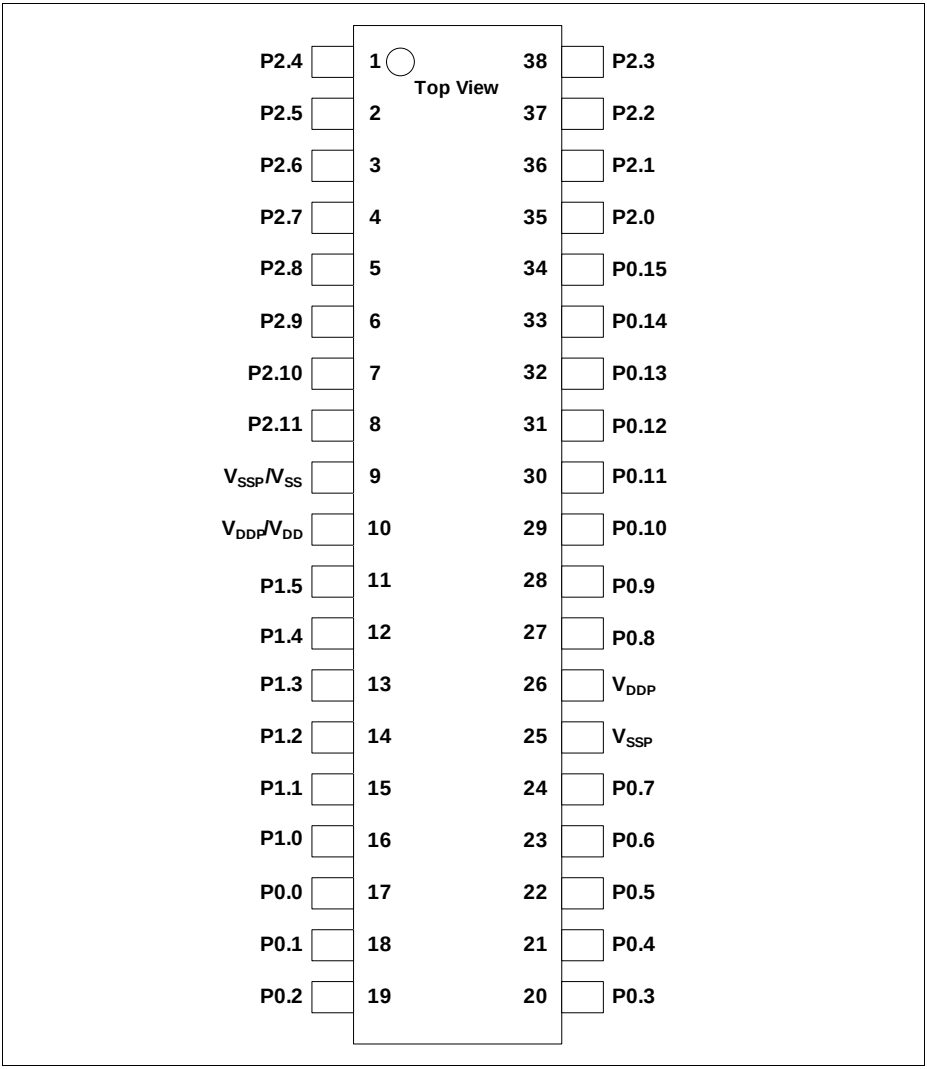

Figure 4 XMC1300 PG-TSSOP-38 Pin Configuration (top view)

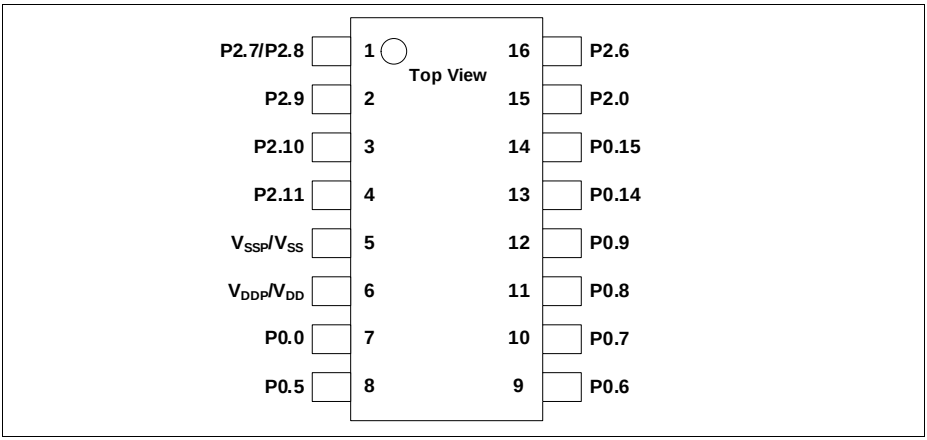

Figure 5 XMC1300 PG-TSSOP-16 Pin Configuration (top view)

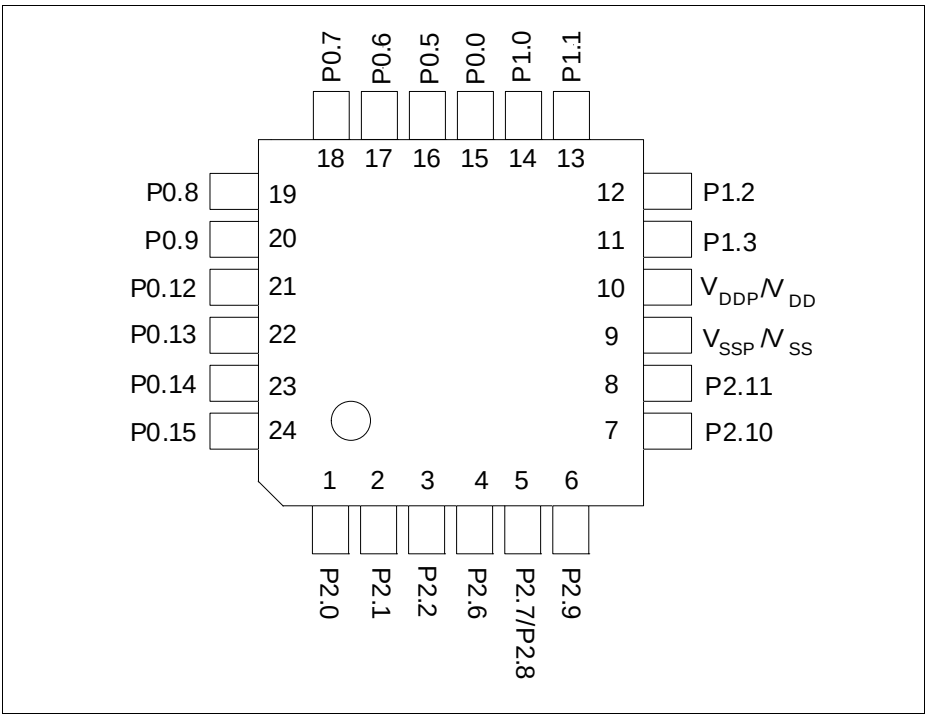

Figure 6 XMC1300 PG-VQFN-24 Pin Configuration (top view)

Table 8 Port I/O Functions (cont'd)

Function	Outputs									Inputs										
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input	Input
P1.6	VADC0. EMUX12	USIC0_CH1 .DOUT0		USIC0_CH0 .SCLKOUT	BCCU0. OUT2	USIC0_CH0 .SELO2	USIC0_CH1 .SELO3							USIC0_CH0 .DX5F						
P2.0	ERU0. PDOUT3	CCU40. OUT0	ERU0. GOUT3		CCU80. OUT20	USIC0_CH0 .DOUT0	USIC0_CH0 .SCLKOUT						VADC0. G0CH5		ERU0.0B0	USIC0_CH0 .DX0E	USIC0_CH0 .DX1E	USIC0_CH1 .DX2F			
P2.1	ERU0. PDOUT2	CCU40. OUT1	ERU0. GOUT2		CCU80. OUT21	USIC0_CH0 .DOUT0	USIC0_CH1 .SCLKOUT					ACMP2.INP	VADC0. G0CH6		ERU0.1B0	USIC0_CH0 .DX0F	USIC0_CH1 .DX3A	USIC0_CH1 .DX4A			
P2.2												ACMP2.INN	VADC0. G0CH7		ERU0.0B1	USIC0_CH0 .DX3A	USIC0_CH0 .DX4A	USIC0_CH1 .DX5A	ORC0.AIN		
P2.3													VADC0. G1CH5		ERU0.1B1	USIC0_CH0 .DX5B	USIC0_CH1 .DX3C	USIC0_CH1 .DX4C	ORC1.AIN		
P2.4													VADC0. G1CH6		ERU0.0A1	USIC0_CH0 .DX3B	USIC0_CH0 .DX4B	USIC0_CH1 .DX5B	ORC2.AIN		
P2.5													VADC0. G1CH7		ERU0.1A1	USIC0_CH0 .DX5D	USIC0_CH1 .DX3E	USIC0_CH1 .DX4E	ORC3.AIN		
P2.6												ACMP1.INN	VADC0. G0CH0		ERU0.2A1	USIC0_CH0 .DX3E	USIC0_CH0 .DX4E	USIC0_CH1 .DX5D	ORC4.AIN		
P2.7												ACMP1.INP	VADC0. G1CH1		ERU0.3A1	USIC0_CH0 .DX5C	USIC0_CH1 .DX3D	USIC0_CH1 .DX4D	ORC5.AIN		
P2.8												ACMP0.INN	VADC0. G0CH1	VADC0. G1CH0	ERU0.3B1	USIC0_CH0 .DX3D	USIC0_CH0 .DX4D	USIC0_CH1 .DX5C	ORC6.AIN		
P2.9												ACMP0.INP	VADC0. G0CH2	VADC0. G1CH4	ERU0.3B0	USIC0_CH0 .DX5A	USIC0_CH1 .DX3B	USIC0_CH1 .DX4B	ORC7.AIN		
P2.10	ERU0. PDOUT1	CCU40. OUT2	ERU0. GOUT1		CCU80. OUT30	ACMP0. OUT	USIC0_CH1 .DOUT0						VADC0. G0CH3	VADC0. G1CH2	ERU0.2B0	USIC0_CH0 .DX3C	USIC0_CH0 .DX4C	USIC0_CH1 .DX0F			
P2.11	ERU0. PDOUT0	CCU40. OUT3	ERU0. GOUT0		CCU80. OUT31	USIC0_CH1 .SCLKOUT	USIC0_CH1 .DOUT0					ACMP.REF	VADC0. G0CH4	VADC0. G1CH3	ERU0.2B1	USIC0_CH1 .DX0E	USIC0_CH1 .DX1E				

3.2.2 Analog to Digital Converters (ADC)

Table 12 shows the Analog to Digital Converter (ADC) characteristics.

Table 12 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	1.8	–	3.0	V	SHSCFG.AREF = 11_B
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground (SH0-CH0, SH1-CH0)	V_{REFGND} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Internal reference voltage (full scale value)	V_{REFINT} CC	4.82	5	5.18	V	-40°C - 105°C
		4.9	5	5.1	V	0°C - 85°C [1]
Switched capacitance of an analog input[1]	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	[1]
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	[1]

Table 12 ADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode [3]	f_{C8} CC	–	–	f_{ADC} / 38.5	–	1 sample pending
		–	–	f_{ADC} / 54.5	–	2 samples pending
DNL error	EA_{DNL} CC	–	±2.0	–	LSB 12	
INL error	EA_{INL} CC	–	±4.0	–	LSB 12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00_B (calibrated)
Gain error with internal reference	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 105°C
		–	±2.0	–	%	SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±6.0	–	LSB 12	Calibrated

1) Not subject to production test, verified by design/characterization.

2) No pending samples assumed, excluding sampling time and calibration.

3) Includes synchronization and calibration (average of gain and offset calibration).

3.2.4 Analog Comparator Characteristics

Table 14 below shows the Analog Comparator characteristics.

Table 14 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes/ Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	–	V_{DDP} + 0.05	V	
Input Offset	V_{CMPOFF}	CC	–	+/-3	–	mV	High power mode ΔV_{CMP} < 200 mV
			–	+/-20	–	mV	Low power mode[2] ΔV_{CMP} < 200 mV
Propagation Delay[1][2]	t_{PDELAY}	CC	–	25	–	ns	High power mode, ΔV_{CMP} = 100 mV
			–	80	–	ns	High power mode, ΔV_{CMP} = 25 mV
			–	250	–	ns	Low power mode, ΔV_{CMP} = 100 mV
			–	700	–	ns	Low power mode, ΔV_{CMP} = 25 mV
Current Consumption[2]	I_{ACMP}	CC	–	100	–	µA	First active ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	66	–	µA	Each additional ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	10	–	µA	First active ACMP in low power mode
			–	6	–	µA	Each additional ACMP in low power mode
Input Hysteresis[2]	V_{HYS}	CC	–	15	–	mV	
Filter Delay[1][2]	t_{FDELAY}	CC	–	5	–	ns	

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

2) Not subject to production test, verified by design.

3.2.5 Temperature Sensor Characteristics

Table 15 Temperature Sensor Characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy[2)]	T_{TSAL} CC	–	+/-20	–	°C	T_J = -40 °C
		–	+/-12	–	°C	T_J = -25 °C
		-5	–	5	°C	T_J = 0 °C
		-2	–	2	°C	T_J = 25 °C
		-4	–	4	°C	T_J = 70 °C
		-2	–	2	°C	T_J = 115 °C

1) Not subject to production test, verified by design/characterization.

2) The temperature sensor accuracy is independent of the supply voltage.

3.2.7 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 18 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per page	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	t_{PSER} CC	102	152	204	µs	
Wake-Up time	t_{WU} CC	–	32.2	–	µs	
Read time per word	t_a CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States [1]	$N_{WSFLASH}$ CC	0	0.5	–		f_{MCLK} = 8 MHz
		0	1.4	–		f_{MCLK} = 16 MHz
		1	1.9	–		f_{MCLK} = 32 MHz
Erase Cycles per page	N_{ECYC} CC	–	–	$5*10^4$	cycles	
Total Erase Cycles	N_{TECYC} CC	–	–	$2*10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3.4 On-Chip Oscillator Characteristics

Table 21 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1300.

Table 21 64 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	63.5	64	64.5	MHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (T_A = 0 °C to 85 °C)[2]
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (T_A = -40 °C to 105 °C)[2]
Accuracy with calibration based on temperature sensor	Δf_{LTT}	CC	-1.3	–	1.25	%	with respect to f_{NOM}(typ), over temperature (T_A = 0 °C to 105 °C)[2]
			-2.6	–	1.25	%	with respect to f_{NOM}(typ), over temperature (T_A = -40 °C to 105 °C)[2]

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	–	500000	ns	–
SWDCLK low time	t_2 SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5 CC	–	–	68	ns	C_L = 50 pF
		–	–	62	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	–	–	ns	

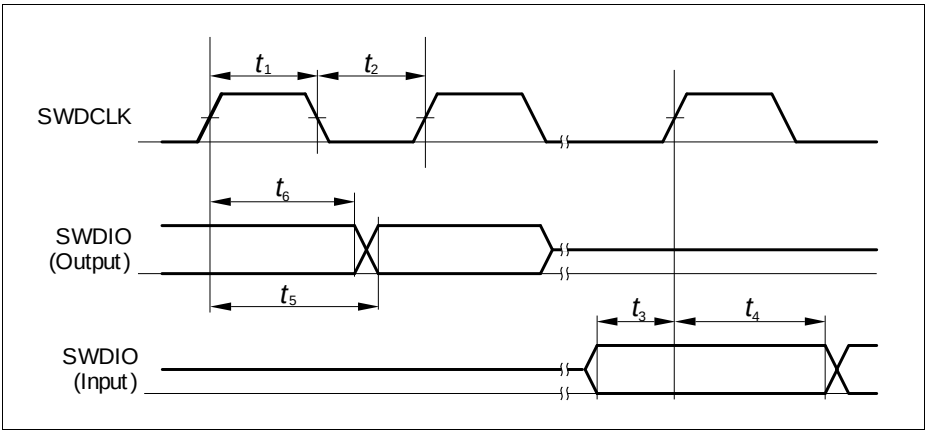

Figure 15 SWD Timing

Table 28 USIC IIC Fast Mode Timing [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

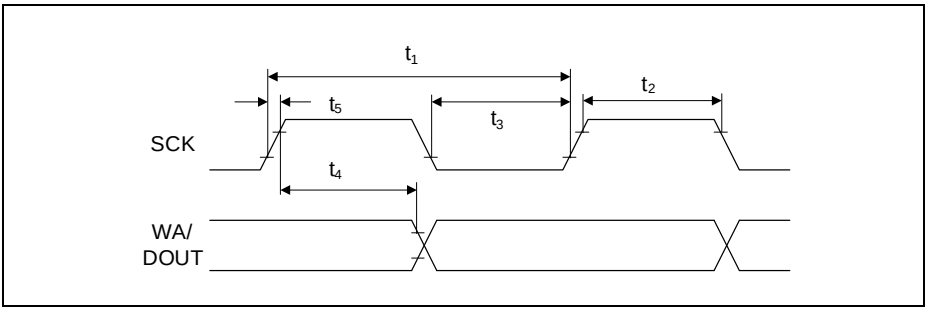

Figure 18 USIC IIS Master Transmitter Timing

Table 30 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	0.35 x t_{6min}	-	-	ns	
Clock Low	t_8 SR	0.35 x t_{6min}	-	-	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	-	-	ns	
Hold time	t_{10} SR	10	-	-	ns	

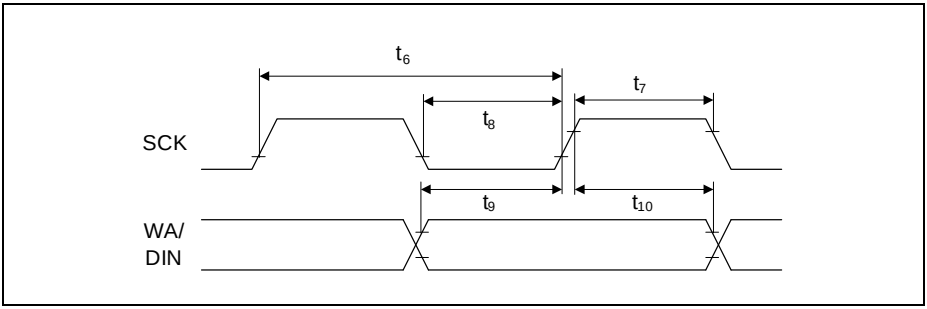

Figure 19 USIC IIS Slave Receiver Timing

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

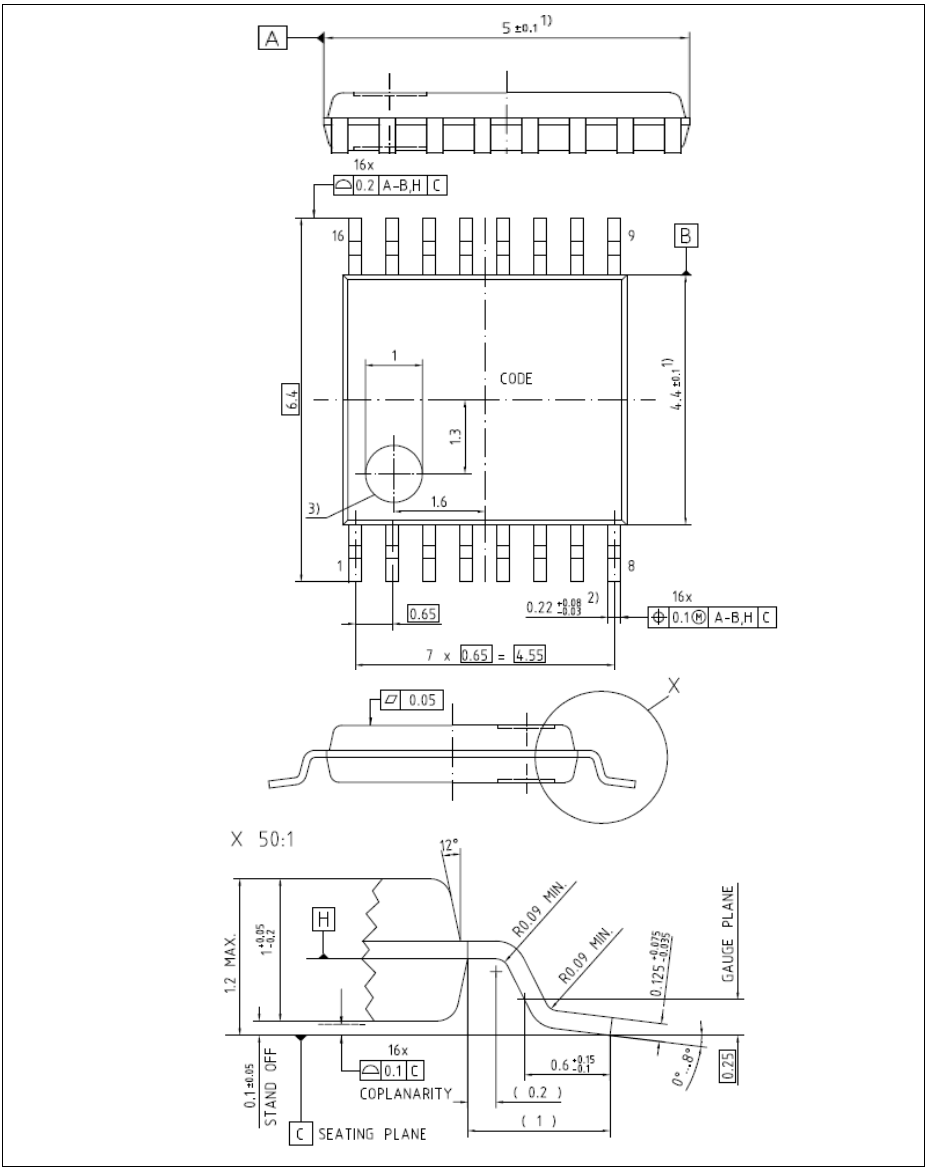

Figure 21 PG-TSSOP-16-8