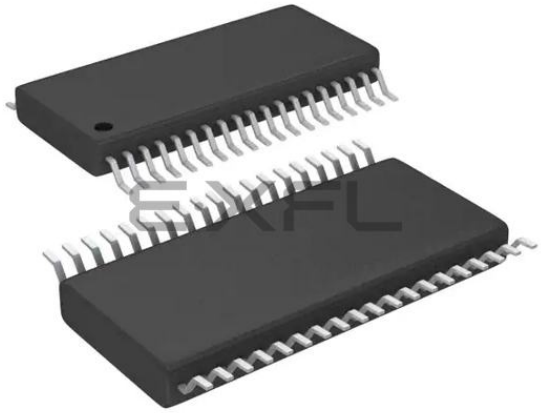
Infineon Technologies - XMC1301T038F0032AAXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301t038f0032aaxuma1

1 Summary of Features

The XMC1300 devices are members of the XMC1000 family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1300 series addresses the real-time control needs of motor control, digital power conversion. It also features peripherals for LED Lighting applications.

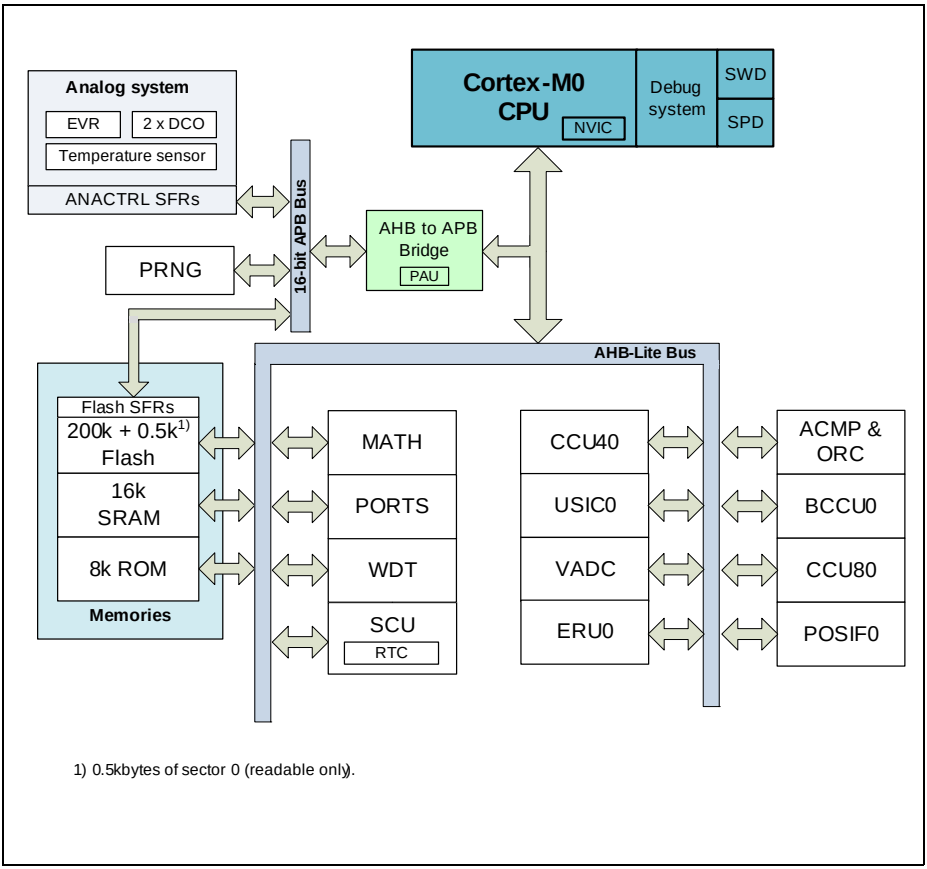

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M0 CPU
  - Most of 16-bit Thumb instruction set

  - Subset of 32-bit Thumb2 instruction set
  - High code density with 32-bit performance
  - Single cycle 32-bit hardware multiplier
  - System timer (SysTick) for Operating System support
  - Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- MATH Co-processor (MATH), consists of a CORDIC unit for trigonometric calculation and a division unit

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 200 kbytes on-chip Flash program and data memory

Communication Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces

Analog Frontend Peripherals

- A/D Converters, up to 12 channels, includes 2 sample and hold stages and a fast 12-bit analog to digital converter with adjustable gain
- Up to 8 channels of out of range comparators (ORC)
- Up to 3 fast analog comparators (ACMP)
- Temperature Sensor (TSE)

Industrial Control Peripherals

- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Position Interfaces (POSIF) for hall and quadrature encoders and motor positioning
- Brightness and Colour Control Unit (BCCU), for LED color and dimming application

System Control

- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG), provides random data with fast generation times

Input/Output Lines

- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

On-Chip Debug Support

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - T: TSSOP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1300 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1300 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC1300** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC1300 **Device Types**

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1301-T016F0008	PG-TSSOP-16-8	8	16
XMC1301-T016F0016	PG-TSSOP-16-8	16	16
XMC1301-T016X0008	PG-TSSOP-16-8	8	16
XMC1301-T016X0016	PG-TSSOP-16-8	16	16

2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 8 Port I/O Functions (cont'd)

Function	Outputs									Inputs										
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input	Input
P1.6	VADC0. EMUX12	USIC0_CH1 .DOUT0		USIC0_CH0 .SCLKOUT	BCCU0. OUT2	USIC0_CH0 .SELO2	USIC0_CH1 .SELO3							USIC0_CH0 .DX5F						
P2.0	ERU0. PDOUT3	CCU40. OUT0	ERU0. GOUT3		CCU80. OUT20	USIC0_CH0 .DOUT0	USIC0_CH0 .SCLKOUT						VADC0. G0CH5		ERU0.0B0	USIC0_CH0 .DX0E	USIC0_CH0 .DX1E	USIC0_CH1 .DX2F			
P2.1	ERU0. PDOUT2	CCU40. OUT1	ERU0. GOUT2		CCU80. OUT21	USIC0_CH0 .DOUT0	USIC0_CH1 .SCLKOUT					ACMP2.INP	VADC0. G0CH6		ERU0.1B0	USIC0_CH0 .DX0F	USIC0_CH1 .DX3A	USIC0_CH1 .DX4A			
P2.2												ACMP2.INN	VADC0. G0CH7		ERU0.0B1	USIC0_CH0 .DX3A	USIC0_CH0 .DX4A	USIC0_CH1 .DX5A	ORC0.AIN		
P2.3													VADC0. G1CH5		ERU0.1B1	USIC0_CH0 .DX5B	USIC0_CH1 .DX3C	USIC0_CH1 .DX4C	ORC1.AIN		
P2.4													VADC0. G1CH6		ERU0.0A1	USIC0_CH0 .DX3B	USIC0_CH0 .DX4B	USIC0_CH1 .DX5B	ORC2.AIN		
P2.5													VADC0. G1CH7		ERU0.1A1	USIC0_CH0 .DX5D	USIC0_CH1 .DX3E	USIC0_CH1 .DX4E	ORC3.AIN		
P2.6												ACMP1.INN	VADC0. G0CH0		ERU0.2A1	USIC0_CH0 .DX3E	USIC0_CH0 .DX4E	USIC0_CH1 .DX5D	ORC4.AIN		
P2.7												ACMP1.INP	VADC0. G1CH1		ERU0.3A1	USIC0_CH0 .DX5C	USIC0_CH1 .DX3D	USIC0_CH1 .DX4D	ORC5.AIN		
P2.8												ACMP0.INN	VADC0. G0CH1	VADC0. G1CH0	ERU0.3B1	USIC0_CH0 .DX3D	USIC0_CH0 .DX4D	USIC0_CH1 .DX5C	ORC6.AIN		
P2.9												ACMP0.INP	VADC0. G0CH2	VADC0. G1CH4	ERU0.3B0	USIC0_CH0 .DX5A	USIC0_CH1 .DX3B	USIC0_CH1 .DX4B	ORC7.AIN		
P2.10	ERU0. PDOUT1	CCU40. OUT2	ERU0. GOUT1		CCU80. OUT30	ACMP0. OUT	USIC0_CH1 .DOUT0						VADC0. G0CH3	VADC0. G1CH2	ERU0.2B0	USIC0_CH0 .DX3C	USIC0_CH0 .DX4C	USIC0_CH1 .DX0F			
P2.11	ERU0. PDOUT0	CCU40. OUT3	ERU0. GOUT0		CCU80. OUT31	USIC0_CH1 .SCLKOUT	USIC0_CH1 .DOUT0					ACMP.REF	VADC0. G0CH4	VADC0. G1CH3	ERU0.2B1	USIC0_CH1 .DX0E	USIC0_CH1 .DX1E				

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 9 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_S	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on any pin with respect to V_{SSP}	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Voltage on any analog input pin with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	–
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	SR	–	–	50	mA	–
Analog comparator input voltage	V_{CM}	SR	-0.3	–	V_{DDP} + 0.3	V	

3.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1300. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 10 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	105	°C	Temp. Range X
Digital supply voltage[1)]	V_{DDP} SR	1.8	–	5.5	V	
MCLK Frequency	f_{MCLK} CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	f_{PCLK} CC	–	–	66.4	MHz	Peripherals clock

1) See also the Supply Monitoring thresholds, **Chapter 3.3.3**.

Table 11 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current into V_{DDP} (TSSOP16, VQFN24)	I_{MVDD1}	SR	–	130	mA	3)
Maximum current into V_{DDP} (TSSOP38, VQFN40)	I_{MVDD2}	SR	–	260	mA	3)
Maximum current out of V_{SS} (TSSOP16, VQFN24)	I_{MVSS1}	SR	–	130	mA	3)
Maximum current out of V_{SS} (TSSOP38, VQFN40)	I_{MVSS2}	SR	–	260	mA	3)

1) Not subject to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

3) Not subject to production test, verified by design/characterization.

4) Not subject to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

Table 12 ADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC		1		–	GNCTRxz.GAINy = 00_B (unity gain)
			3		–	GNCTRxz.GAINy = 01_B (gain g1)
			6		–	GNCTRxz.GAINy = 10_B (gain g2)
			12		–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	3	–	–	1 / f_{ADC}	V_{DDP} = 5.0 V
		3	–	–	1 / f_{ADC}	V_{DDP} = 3.3 V
		30	–	–	1 / f_{ADC}	V_{DDP} = 1.8 V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	µs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC		9		1 / f_{ADC}	2)
Conversion time in 12-bit mode	t_{C12} CC		20		1 / f_{ADC}	2)
Maximum sample rate in 12-bit mode 3)	f_{C12} CC	–	–	f_{ADC} / 42.5	–	1 sample pending
		–	–	f_{ADC} / 62.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC		18		1 / f_{ADC}	2)
Maximum sample rate in 10-bit mode 3)	f_{C10} CC	–	–	f_{ADC} / 40.5	–	1 sample pending
		–	–	f_{ADC} / 58.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC		16		1 / f_{ADC}	2)

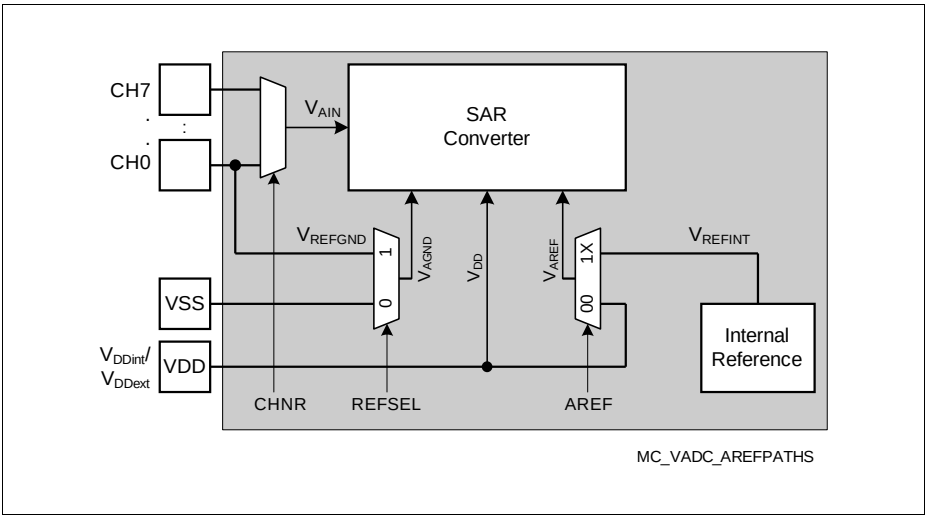

Figure 8 ADC Voltage Supply

3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 13 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; V_{DDP} = 3.0 V - 5.5 V; C_L = 0.25 pF)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	60	–	120	mV	$V_{AIN} \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	25	–	V_{ODC}	mV	
Always detected Overvoltage Pulse	t_{OPDD}	CC	103	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			88	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	21	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			–	–	11	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Detection Delay	t_{ODD}	CC	39	–	132	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			31	–	121	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Release Delay	t_{ORD}	CC	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 5 V
			57	–	340	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 3.3 V
Enable Delay	t_{OED}	CC	–	–	300	ns	ORCCTRL.ENORCx = 1

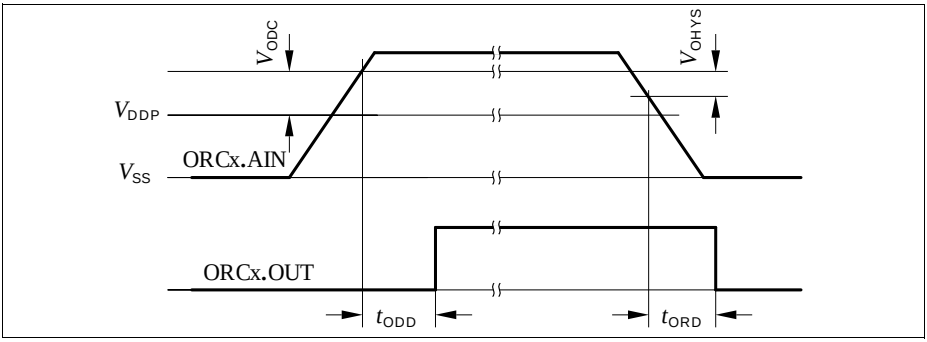

Figure 9 ORCx.OUT Trigger Generation

3.2.5 Temperature Sensor Characteristics

Table 15 Temperature Sensor Characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy[2)]	T_{TSAL} CC	–	+/-20	–	°C	T_J = -40 °C
		–	+/-12	–	°C	T_J = -25 °C
		-5	–	5	°C	T_J = 0 °C
		-2	–	2	°C	T_J = 25 °C
		-4	–	4	°C	T_J = 70 °C
		-2	–	2	°C	T_J = 115 °C

1) Not subject to production test, verified by design/characterization.

2) The temperature sensor accuracy is independent of the supply voltage.

3.2.6 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Table 16 Power Supply Parameters[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[2)]	Max.		
Active mode current[3)]	I_{DDPA} CC	–	9.2	12	mA	f_{MCLK} = 32 MHz f_{PCLK} = 64 MHz
		–	4	–	mA	f_{MCLK} = 1 MHz f_{PCLK} = 1 MHz
Sleep mode current Peripherals clock enabled[4)]	I_{DDPSE} CC	–	6.6	–	mA	f_{MCLK} = 32 MHz f_{PCLK} = 64 MHz
Sleep mode current Peripherals clock disabled[5)]	I_{DDPSD} CC	–	1.2	–	mA	f_{MCLK} = 1 MHz f_{PCLK} = 1 MHz
Deep Sleep mode current[6)]	I_{DDPDS} CC	–	0.24	–	mA	
Wake-up time from Sleep to Active mode[7)]	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[8)]	t_{DSA} CC	–	280	–	µsec	

1) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
2) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V.
3) CPU and all peripherals clock enabled, Flash is in active mode.
4) CPU is sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU is sleep, Flash is powered down and code executed from RAM after wake-up.
6) CPU is sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
7) CPU is sleep, Flash is in active mode during sleep mode.
8) CPU is sleep, Flash is in power down mode during deep sleep mode.

3.2.7 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 18 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per page	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	t_{PSER} CC	102	152	204	µs	
Wake-Up time	t_{WU} CC	–	32.2	–	µs	
Read time per word	t_a CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States [1]	$N_{WSFLASH}$ CC	0	0.5	–		f_{MCLK} = 8 MHz
		0	1.4	–		f_{MCLK} = 16 MHz
		1	1.9	–		f_{MCLK} = 32 MHz
Erase Cycles per page	N_{ECYC} CC	–	–	$5*10^4$	cycles	
Total Erase Cycles	N_{TECYC} CC	–	–	$2*10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

4) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

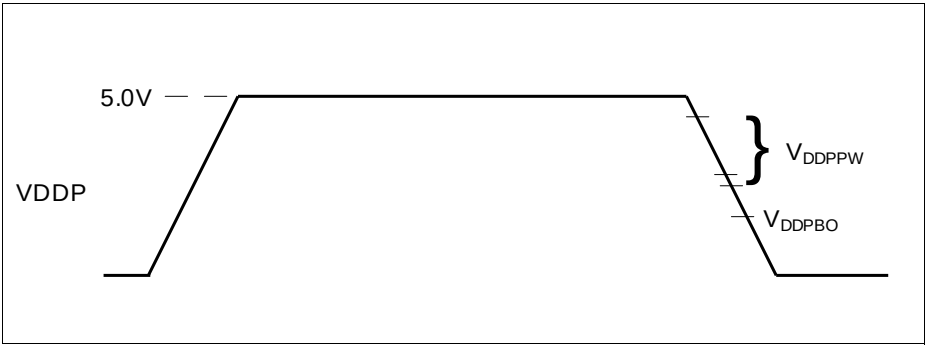

Figure 13 Supply Threshold Parameters

Figure 14 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

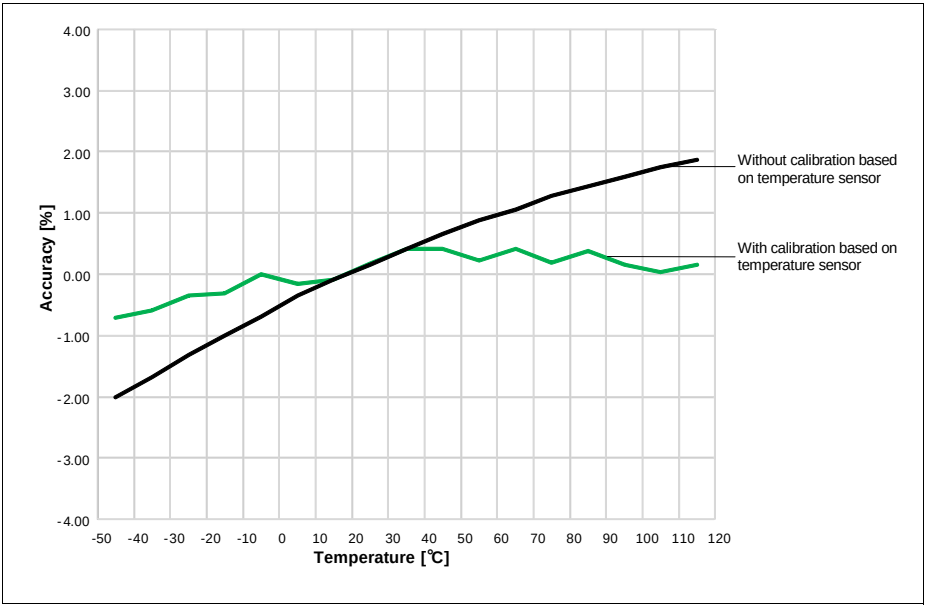

Figure 14 Typical DCO1 accuracy over temperature

Table 22 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1300.

Table 22 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	32.5	32.75	33	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)[2]
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)[2]

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	–	500000	ns	–
SWDCLK low time	t_2 SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5 CC	–	–	68	ns	C_L = 50 pF
		–	–	62	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	–	–	ns	

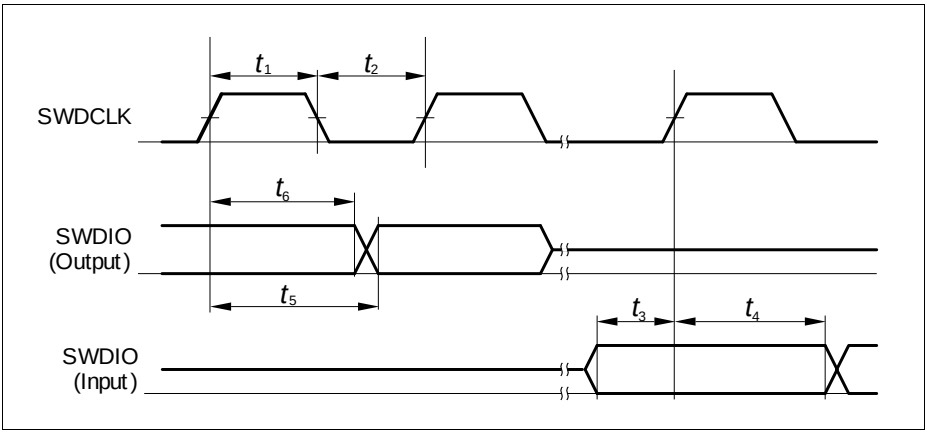

Figure 15 SWD Timing

3.3.7 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.7.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 25 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	0	–	–	ns	

Table 26 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10}	SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11}	SR	10	–	–	ns	

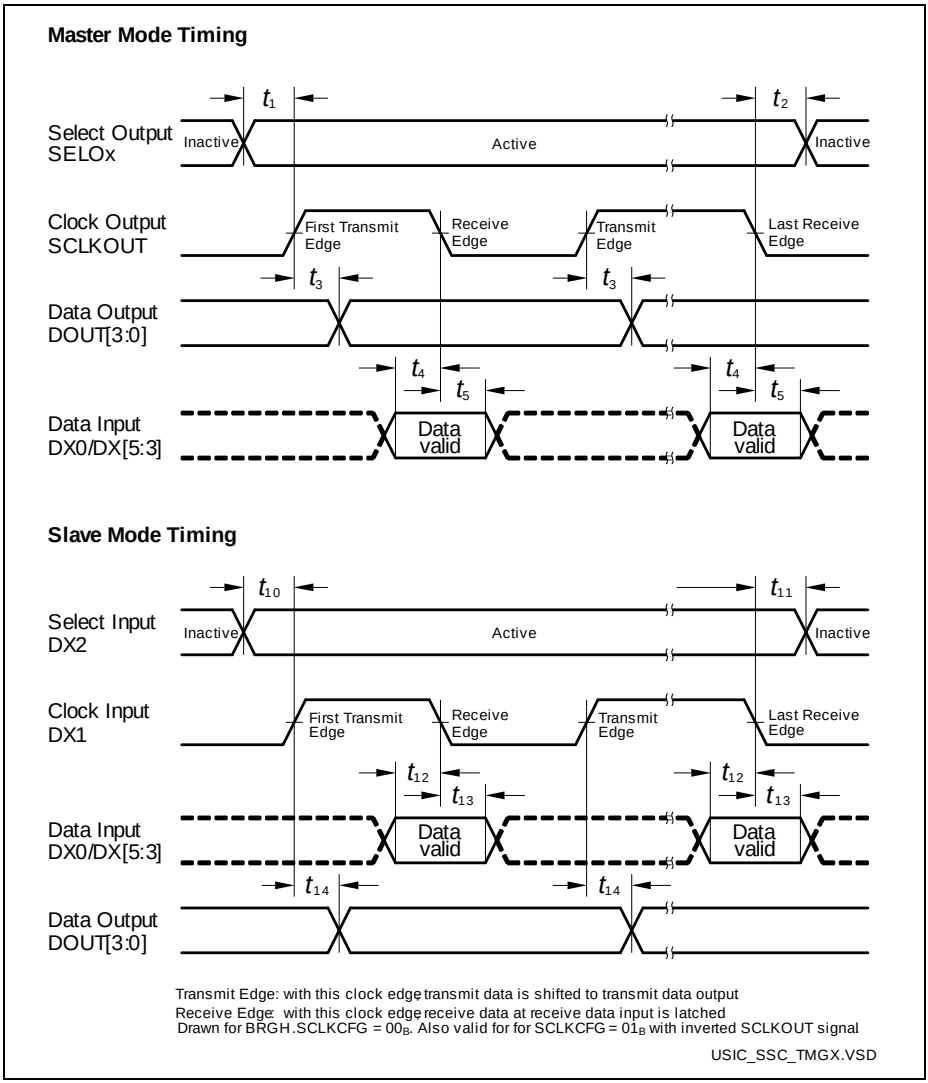

Figure 16 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.