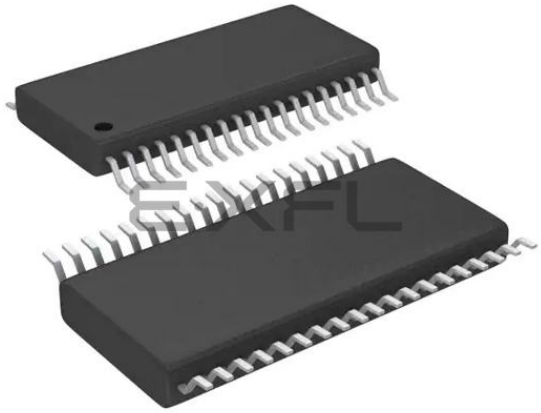
Infineon Technologies - XMC1301T038F0064AAXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301t038f0064aaxuma1

XMC1300

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex™-M0
32-bit processor core

Data Sheet

V1.4 2014-05

Microcontrollers

XMC1300 Data Sheet

Revision History: V1.4 2014-05

Previous Version: V1.3	
Page	Subjects
Page 12	ADC channels of Table 2 is updated. Table 3 is added.
Page 12	Description for Chip Identification Number of Section 1.4 is updated.
Page 20	The pad type is corrected for P1.6 in Table 6.
Page 32	The t_{C12} , f_{C12}, t_{C10}, f_{C10}, t_{C8} and f_{C8} parameters are updated in Table 12.
Page 35	Figure 8 is added.
Page 38	The t_{SR} and t_{TSAL} parameters are updated in Table 15.
Page 41	Parameter name for t_{PSER} is updated. The $N_{WSFLASH}$ parameter and test condition for t_{RET} are added to Table 18.
Page 44	The min value for V_{DDPBO} parameter is added to Table 20. Footnote 1 is updated.
Page 46	The Δf_{LTT} parameter is added to Table 21.
Page 47	Figure 14 is added.

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About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1300 series devices.

The document describes the characteristics of a superset of the XMC1300 series devices. For simplicity, the various device types are referred to by the collective term XMC1300 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc1000** to get access to the latest versions of those documents.

Input/Output Lines

- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

On-Chip Debug Support

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - T: TSSOP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1300 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1300 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC1300** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC1300 **Device Types**

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1301-T016F0008	PG-TSSOP-16-8	8	16
XMC1301-T016F0016	PG-TSSOP-16-8	16	16
XMC1301-T016X0008	PG-TSSOP-16-8	8	16
XMC1301-T016X0016	PG-TSSOP-16-8	16	16

Table 2 Features of XMC1300 Device Types[1)]

Derivative	ADC channel	ACMP	BCCU	MATH
XMC1301-T016	11	2	-	-
XMC1302-T016	11	2	1	1
XMC1301-T038	16	3	-	-
XMC1302-T038	16	3	1	1
XMC1301-Q024	13	3	-	-
XMC1302-Q024	13	3	1	1
XMC1301-Q040	16	3	-	-
XMC1302-Q040	16	3	1	1

1) Features that are not included in this table are available in all the derivatives

Table 3 ADC Channels [1)]

Package	VADC0 G0	VADC0 G1
PG-TSSOP-16	CH0..CH5	CH0..CH4
PG-TSSOP-28	CH0..CH7	CH0 .. CH4, CH7
PG-TSSOP-38	CH0..CH7	CH0..CH7
PG-VQFN-24	CH0..CH7	CH0..CH4
PG-VQFN-40	CH0..CH7	CH1, CH5 .. CH7

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 $0F00_H$ (MSB) - 1000 $0F1B_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 4 XMC1300 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1302-Q024F0016	00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1302-Q024F0032	00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1302-Q024F0064	00013062 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1302-Q024X0016	00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1302-Q024X0032	00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1302-Q024X0064	00013063 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1301-Q040F0008	00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083$_H$	AA
XMC1301-Q040F0016	00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1301-Q040F0032	00013042 01CF00FF 00001FF7 0000100F 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1302-Q040X0016	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1302-Q040X0032	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1302-Q040X0064	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1302-Q040X0128	00013043 01FF00FF 00001FF7 0000900F 00000B00 00001000 00021000 101ED083$_H$	AA

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

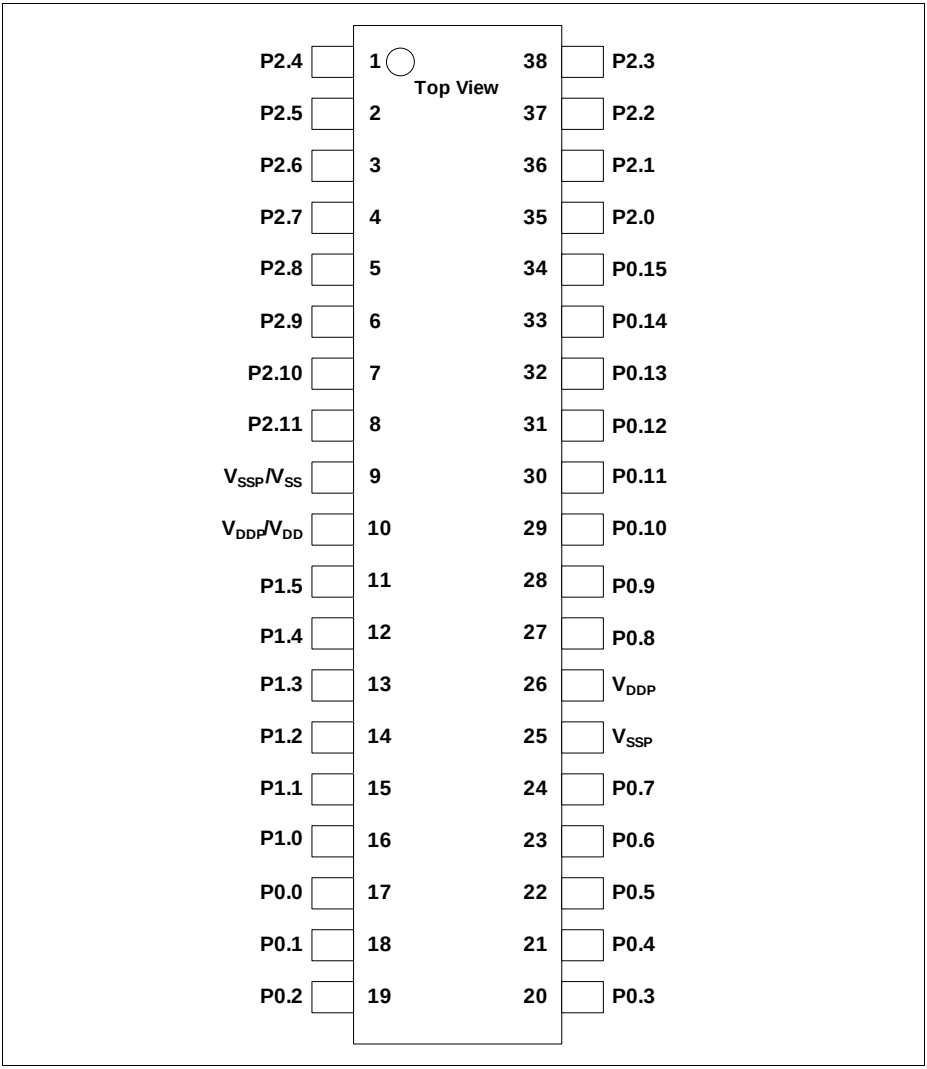

Figure 4 XMC1300 PG-TSSOP-38 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 5 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT(standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	15	7	STD_INOUT	
P0.1	24	18	-	-	STD_INOUT	
P0.2	25	19	-	-	STD_INOUT	
P0.3	26	20	-	-	STD_INOUT	
P0.4	27	21	-	-	STD_INOUT	
P0.5	28	22	16	8	STD_INOUT	
P0.6	29	23	17	9	STD_INOUT	
P0.7	30	24	18	10	STD_INOUT	
P0.8	33	27	19	11	STD_INOUT	
P0.9	34	28	20	12	STD_INOUT	
P0.10	35	29	-	-	STD_INOUT	
P0.11	36	30	-	-	STD_INOUT	
P0.12	37	31	21	-	STD_INOUT	

2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 8 Port I/O Functions (cont'd)

Function	Outputs									Inputs										
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input	Input
P1.6	VADC0. EMUX12	USIC0_CH1 .DOUT0		USIC0_CH0 .SCLKOUT	BCCU0. OUT2	USIC0_CH0 .SELO2	USIC0_CH1 .SELO3							USIC0_CH0 .DX5F						
P2.0	ERU0. PDOUT3	CCU40. OUT0	ERU0. GOUT3		CCU80. OUT20	USIC0_CH0 .DOUT0	USIC0_CH0 .SCLKOUT						VADC0. G0CH5		ERU0.0B0	USIC0_CH0 .DX0E	USIC0_CH0 .DX1E	USIC0_CH1 .DX2F			
P2.1	ERU0. PDOUT2	CCU40. OUT1	ERU0. GOUT2		CCU80. OUT21	USIC0_CH0 .DOUT0	USIC0_CH1 .SCLKOUT					ACMP2.INP	VADC0. G0CH6		ERU0.1B0	USIC0_CH0 .DX0F	USIC0_CH1 .DX3A	USIC0_CH1 .DX4A			
P2.2												ACMP2.INN	VADC0. G0CH7		ERU0.0B1	USIC0_CH0 .DX3A	USIC0_CH0 .DX4A	USIC0_CH1 .DX5A	ORC0.AIN		
P2.3													VADC0. G1CH5		ERU0.1B1	USIC0_CH0 .DX5B	USIC0_CH1 .DX3C	USIC0_CH1 .DX4C	ORC1.AIN		
P2.4													VADC0. G1CH6		ERU0.0A1	USIC0_CH0 .DX3B	USIC0_CH0 .DX4B	USIC0_CH1 .DX5B	ORC2.AIN		
P2.5													VADC0. G1CH7		ERU0.1A1	USIC0_CH0 .DX5D	USIC0_CH1 .DX3E	USIC0_CH1 .DX4E	ORC3.AIN		
P2.6												ACMP1.INN	VADC0. G0CH0		ERU0.2A1	USIC0_CH0 .DX3E	USIC0_CH0 .DX4E	USIC0_CH1 .DX5D	ORC4.AIN		
P2.7												ACMP1.INP	VADC0. G1CH1		ERU0.3A1	USIC0_CH0 .DX5C	USIC0_CH1 .DX3D	USIC0_CH1 .DX4D	ORC5.AIN		
P2.8												ACMP0.INN	VADC0. G0CH1	VADC0. G1CH0	ERU0.3B1	USIC0_CH0 .DX3D	USIC0_CH0 .DX4D	USIC0_CH1 .DX5C	ORC6.AIN		
P2.9												ACMP0.INP	VADC0. G0CH2	VADC0. G1CH4	ERU0.3B0	USIC0_CH0 .DX5A	USIC0_CH1 .DX3B	USIC0_CH1 .DX4B	ORC7.AIN		
P2.10	ERU0. PDOUT1	CCU40. OUT2	ERU0. GOUT1		CCU80. OUT30	ACMP0. OUT	USIC0_CH1 .DOUT0						VADC0. G0CH3	VADC0. G1CH2	ERU0.2B0	USIC0_CH0 .DX3C	USIC0_CH0 .DX4C	USIC0_CH1 .DX0F			
P2.11	ERU0. PDOUT0	CCU40. OUT3	ERU0. GOUT0		CCU80. OUT31	USIC0_CH1 .SCLKOUT	USIC0_CH1 .DOUT0					ACMP.REF	VADC0. G0CH4	VADC0. G1CH3	ERU0.2B1	USIC0_CH1 .DX0E	USIC0_CH1 .DX1E				

3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1300.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1300 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1300 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1300 is designed in.

3.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1300. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 10 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	105	°C	Temp. Range X
Digital supply voltage[1)]	V_{DDP} SR	1.8	–	5.5	V	
MCLK Frequency	f_{MCLK} CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	f_{PCLK} CC	–	–	66.4	MHz	Peripherals clock

1) See also the Supply Monitoring thresholds, **Chapter 3.3.3**.

3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 13 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; V_{DDP} = 3.0 V - 5.5 V; C_L = 0.25 pF)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	60	–	120	mV	$V_{AIN} \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	25	–	V_{ODC}	mV	
Always detected Overvoltage Pulse	t_{OPDD}	CC	103	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			88	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	21	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			–	–	11	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Detection Delay	t_{ODD}	CC	39	–	132	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			31	–	121	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Release Delay	t_{ORD}	CC	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 5 V
			57	–	340	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 3.3 V
Enable Delay	t_{OED}	CC	–	–	300	ns	ORCCTRL.ENORCx = 1

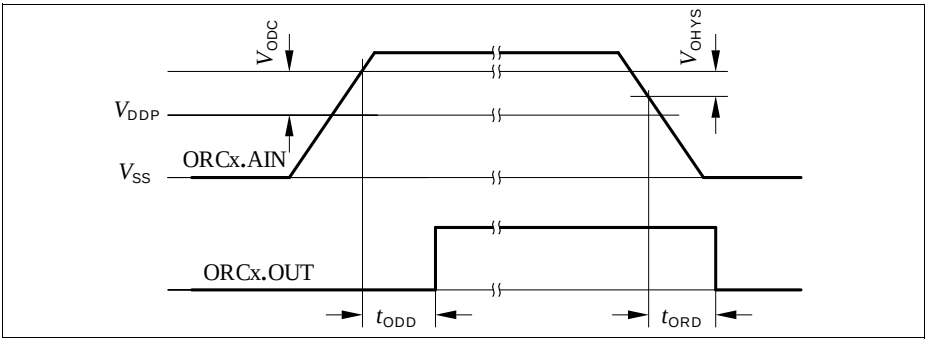

Figure 9 ORCx.OUT Trigger Generation

3.2.5 Temperature Sensor Characteristics

Table 15 Temperature Sensor Characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy[2)]	T_{TSAL} CC	–	+/-20	–	°C	T_J = -40 °C
		–	+/-12	–	°C	T_J = -25 °C
		-5	–	5	°C	T_J = 0 °C
		-2	–	2	°C	T_J = 25 °C
		-4	–	4	°C	T_J = 70 °C
		-2	–	2	°C	T_J = 115 °C

1) Not subject to production test, verified by design/characterization.

2) The temperature sensor accuracy is independent of the supply voltage.

3.3 AC Parameters

3.3.1 Testing Waveforms

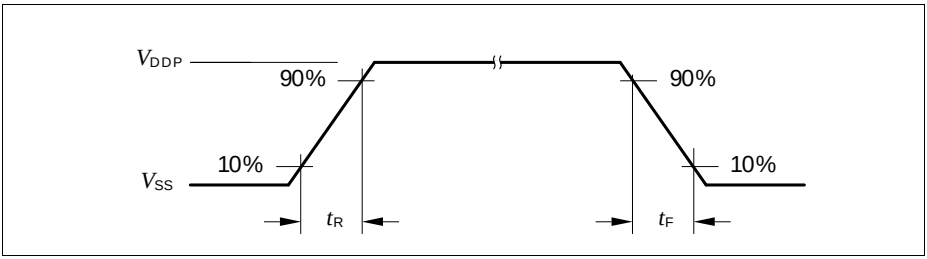

Figure 10 Rise/Fall Time Parameters

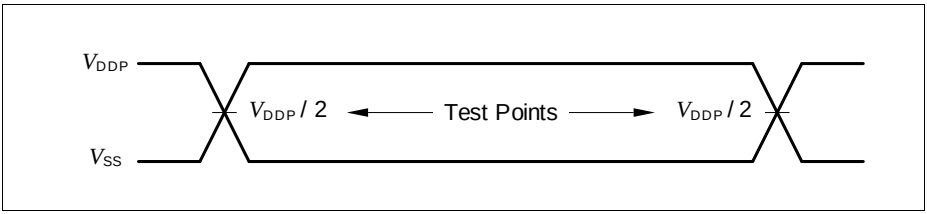

Figure 11 Testing Waveform, Output Delay

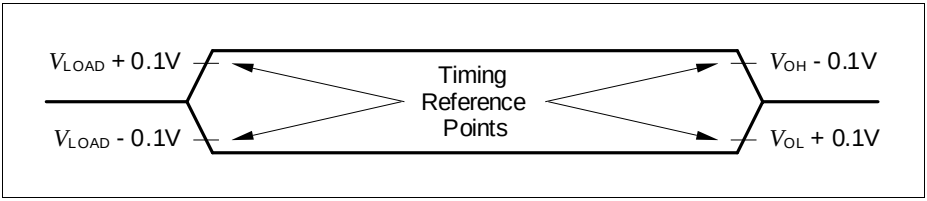

Figure 12 Testing Waveform, Output High Impedance

3.3.6 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 24 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

Table 26 USIC SSC Slave Mode Timing (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

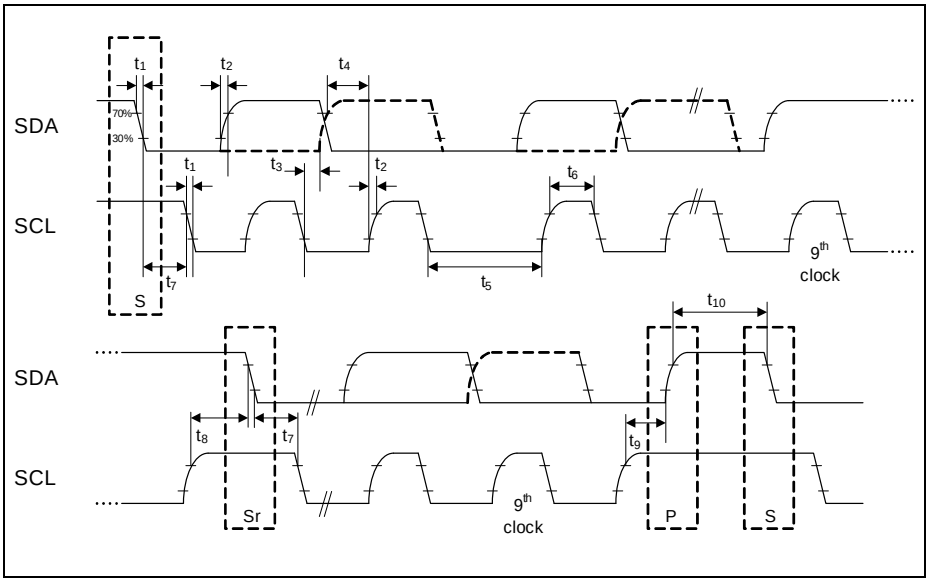

Figure 17 USIC IIC Stand and Fast Mode Timing

3.3.7.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 29 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$2/f_{MCLK}$	-	-	ns	$V_{DDP} \geq 3$ V
		$4/f_{MCLK}$	-	-	ns	$V_{DDP} < 3$ V
Clock HIGH	t_2 CC	0.35 x t_{1min}	-	-	ns	
Clock Low	t_3 CC	0.35 x t_{1min}	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	0.15 x t_{1min}	ns	

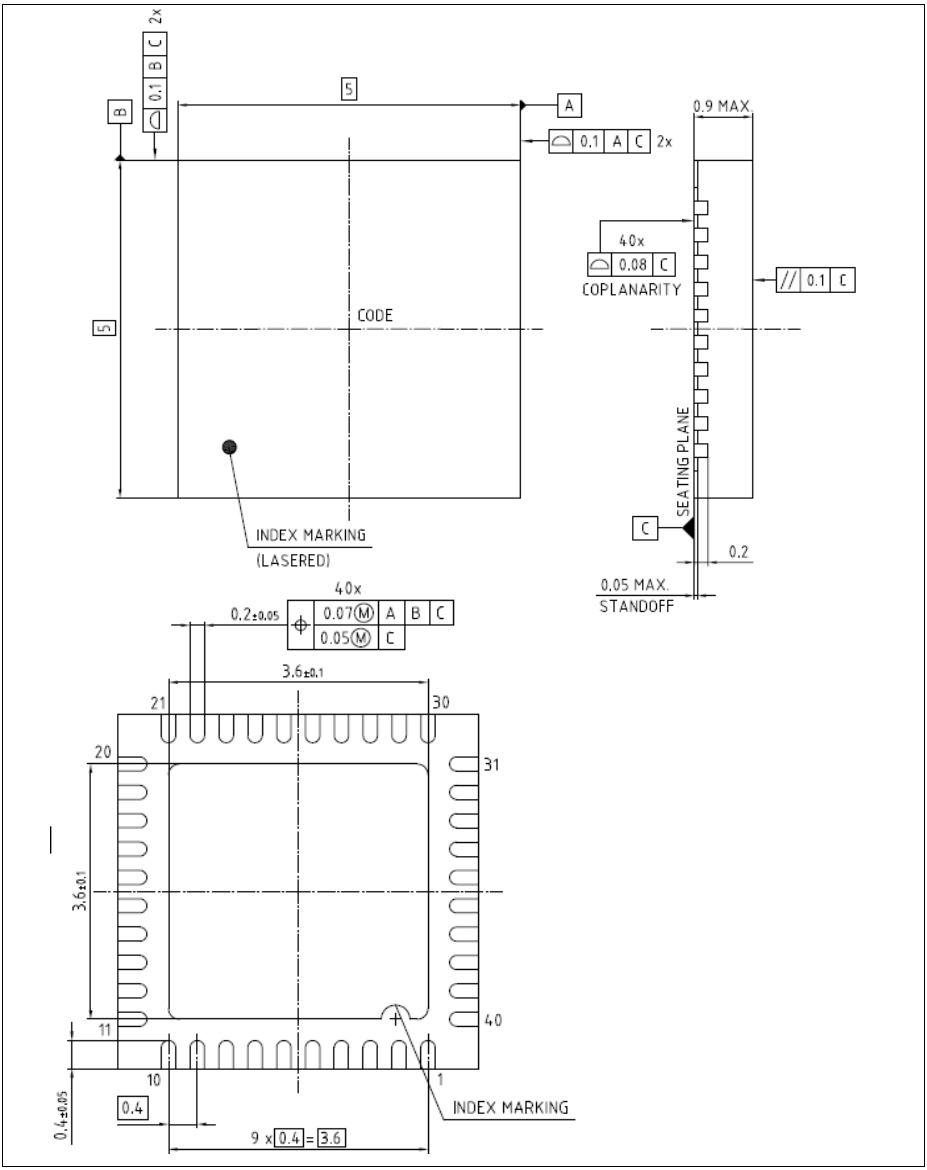

Figure 23 PG-VQFN-40-13

All dimensions in mm.

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