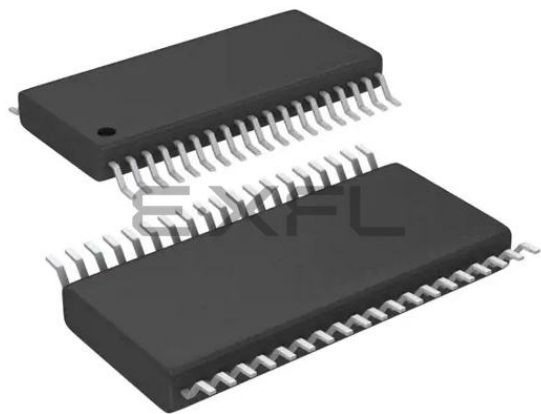




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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1302t038x0064aaxuma1

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Table 4 XMC1300 Chip Identification Number

Derivative	Value	Marking
XMC1301-T016F0008	00013032 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1301-T016F0016	00013032 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1301-T016X0008	00013033 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1301-T016X0016	00013033 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1302-T016X0008	00013033 01FF00FF 00001FF7 0000900F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1302-T016X0016	00013033 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1302-T016X0032	00013033 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1301-T038F0008	00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1301-T038F0016	00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1301-T038F0032	00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1302-T038X0016	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1302-T038X0032	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1302-T038X0064	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083 _H	AA
XMC1302-T038X0128	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00021000 101ED083 _H	AA
XMC1302-T038X0200	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00033000 101ED083 _H	AA
XMC1301-Q024F0008	00013062 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1301-Q024F0016	00013062 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083 _H	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

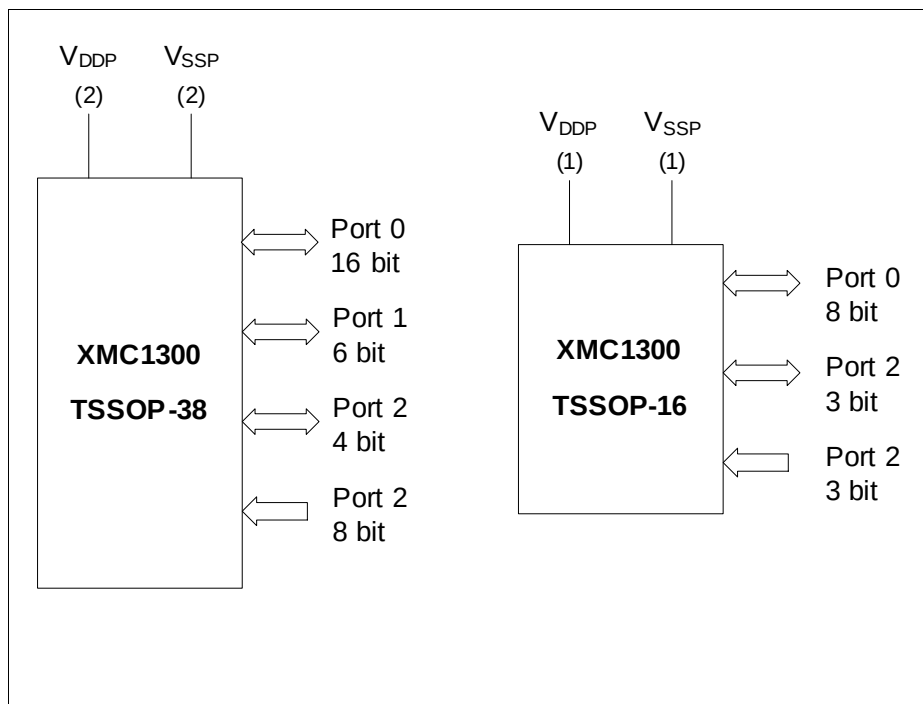


Figure 2 XMC1300 Logic Symbol for TSSOP-38 and TSSOP-16

2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOC.R.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 8 Port I/O Functions (cont'd)

Function	Outputs									Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P1.6	VADC0.EMUX12	USIC0_CH1.DOUT0		USIC0_CH0.SCLKOUT	BCCU0.OUT2	USIC0_CH0.SEL02	USIC0_CH1.SEL03							USIC0_CH0.DX5F					
P2.0	ERU0.PDOUT3	CCU40.OUT0	ERU0.GOUT3		CCU80.OUT20	USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT						VADC0.G0CH5		ERU0.0B0	USIC0_CH0.DX0E	USIC0_CH0.DX1E	USIC0_CH1.DX2F	
P2.1	ERU0.PDOUT2	CCU40.OUT1	ERU0.GOUT2		CCU80.OUT21	USIC0_CH0.DOUT0	USIC0_CH1.SCLKOUT					ACMP2.INP	VADC0.G0CH6		ERU0.1B0	USIC0_CH0.DX0F	USIC0_CH1.DX3A	USIC0_CH1.DX4A	
P2.2												ACMP2.INN	VADC0.G0CH7		ERU0.0B1	USIC0_CH0.DX3A	USIC0_CH0.DX4A	USIC0_CH1.DX5A	ORC0.AIN
P2.3													VADC0.G1CH5		ERU0.1B1	USIC0_CH0.DX5B	USIC0_CH1.DX3C	USIC0_CH1.DX4C	ORC1.AIN
P2.4													VADC0.G1CH6		ERU0.0A1	USIC0_CH0.DX3B	USIC0_CH0.DX4B	USIC0_CH1.DX5B	ORC2.AIN
P2.5													VADC0.G1CH7		ERU0.1A1	USIC0_CH0.DX5D	USIC0_CH1.DX3E	USIC0_CH1.DX4E	ORC3.AIN
P2.6												ACMP1.INN	VADC0.G0CH0		ERU0.2A1	USIC0_CH0.DX3E	USIC0_CH0.DX4E	USIC0_CH1.DX5D	ORC4.AIN
P2.7												ACMP1.INP	VADC0.G1CH1		ERU0.3A1	USIC0_CH0.DX5C	USIC0_CH1.DX3D	USIC0_CH1.DX4D	ORC5.AIN
P2.8												ACMP0.INN	VADC0.G0CH1	VADC0.G1CH0	ERU0.3B1	USIC0_CH0.DX3D	USIC0_CH0.DX4D	USIC0_CH1.DX5C	ORC6.AIN
P2.9												ACMP0.INP	VADC0.G0CH2	VADC0.G1CH4	ERU0.3B0	USIC0_CH0.DX5A	USIC0_CH1.DX3B	USIC0_CH1.DX4B	ORC7.AIN
P2.10	ERU0.PDOUT1	CCU40.OUT2	ERU0.GOUT1		CCU80.OUT30	ACMP0.OUT	USIC0_CH1.DOUT0						VADC0.G0CH3	VADC0.G1CH2	ERU0.2B0	USIC0_CH0.DX3C	USIC0_CH0.DX4C	USIC0_CH1.DX0F	
P2.11	ERU0.PDOUT0	CCU40.OUT3	ERU0.GOUT0		CCU80.OUT31	USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0					ACMP.REF	VADC0.G0CH4	VADC0.G1CH3	ERU0.2B1	USIC0_CH1.DX0E	USIC0_CH1.DX1E		

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 11 provides the characteristics of the input/output pins of the XMC1300.

Table 11 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC	–	1.0	V	$I_{OL} = 11 \text{ mA (5 V)}$ $I_{OL} = 7 \text{ mA (3.3 V)}$
			–	0.4	V	$I_{OL} = 5 \text{ mA (5 V)}$ $I_{OL} = 3.5 \text{ mA (3.3 V)}$
Output low voltage on high current pads	V_{OLP1}	CC	–	1.0	V	$I_{OL} = 50 \text{ mA (5 V)}$ $I_{OL} = 25 \text{ mA (3.3 V)}$
			–	0.32	V	$I_{OL} = 10 \text{ mA (5 V)}$
			–	0.4	V	$I_{OL} = 5 \text{ mA (3.3 V)}$
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	$V_{DDP} - 1.0$	–	V	$I_{OH} = -10 \text{ mA (5 V)}$ $I_{OH} = -7 \text{ mA (3.3 V)}$
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4.5 \text{ mA (5 V)}$ $I_{OH} = -2.5 \text{ mA (3.3 V)}$
Output high voltage on high current pads	V_{OHP1}	CC	$V_{DDP} - 0.32$	–	V	$I_{OH} = -6 \text{ mA (5 V)}$
			$V_{DDP} - 1.0$	–	V	$I_{OH} = -8 \text{ mA (3.3 V)}$
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4 \text{ mA (3.3 V)}$
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	$0.19 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	$0.7 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	V_{ILPL}	SR	–	$0.08 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V) ³⁾

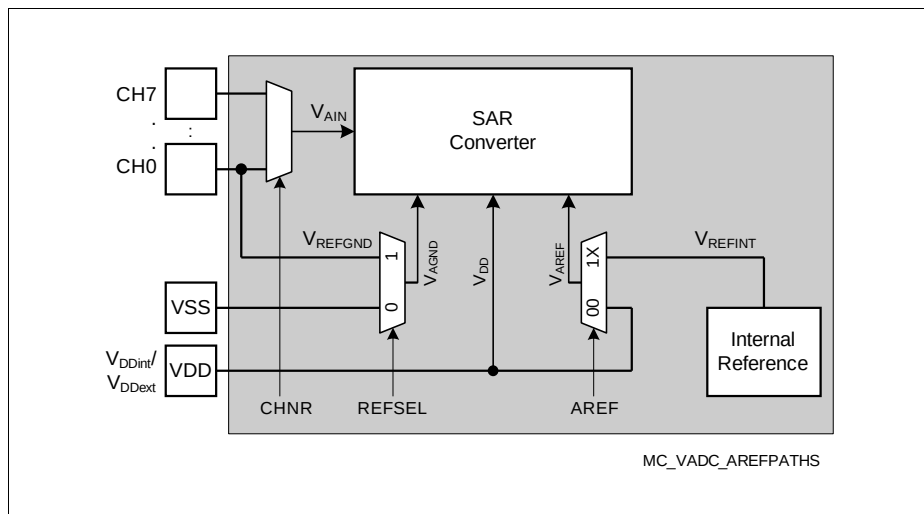


Figure 8 **ADC Voltage Supply**

3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 13 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; $V_{DDP} = 3.0\text{ V} - 5.5\text{ V}$; $C_L = 0.25\text{ pF}$)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	60	–	120	mV	$V_{AIN} \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	25	–	V_{ODC}	mV	
Always detected Overvoltage Pulse	t_{OPDD}	CC	103	–	–	ns	$V_{AIN} \geq V_{DDP} + 150\text{ mV}$
			88	–	–	ns	$V_{AIN} \geq V_{DDP} + 350\text{ mV}$
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	21	ns	$V_{AIN} \geq V_{DDP} + 150\text{ mV}$
			–	–	11	ns	$V_{AIN} \geq V_{DDP} + 350\text{ mV}$
Detection Delay	t_{ODD}	CC	39	–	132	ns	$V_{AIN} \geq V_{DDP} + 150\text{ mV}$
			31	–	121	ns	$V_{AIN} \geq V_{DDP} + 350\text{ mV}$
Release Delay	t_{ORD}	CC	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; $V_{DDP} = 5\text{ V}$
			57	–	340	ns	$V_{AIN} \leq V_{DDP}$; $V_{DDP} = 3.3\text{ V}$
Enable Delay	t_{OED}	CC	–	–	300	ns	ORCCTRL.ENORCx = 1

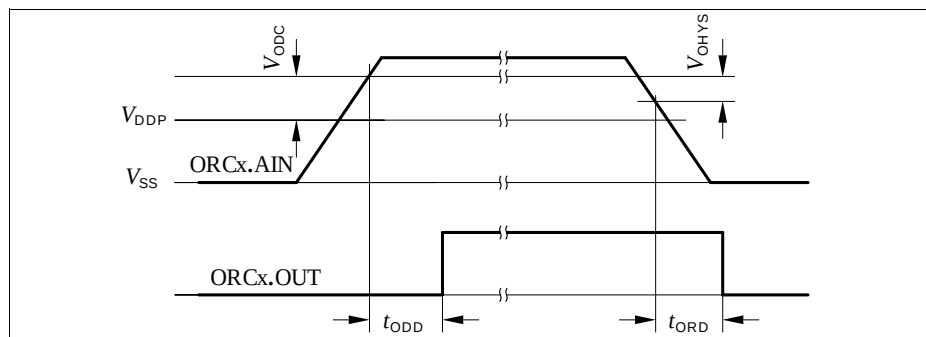


Figure 9 ORCx.OUT Trigger Generation

3.2.5 Temperature Sensor Characteristics

Table 15 Temperature Sensor Characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy ²⁾	T_{TSAL} CC	–	+/-20	–	°C	$T_J = -40\text{ °C}$
		–	+/-12	–	°C	$T_J = -25\text{ °C}$
		-5	–	5	°C	$T_J = 0\text{ °C}$
		-2	–	2	°C	$T_J = 25\text{ °C}$
		-4	–	4	°C	$T_J = 70\text{ °C}$
		-2	–	2	°C	$T_J = 115\text{ °C}$

1) Not subject to production test, verified by design/characterization.

2) The temperature sensor accuracy is independent of the supply voltage.

3.2.6 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Table 16 Power Supply Parameters¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ. ²⁾	Max.		
Active mode current ³⁾	I_{DDPA} CC	–	9.2	12	mA	$f_{MCLK} = 32$ MHz $f_{PCLK} = 64$ MHz
		–	4	–	mA	$f_{MCLK} = 1$ MHz $f_{PCLK} = 1$ MHz
Sleep mode current Peripherals clock enabled ⁴⁾	I_{DDPSE} CC	–	6.6	–	mA	$f_{MCLK} = 32$ MHz $f_{PCLK} = 64$ MHz
Sleep mode current Peripherals clock disabled ⁵⁾	I_{DDPSD} CC	–	1.2	–	mA	$f_{MCLK} = 1$ MHz $f_{PCLK} = 1$ MHz
Deep Sleep mode current ⁶⁾	I_{DDPDS} CC	–	0.24	–	mA	
Wake-up time from Sleep to Active mode ⁷⁾	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode ⁸⁾	t_{DSA} CC	–	280	–	μsec	

1) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.

2) The typical values are measured at $T_A = +25$ °C and $V_{DDP} = 5$ V.

3) CPU and all peripherals clock enabled, Flash is in active mode.

4) CPU is sleep, all peripherals clock enabled and Flash is in active mode.

5) CPU is sleep, Flash is powered down and code executed from RAM after wake-up.

6) CPU is sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.

7) CPU is sleep, Flash is in active mode during sleep mode.

8) CPU is sleep, Flash is in power down mode during deep sleep mode.

3.2.7 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 18 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per page	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	$t_{\text{PSE}}^{\text{CC}}$	102	152	204	μs	
Wake-Up time	t_{WU} CC	–	32.2	–	μs	
Read time per word	t_{a} CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States ¹⁾	N_{WSFLASH} CC	0	0.5	–		$f_{\text{MCLK}} = 8 \text{ MHz}$
		0	1.4	–		$f_{\text{MCLK}} = 16 \text{ MHz}$
		1	1.9	–		$f_{\text{MCLK}} = 32 \text{ MHz}$
Erase Cycles per page	N_{ECYC} CC	–	–	$5 \cdot 10^4$	cycles	
Total Erase Cycles	N_{TECYC} CC	–	–	$2 \cdot 10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3 AC Parameters

3.3.1 Testing Waveforms

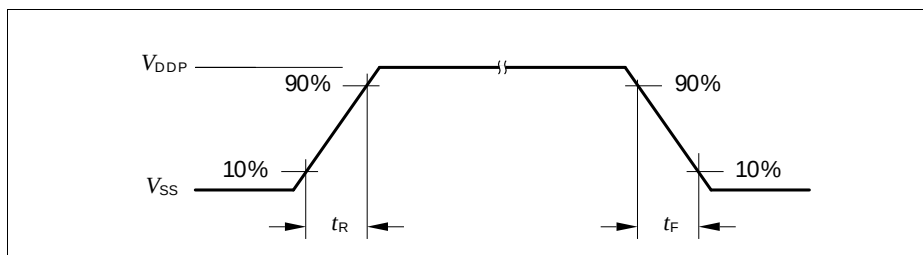


Figure 10 Rise/Fall Time Parameters

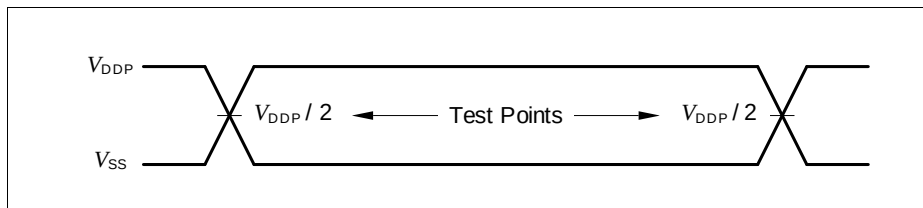


Figure 11 Testing Waveform, Output Delay

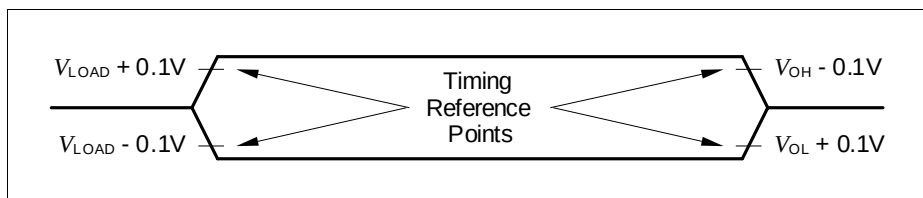


Figure 12 Testing Waveform, Output High Impedance

Electrical Parameter

- 3) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.
- 4) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

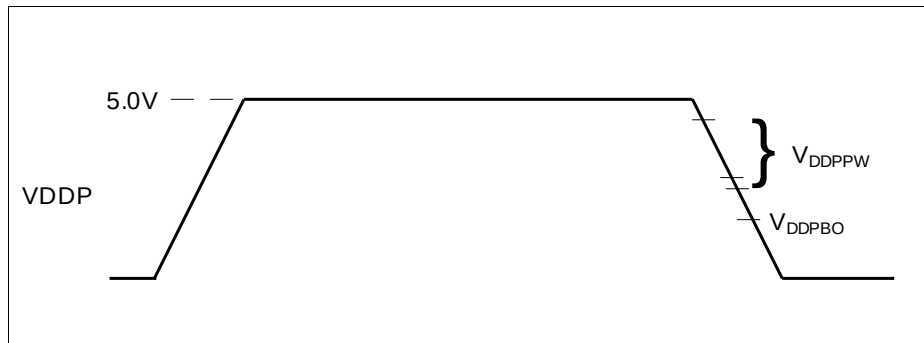


Figure 13 **Supply Threshold Parameters**

3.3.4 On-Chip Oscillator Characteristics

Table 21 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1300.

Table 21 64 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	63.5	64	64.5	MHz	under nominal conditions ¹⁾ after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature ($T_A = 0\text{ °C}$ to 85 °C) ²⁾
			-3.9	–	4.0	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature ($T_A = -40\text{ °C}$ to 105 °C) ²⁾
Accuracy with calibration based on temperature sensor	Δf_{LTT}	CC	-1.3	–	1.25	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature ($T_A = 0\text{ °C}$ to 105 °C) ²⁾
			-2.6	–	1.25	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature ($T_A = -40\text{ °C}$ to 105 °C) ²⁾

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and $T_A = +25\text{ °C}$.

2) Not subject to production test, verified by design/characterisation.

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	—	500000	ns	—
SWDCLK low time	t_2 SR	50	—	500000	ns	—
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	—	—	ns	—
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	—	—	ns	—
SWDIO output valid time after SWDCLK rising edge	t_5 CC	—	—	68	ns	$C_L = 50$ pF
		—	—	62	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	—	—	ns	

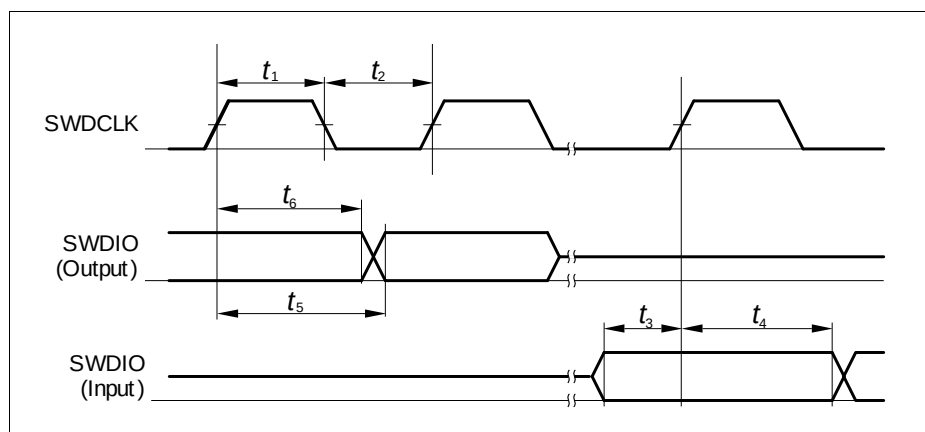


Figure 15 SWD Timing

3.3.7.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 27 USIC IIC Standard Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	μs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	μs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	μs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	μs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	μs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	μs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

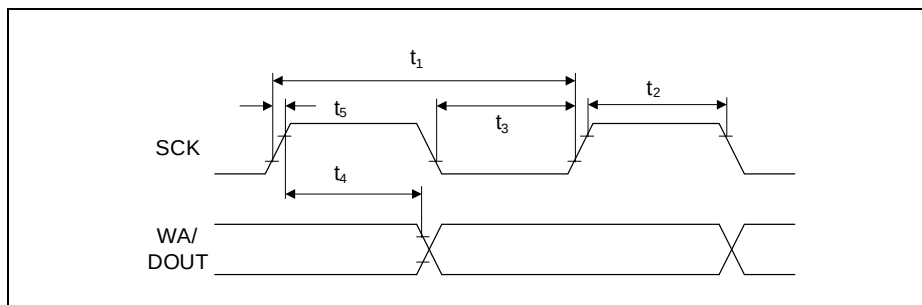


Figure 18 USIC IIS Master Transmitter Timing

Table 30 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	$0.35 \times t_{6min}$	-	-	ns	
Clock Low	t_8 SR	$0.35 \times t_{6min}$	-	-	ns	
Set-up time	t_9 SR	$0.2 \times t_{6min}$	-	-	ns	
Hold time	t_{10} SR	10	-	-	ns	

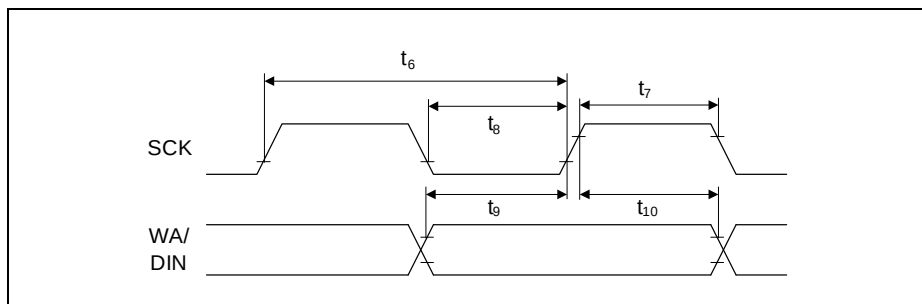


Figure 19 USIC IIS Slave Receiver Timing

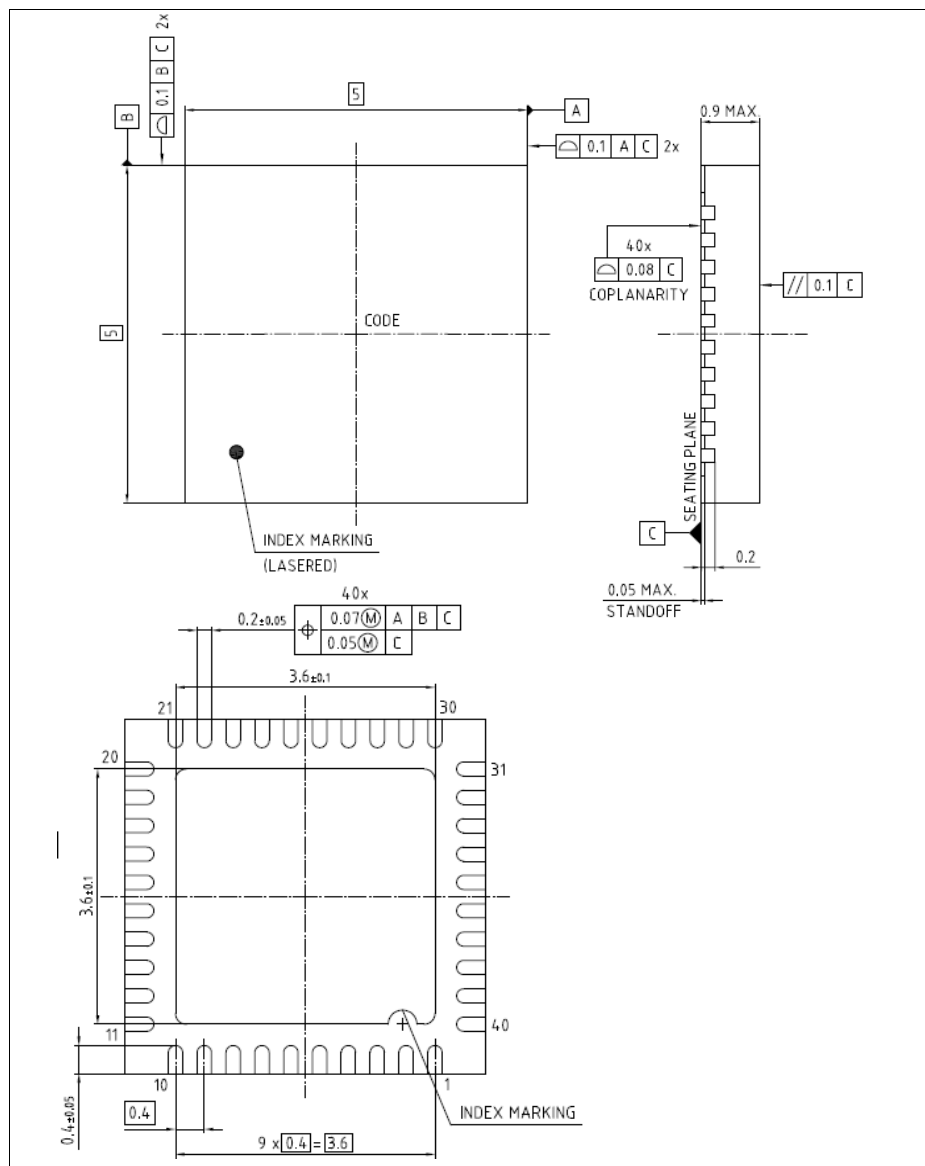


Figure 23 PG-VQFN-40-13

All dimensions in mm.

5 Quality Declaration

Table 32 shows the characteristics of the quality parameters in the XMC1300.

Table 32 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020C

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